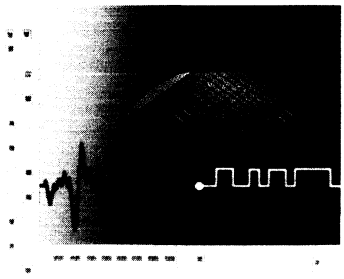
DATA BOOK

LEADERSHIP IN DATA CONVERSION AND SIGNAL PROCESSING



1993

SIGNAL PROCESSING TECHNOLOGIES

1993 DATA BOOK

4755 FORGE ROAD, COLORADO SPRINGS, CO 80907
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PRODUCT SELECTION GUIDE

MEDIUM-SPEED A/D CONVERTERS

PART NO.	GRADES	RESOLUTION (BITS)	CONVERSION TIME (μsec)	LINEARITY (LSB)	INPUT RANGES (V)	TEMP RANGE	PKGS / PINS	QUAL LEVEL	FEATURES
SPT774	A	12	8	1/2	±5, ±10	C, I, M	J, D, C, U	/883	MONOLITHIC, S/H FUNCTION, LOW POWER. ALTERNATIVE FOR HI774
	B			1/2	0-10, 0-20		/ 28		
	C			1					
HADC674Z	A	12	15	1/2	±5, ±10	C, I, M	J, D, C, U	/883	S/H FUNCTION LOW POWER
	B			1/2	0-10, 0-20		/ 28		HI674 ALTERNATIVE
	C			1					DESC DRAWING AVAILABLE
HADC574Z	A	12	25	1/2	±5, ±10	C, I, M	J, D, C, U	/883	S/H FUNCTION LOW POWER
	B			1/2	0-10, 0-20		/ 28		ALTERNATIVES FOR HI574 AND AD574
	C			1					DESC DRAWING AVAILABLE

D/A CONVERTERS - GENERAL PURPOSE

PART NO.	GRADES	RESOLUTION (BITS)	SETTLING TIME (ns)	INL (LSB)/ SNR (dB)	OUTPUT TYPE	TEMP RANGE	PKGS / PINS	QUAL LEVEL	FEATURES
HDAC7542A	A	12	500	1/2	I	C, I,M	D / 16	-	ALTERNATIVE FOR AD7542
	B			1					
HDAC7543A	A	12	500	1/2	I	C, I,M	D / 16	-	ALTERNATIVE FOR AD7543
	B			1					
HDAC52160	B	16	150	2/6**	I,V	C	J / 32		PARALLEL INPUT, REFERENCE, OUTPUT RANGE: +10 to 0, +5 to 0, ±5 OR ±2.5 V
	C			2/8**					
SPT5300	S	18	-	108	V	C	S / 32	*	PCM AUDIO

** OVER TEMPERATURE.

* CONSULT FACTORY FOR AVAILABILITY OF /883 PROCESSED UNITS.

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PRODUCT SELECTION GUIDE

D/A CONVERTERS - VIDEO

PART NO.	GRADES	RESOLUTION (BITS)	GLITCH ENERGY (PV -S)	LINEARITY (LSB)	CONVERSION RATE (MWPS)	TEMP RANGE	PKGS / PINS	QUAL LEVEL	FEATURES
HDAC10180	A	8	10	1/2	275	I/M	D / 24	/883	VIDEO CONTROL ALTERNATIVE FOR TDC1018
	B			1/2	165				
HDAC10181	A	8	10	1/2	275	I/M	D / 24	/883	VIDEO CONTROL WITH REFERENCE
	B			1/2	165				
HDAC51400	S	8	10	1/2	400	I/M	D/24	/883	REF, VIDEO CONTROL
SPT5220	S	10	-	1	80	C	N / 28	*	SINGLE +5 V SUPPLY VIDEO CONTROLS

COMPARATORS

PART NO.	GRADES	TR/TF (NS)	PROP DELAY (NS)	V_{CM} (V)	V_{OS} (V)	POWER DISSIPATION (mW)	TEMP RANGE	PKGS / PINS	FEATURES
HCMP96850	S	1.76/1.76	2.4	±2.5	±3.0	90	I	D, U / 16	SYMMETRICAL TR/TF, ALTERNATE FOR SP9685, AM6685, AD9685
HCMP96870/A	S	1.2/1.2	2.0	±2.5	±3.0	185	I	N, D, C, P, U / 16,16,20,20,16	HIGH PERFORMANCE, ALTERNATE FOR SP9687, AM6687, AD96687
SPT9689	A	.18/.08	.65	-2.5/+4.0	±10	350	I	J/C / 16/20	900 MHz BANDWIDTH DIFFERENTIAL LATCH CONTROL
	B				±25				
SPT9691	S	0.4/0.4	2.2	-4/+8.0	±25	700	I	J,C,P,N / 20	JFET INPUTS CONSTANT PROPAGATION DELAYS

FILTERS

PART NO.	GRADES	DYNAMIC RANGE (dB)	MAX BANDEDGE (kHz)	BANDEDGE TOLERANCE (%)	SUPPLY VOLTAGE (V)	TEMP RANGE	PKGS / PINS	FEATURES
HSCF24040	A	85	20	±0.5	±5.0	C	J / 32	7th ORDER LOW PASS, >76 dB STOPBAND ATTENUATION, ON-CHIP ANTI-ALIAS FILTER, DIGITALLY PROGRAMMABLE BANDEDGE AND DC

* CONSULT FACTORY FOR AVAILABILITY OF /883 PROCESSED UNITS.

PRODUCT CROSS REFERENCE GUIDE

(INDUSTRIAL SPT EQUIVALENT)

MAXIM	SPT	DESCRIPTION
MAX663	*SPT114xx/115xx	VOLTAGE REGULATOR
MAX667	*SPT114xx/115xx	VOLTAGE REGULATOR

MICRO POWER	SPT	DESCRIPTION
MP7542DIE	HDAC7542ACCU	DIE
MP7542AD	HDAC7542ABID	12-BIT DAC
MP7542BD	HDAC7542AAID	12-BIT DAC
MP7542SD	HDAC7542ABMD	12-BIT DAC
MP7542TD	HDAC7542AAMD	12-BIT DAC
MP7543DIE	HDAC7543ACCU	DIE
MP7543AD	HDAC7543ABID	12-BIT DAC
MP7543BD	HDAC7543AAID	12-BIT DAC
MP7543SD	HDAC7543ABMD	12-BIT DAC
MP7543TD	HDAC7543AAMD	12-BIT DAC

NATIONAL	SPT	DESCRIPTION
LM2931	SPT116xx	VOLTAGE REGULATOR
LM2931A	SPT116xx	VOLTAGE REGULATOR
LM2936	SPT116xx	VOLTAGE REGULATOR

PLESSEY	SPT	DESCRIPTION
SP9685DG	HCMP96850SID	SINGLE COMPARATOR
SP9687DG	HCMP96870SID/A	DUAL COMPARATOR

SEIKO	SPT	DESCRIPTION
S-8850	*SPT114xx/115xx	VOLTAGE REGULATOR
S-812xxAG	SPT116xx	VOLTAGE REGULATOR
S-812xxHG	SPT116xx	VOLTAGE REGULATOR
S-812xxPG	SPT116xx	VOLTAGE REGULATOR
S-813xxHG	SPT116xx	VOLTAGE REGULATOR

SONY	SPT	DESCRIPTION
CX20116	SPT7710AIJ	8-BIT, 150 MSPS ADC
CXA1396D	SPT7710AIJ	8-BIT, 150 MSPS ADC
CXD1175AM	SPT1175	8-BIT, 40 MSPS ADC

TEXAS INST	SPT	DESCRIPTION
TL751LXD	*SPT114xx/115xx	VOLTAGE REGULATOR
TL751LXP	*SPT114xx/115xx	VOLTAGE REGULATOR
TL750LXD	*SPT116xx	VOLTAGE REGULATOR
TL750LXP	*SPT116xx	VOLTAGE REGULATOR
TL750LXLP	SPT116xx	VOLTAGE REGULATOR

TRW	SPT	DESCRIPTION
TDC1018	HDAC10180	8-BIT, 275MWPS DAC
TMC1175M7C20	SPT1175	8-BIT, 40 MSPS ADC

* Functional Replacement

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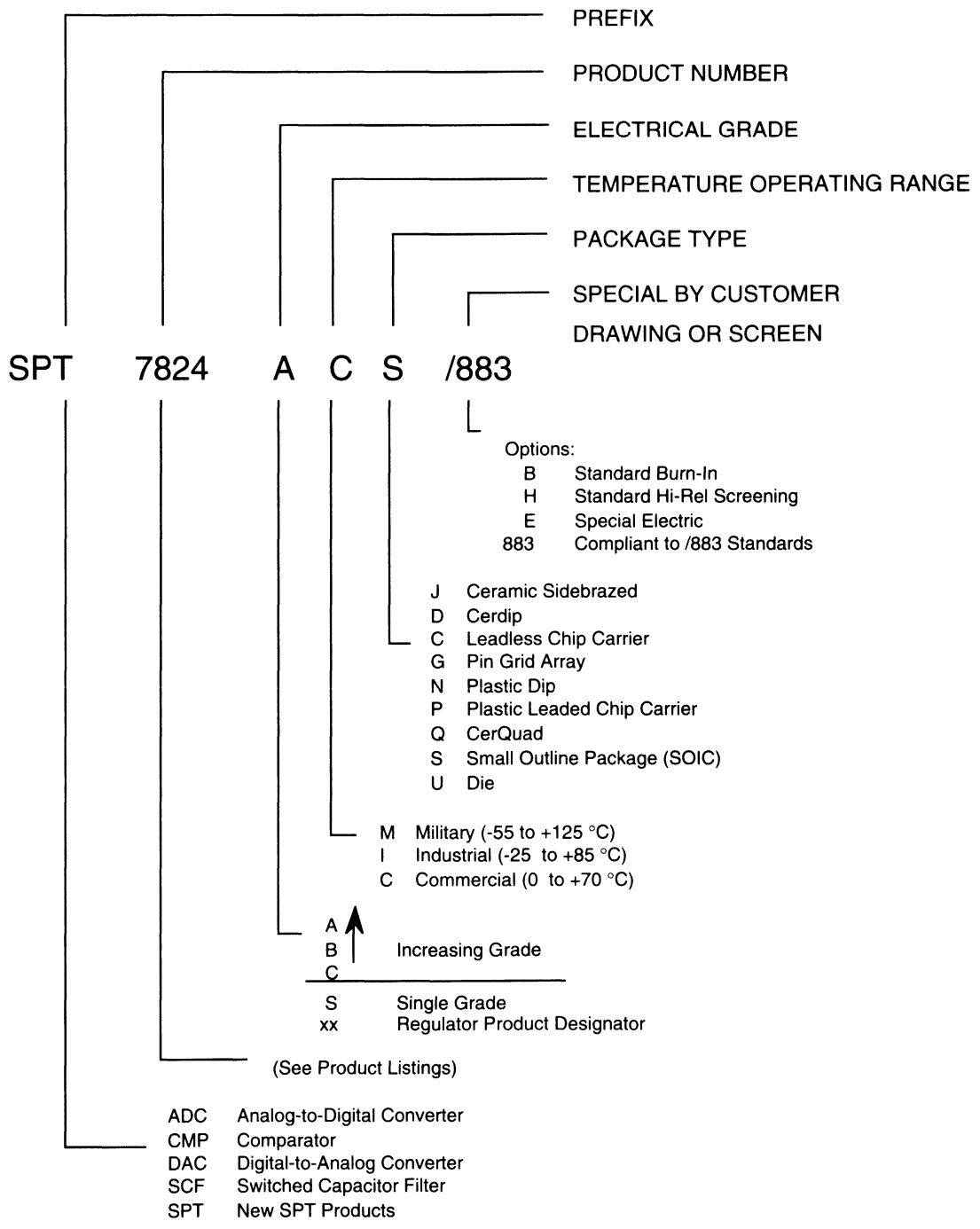
SPT PRODUCT IDENTIFICATION CODE



ORDERING INFORMATION

ANALOG-TO-DIGITAL CONVERTERS

PART NUMBER	DESCRIPTION	PACKAGE TYPE	# PINS	TEMPERATURE RANGE
HADC574ZAC(X)	12-BIT, 25 µsec ADC	SEE NOTE BELOW	28	COMMERCIAL
HADC574ZBC(X)	12-BIT, 25 µsec ADC	SEE NOTE BELOW	28	COMMERCIAL
HADC574ZCC(X)	12-BIT, 25 µsec ADC	SEE NOTE BELOW	28	COMMERCIAL
HADC574ZAI(X)	12-BIT, 25 µsec ADC	SEE NOTE BELOW	28	INDUSTRIAL
HADC574ZBI(X)	12-BIT, 25 µsec ADC	SEE NOTE BELOW	28	INDUSTRIAL
HADC574ZCI(X)	12-BIT, 25 µsec ADC	SEE NOTE BELOW	28	INDUSTRIAL
HADC574ZAM(X)	12-BIT, 25 µsec ADC	SEE NOTE BELOW	28	MILITARY
HADC574ZBM(X)	12-BIT, 25 µsec ADC	SEE NOTE BELOW	28	MILITARY
HADC574ZCM(X)	12-BIT, 25 µsec ADC	SEE NOTE BELOW	28	MILITARY
HADC574ZAM(X)/883	12-BIT, 25 µsec ADC	SEE NOTE BELOW	28	MILITARY/883
HADC574ZBM(X)/883	12-BIT, 25 µsec ADC	SEE NOTE BELOW	28	MILITARY/883
HADC574ZCM(X)/883	12-BIT, 25 µsec ADC	SEE NOTE BELOW	28	MILITARY/883
HADC574Z	12-BIT, 25 µsec ADC	DIE*		+25 °C
	DESC Drawing Number 5962-85127		28	MILITARY/883
HADC674ZAC(X)	12-BIT, 15 µsec ADC	SEE NOTE BELOW	28	COMMERCIAL
HADC674ZBC(X)	12-BIT, 15 µsec ADC	SEE NOTE BELOW	28	COMMERCIAL
HADC674ZCC(X)	12-BIT, 15 µsec ADC	SEE NOTE BELOW	28	COMMERCIAL
HADC674ZAI(X)	12-BIT, 15 µsec ADC	SEE NOTE BELOW	28	INDUSTRIAL
HADC674ZBI(X)	12-BIT, 15 µsec ADC	SEE NOTE BELOW	28	INDUSTRIAL
HADC674ZCI(X)	12-BIT, 15 µsec ADC	SEE NOTE BELOW	28	INDUSTRIAL
HADC674ZAM(X)	12-BIT, 15 µsec ADC	SEE NOTE BELOW	28	MILITARY
HADC674ZBM(X)	12-BIT, 15 µsec ADC	SEE NOTE BELOW	28	MILITARY
HADC674ZCM(X)	12-BIT, 15 µsec ADC	SEE NOTE BELOW	28	MILITARY
HADC674ZAM(X)/883	12-BIT, 15 µsec ADC	SEE NOTE BELOW	28	MILITARY/883
HADC674ZBM(X)/883	12-BIT, 15 µsec ADC	SEE NOTE BELOW	28	MILITARY/883
HADC674ZCM(X)/883	12-BIT, 15 µsec ADC	SEE NOTE BELOW	28	MILITARY/883
HADC674Z	12-BIT, 15 µsec ADC	DIE*		+25 °C
	DESC Drawing Number 5962-91690		28	MILITARY/883
SPT774AC(X)	12-BIT, 8 µsec ADC	SEE NOTE BELOW	28	COMMERCIAL
SPT774BC(X)	12-BIT, 8 µsec ADC	SEE NOTE BELOW	28	COMMERCIAL
SPT774CC(X)	12-BIT, 8 µsec ADC	SEE NOTE BELOW	28	COMMERCIAL
SPT774AI(X)	12-BIT, 8 µsec ADC	SEE NOTE BELOW	28	INDUSTRIAL
SPT774BI(X)	12-BIT, 8 µsec ADC	SEE NOTE BELOW	28	INDUSTRIAL
SPT774CI(X)	12-BIT, 8 µsec ADC	SEE NOTE BELOW	28	INDUSTRIAL
SPT774AM(X)	12-BIT, 8 µsec ADC	SEE NOTE BELOW	28	MILITARY
SPT774BM(X)	12-BIT, 8 µsec ADC	SEE NOTE BELOW	28	MILITARY
SPT774CM(X)	12-BIT, 8 µsec ADC	SEE NOTE BELOW	28	MILITARY
SPT774AM(X)/883	12-BIT, 8 µsec ADC	SEE NOTE BELOW	28	MILITARY/883
SPT774BM(X)/883	12-BIT, 8 µsec ADC	SEE NOTE BELOW	28	MILITARY/883
SPT774CM(X)/883	12-BIT, 8 µsec ADC	SEE NOTE BELOW	28	MILITARY/883
SPT774	12-BIT, 8 µsec ADC	DIE*		+25 °C

NOTE: (X) Denotes Package Type: J - SIDEBRAZED DIP; D - CERDIP; C - LCC

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ORDERING INFORMATION

ANALOG-TO-DIGITAL CONVERTERS - Continued

PART NUMBER	DESCRIPTION	PACKAGE TYPE	# PINS	TEMPERATURE RANGE
SPT1175SCN	8-BIT, 40 MSPS ADC	PLASTIC DIP	24	COMMERCIAL
SPT1175SCS	8-BIT, 40 MSPS ADC	SOIC	24	COMMERCIAL
SPT1175SCU	8-BIT, 40 MSPS ADC	DIE*		COMMERCIAL
SPT7710AIJ	8-BIT, 150 MSPS ADC ±.75 LSB	SIDEBRAZED	42	INDUSTRIAL
SPT7710BIJ	8-BIT, 150 MSPS ADC ±.95 LSB	SIDEBRAZED	42	INDUSTRIAL
SPT7710AIG	8-BIT, 150 MSPS ADC ±.75 LSB	PGA	46	INDUSTRIAL
SPT7710BIG	8-BIT, 150 MSPS ADC ±.95 LSB	PGA	46	INDUSTRIAL
SPT7710BCU	8-BIT, 150 MSPS ADC ±.95 LSB	DIE*		+25 °C
SPT7725AIJ	8-BIT, 150 MSPS ADC ±.75 LSB	SIDEBRAZED	42	INDUSTRIAL
SPT7725BIJ	8-BIT, 150 MSPS ADC ±.95 LSB	SIDEBRAZED	42	INDUSTRIAL
SPT7725AIG	8-BIT, 150 MSPS ADC ±.75 LSB	PGA	46	INDUSTRIAL
SPT7725BIG	8-BIT, 150 MSPS ADC ±.95 LSB	PGA	46	INDUSTRIAL
SPT7725BCU	8-BIT, 150 MSPS ADC ±.95 LSB	DIE*		+25 °C
SPT7750AIG	8-BIT, 500 MSPS ADC	PGA	68	INDUSTRIAL
SPT7750BIG	8-BIT, 500 MSPS ADC	PGA	68	INDUSTRIAL
SPT7750BCU	8-BIT, 500 MSPS ADC	DIE*		COMMERCIAL
SPT7810AIJ	10-BIT, 20 MSPS ADC	SIDEBRAZED	28	INDUSTRIAL
SPT7810BIJ	10-BIT, 20 MSPS ADC	SIDEBRAZED	28	INDUSTRIAL
SPT7810ACN	10-BIT, 20 MSPS ADC	PLASTIC DIP	28	COMMERCIAL
SPT7810BCN	10-BIT, 20 MSPS ADC	PLASTIC DIP	28	COMMERCIAL
SPT7810BCU	10-BIT, 20 MSPS ADC	DIE*		+25 °C
SPT7814AIJ	10-BIT, 40 MSPS ADC	SIDEBRAZED	28	INDUSTRIAL
SPT7814BIJ	10-BIT, 40 MSPS ADC	SIDEBRAZED	28	INDUSTRIAL
SPT7814ACN	10-BIT, 40 MSPS ADC	PLASTIC DIP	28	COMMERCIAL
SPT7814BCN	10-BIT, 40 MSPS ADC	PLASTIC DIP	28	COMMERCIAL
SPT7814BCU	10-BIT, 40 MSPS ADC	DIE*		+25 °C
SPT7820ACN	10-BIT, 20 MSPS ADC	PLASTIC DIP	28	COMMERCIAL
SPT7820BCN	10-BIT, 20 MSPS ADC	PLASTIC DIP	28	COMMERCIAL
SPT7820ACS	10-BIT, 20 MSPS ADC	SOIC	28	COMMERCIAL
SPT7820BCS	10-BIT, 20 MSPS ADC	SOIC	28	COMMERCIAL
SPT7820AIC	10-BIT, 20 MSPS ADC	LCC	28	INDUSTRIAL
SPT7820BIC	10-BIT, 20 MSPS ADC	LCC	28	INDUSTRIAL
SPT7820AIJ	10-BIT, 20 MSPS ADC	SIDEBRAZED	28	INDUSTRIAL
SPT7820BIJ	10-BIT, 20 MSPS ADC	SIDEBRAZED	28	INDUSTRIAL
SPT7820AMJ	10-BIT, 20 MSPS ADC	SIDEBRAZED	28	MILITARY
SPT7820BMJ	10-BIT, 20 MSPS ADC	SIDEBRAZED	28	MILITARY
SPT7820BCU	10-BIT, 20 MSPS ADC	DIE*		+25 °C
SPT7824ACN	10-BIT, 40 MSPS ADC	PLASTIC DIP	28	COMMERCIAL
SPT7824BCN	10-BIT, 40 MSPS ADC	PLASTIC DIP	28	COMMERCIAL
SPT7824ACS	10-BIT, 40 MSPS ADC	SOIC	28	COMMERCIAL
SPT7824BCS	10-BIT, 40 MSPS ADC	SOIC	28	COMMERCIAL
SPT7824AIC	10-BIT, 40 MSPS ADC	LCC	28	INDUSTRIAL
SPT7824BIC	10-BIT, 40 MSPS ADC	LCC	28	INDUSTRIAL
SPT7824AIJ	10-BIT, 40 MSPS ADC	SIDEBRAZED	28	INDUSTRIAL
SPT7824BIJ	10-BIT, 40 MSPS ADC	SIDEBRAZED	28	INDUSTRIAL
SPT7824AMJ	10-BIT, 40 MSPS ADC	SIDEBRAZED	28	MILITARY
SPT7824BMJ	10-BIT, 40 MSPS ADC	SIDEBRAZED	28	MILITARY
SPT7824BCU	10-BIT, 40 MSPS ADC	DIE*		+25 °C

* CONSULT FACTORY FOR AVAILABILITY

ORDERING INFORMATION

ANALOG-TO-DIGITAL CONVERTERS - Continued

PART NUMBER	DESCRIPTION	PACKAGE TYPE	# PINS	TEMPERATURE RANGE
SPT7840SCD	10-BIT, 10 MSPS ADC	CERDIP	28	COMMERCIAL
SPT7840SCN	10-BIT, 10 MSPS ADC	PLASTIC DIP	28	COMMERCIAL
SPT7840SCS	10-BIT, 10 MSPS ADC	SOIC	28	COMMERCIAL
SPT7840SCU	10-BIT, 10 MSPS ADC	DIE*		+25 °C
SPT7850SCD	10-BIT, 20 MSPS ADC	CERDIP	28	COMMERCIAL
SPT7850SCN	10-BIT, 20 MSPS ADC	PLASTIC DIP	28	COMMERCIAL
SPT7850SCS	10-BIT, 20 MSPS ADC	SOIC	28	COMMERCIAL
SPT7850SCU	10-BIT, 20 MSPS ADC	DIE*		+25 °C
SPT7860SCD	10-BIT, 40 MSPS ADC	CERDIP	28	COMMERCIAL
SPT7860SCN	10-BIT, 40 MSPS ADC	PLASTIC DIP	28	COMMERCIAL
SPT7860SCS	10-BIT, 40 MSPS ADC	SOIC	28	COMMERCIAL
SPT7860SCU	10-BIT, 40 MSPS ADC	DIE*		+25 °C
SPT7910SCJ	12-BIT, 10 MSPS ECL ADC	SIDEBRAZED	32	COMMERCIAL
SPT7910SCU	12-BIT, 10 MSPS ECL ADC	DIE*		+25 °C
SPT7912SCJ	12-BIT, 30 MSPS ECL ADC	SIDEBRAZED	32	COMMERCIAL
SPT7912SCU	12-BIT, 30 MSPS ECL ADC	DIE		+25 °C
SPT7920SCJ	12-BIT, 10 MSPS TTL ADC	SIDEBRAZED	32	COMMERCIAL
SPT7920SCU	12-BIT, 10 MSPS TTL ADC	DIE*		+25 °C
SPT7922SCJ	12-BIT, 30 MSPS TTL ADC	SIDEBRAZED	32	COMMERCIAL
SPT7922SCU	12-BIT, 30 MSPS TTL ADC	DIE*		+25 °C
SPT8100SCN	18-BIT ADC	PLASTIC DIP	32	COMMERCIAL

DIGITAL-TO-ANALOG CONVERTERS

PART NUMBER	DESCRIPTION	PACKAGE TYPE	# PINS	TEMPERATURE RANGE
HDAC7542AACD/G	12-BIT DAC	CERDIP	16	COMMERCIAL
HDAC7542AACD	12-BIT DAC	CERDIP	16	COMMERCIAL
HDAC7542ABCD	12-BIT DAC	CERDIP	16	COMMERCIAL
HDAC7542AAID/G	12-BIT DAC	CERDIP	16	INDUSTRIAL
HDAC7542AAID	12-BIT DAC	CERDIP	16	INDUSTRIAL
HDAC7542ABID	12-BIT DAC	CERDIP	16	INDUSTRIAL
HDAC7542AAMD/G	12-BIT DAC	CERDIP	16	MILITARY
HDAC7542AAMD	12-BIT DAC	CERDIP	16	MILITARY
HDAC7542ABMD	12-BIT DAC	CERDIP	16	MILITARY
HDAC7543AACD/G	12-BIT DAC	CERDIP	16	COMMERCIAL
HDAC7543AACD	12-BIT DAC	CERDIP	16	COMMERCIAL
HDAC7543ABCD	12-BIT DAC	CERDIP	16	COMMERCIAL
HDAC7543AAID/G	12-BIT DAC	CERDIP	16	INDUSTRIAL
HDAC7543AAID	12-BIT DAC	CERDIP	16	INDUSTRIAL
HDAC7543ABID	12-BIT DAC	CERDIP	16	INDUSTRIAL
HDAC7543AAMD/G	12-BIT DAC	CERDIP	16	MILITARY
HDAC7543AAMD	12-BIT DAC	CERDIP	16	MILITARY
HDAC7543ABMD	12-BIT DAC	CERDIP	16	MILITARY

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ORDERING INFORMATION

DIGITAL-TO-ANALOG CONVERTERS - Continued

PART NUMBER	DESCRIPTION	PACKAGE TYPE	# PINS	TEMPERATURE RANGE
HDAC10180AID	8-BIT, 275 MWPS DAC	CERDIP	24	INDUSTRIAL
HDAC10180BID	8-BIT, 165 MWPS DAC	CERDIP	24	INDUSTRIAL
HDAC10180AMD	8-BIT, 275 MWPS DAC	CERDIP	24	MILITARY
HDAC10180BMD	8-BIT, 165 MWPS DAC	CERDIP	24	MILITARY
HDAC10180AMD/883	8-BIT, 275 MWPS DAC	CERDIP	24	MILITARY/883
HDAC10180BMD/883	8-BIT, 165 MWPS DAC	CERDIP	24	MILITARY/883
	DESC Drawing Number 5962-91748	CERDIP	24	MILITARY/883
HDAC10181AID	8-BIT, 275 MWPS DAC W/REF	CERDIP	24	INDUSTRIAL
HDAC10181BID	8-BIT, 165 MWPS DAC W/REF	CERDIP	24	INDUSTRIAL
HDAC10181AMD	8-BIT, 275 MWPS DAC W/REF	CERDIP	24	MILITARY
HDAC10181BMD	8-BIT, 165 MWPS DAC W/REF	CERDIP	24	MILITARY
HDAC10181AMD/883	8-BIT, 275 MWPS DAC W/REF	CERDIP	24	MILITARY/883
HDAC10181BMD/883	8-BIT, 165 MWPS DAC W/REF	CERDIP	24	MILITARY/883
HDAC51400SID	8-BIT, 400 MWPS DAC W/REF	CERDIP	24	INDUSTRIAL
HDAC51400SMD	8-BIT, 400 MWPS DAC W/REF	CERDIP	24	MILITARY
HDAC51400SMD/883	8-BIT, 400 MWPS DAC W/REF	CERDIP	24	MILITARY/883
SPT5220SCN	10-BIT/80 MWPS	PLASTIC DIP	28	COMMERCIAL
HDAC52160BCJ	16-BIT RES DAC W/REF	SIDEBRAZED	32	COMMERCIAL
HDAC52160CCJ	16-BIT RES DAC W/REF	SIDEBRAZED	32	COMMERCIAL
HDAC52160CCU	16-BIT RES DAC W/REF	DIE*		+25 °C
SPT5300SCS	18-BIT AUDIO DAC	SOIC	32	COMMERCIAL

COMPARATORS

PART NUMBER	DESCRIPTION	PACKAGE TYPE	# PINS	TEMPERATURE RANGE
HCMP96850SID	HIGH-SPEED COMPARATOR	CERDIP	16	INDUSTRIAL
HCMP96850SCU	HIGH-SPEED COMPARATOR	DIE*		+25 °C
HCMP96870SIC/A	DUAL HIGH-SPEED COMPARATOR	LCC	20	INDUSTRIAL
HCMP96870SID/A	DUAL HIGH-SPEED COMPARATOR	CERDIP	16	INDUSTRIAL
HCMP96870SIJ/A	DUAL HIGH-SPEED COMPARATOR	SIDEBRAZED	16	INDUSTRIAL
HCMP96870SIN/A	DUAL HIGH-SPEED COMPARATOR	PLASTIC DIP	16	INDUSTRIAL
HCMP96870SIP/A	DUAL HIGH-SPEED COMPARATOR	PLCC	20	INDUSTRIAL
HCMP96870SCU/A	DUAL HIGH-SPEED COMPARATOR	DIE*		+25 °C
SPT9689AIJ	SUB-NANOSECOND COMPARATOR	SIDEBRAZED	20	INDUSTRIAL
SPT9689BIJ	SUB-NANOSECOND COMPARATOR	SIDEBRAZED	20	INDUSTRIAL
SPT9689AIC	SUB-NANOSECOND COMPARATOR	LCC	20	INDUSTRIAL
SPT9689BIC	SUB-NANOSECOND COMPARATOR	LCC	20	INDUSTRIAL
SPT9689BCU	SUB-NANOSECOND COMPARATOR	DIE*		+25 °C
SPT9691SCJ	JFET COMPARATOR	SIDEBRAZED	20	COMMERCIAL
SPT9691SCC	JFET COMPARATOR	LCC	20	COMMERCIAL
SPT9691SCN	JFET COMPARATOR	PLASTIC DIP	20	COMMERCIAL
SPT9691SCP	JFET COMPARATOR	PLCC	20	COMMERCIAL
SPT9691SCU	JFET COMPARATOR	DIE*	20	+25 °C

* ***CONSULT FACTORY FOR AVAILABILITY***

ORDERING INFORMATION

FILTERS

PART NUMBER	DESCRIPTION	PACKAGE TYPE	# PINS	TEMPERATURE RANGE
HSCF24040ACJ	LOW PASS PROGRAMMABLE FILTER	SIDEBRAZED	32	COMMERCIAL
HSCF24040	LOW PASS PROGRAMMABLE FILTER	DIE*		+25 °C

VOLTAGE REGULATORS

PART NUMBER	DESCRIPTION	PACKAGE TYPE	# PINS	TEMPERATURE RANGE
SPT11220TI(XX)	2.0 V OUTPUT	SOT23L	6	INDUSTRIAL
SPT11221TI(XX)	2.1 V OUTPUT	SOT23L	6	INDUSTRIAL
SPT11222TI(XX)	2.25 V OUTPUT	SOT23L	6	INDUSTRIAL
SPT11225TI(XX)	2.5 V OUTPUT	SOT23L	6	INDUSTRIAL
SPT11227TI(XX)	2.75 V OUTPUT	SOT23L	6	INDUSTRIAL
SPT11230TI(XX)	3.0 V OUTPUT	SOT23L	6	INDUSTRIAL
SPT11232TI(XX)	3.25 V OUTPUT	SOT23L	6	INDUSTRIAL
SPT11235TI(XX)	3.5 V OUTPUT	SOT23L	6	INDUSTRIAL
SPT11240TI(XX)	4.0 V OUTPUT	SOT23L	6	INDUSTRIAL
SPT11245TI(XX)	4.5 V OUTPUT	SOT23L	6	INDUSTRIAL
SPT11247TI(XX)	4.75 V OUTPUT	SOT23L	6	INDUSTRIAL
SPT11250TI(XX)	5.0 V OUTPUT	SOT23L	6	INDUSTRIAL
SPT11255TI(XX)	5.5 V OUTPUT	SOT23L	6	INDUSTRIAL
SPT11260TI(XX)	6.0 V OUTPUT	SOT23L	6	INDUSTRIAL
SPT11220TI(XX)	8.0 V OUTPUT	SOT23L	6	INDUSTRIAL
SPT11420M	2.0 VOLT OUTPUT	SOT23L	6	COMMERCIAL
SPT11425M	2.5 VOLT OUTPUT	SOT23L	6	COMMERCIAL
SPT11430M	3.0 VOLT OUTPUT	SOT23L	6	COMMERCIAL
SPT11432M	3.25 VOLT OUTPUT	SOT23L	6	COMMERCIAL
SPT11435M	3.5 VOLT OUTPUT	SOT23L	6	COMMERCIAL
SPT11440M	4.0 VOLT OUTPUT	SOT23L	6	COMMERCIAL
SPT11445M	4.5 VOLT OUTPUT	SOT23L	6	COMMERCIAL
SPT11450M	5.0 VOLT OUTPUT	SOT23L	6	COMMERCIAL
SPT11455M	5.5 VOLT OUTPUT	SOT23L	6	COMMERCIAL
SPT11460M	6.0 VOLT OUTPUT	SOT23L	6	COMMERCIAL
SPT11480M	8.0 VOLT OUTPUT	SOT23L	6	COMMERCIAL
SPT114xxMTR**	TAPE AND REEL (RIGHT)	SOT23L	6	COMMERCIAL
SPT114xxMTL**	TAPE AND REEL (LEFT)	SOT23L	6	COMMERCIAL
SPT11525M	2.5 VOLT OUTPUT	MFP-8	8	COMMERCIAL
SPT11530M	3.0 VOLT OUTPUT	MFP-8	8	COMMERCIAL
SPT11532M	3.25 VOLT OUTPUT	MFP-8	8	COMMERCIAL
SPT11535M	3.5 VOLT OUTPUT	MFP-8	8	COMMERCIAL
SPT11540M	4.0 VOLT OUTPUT	MFP-8	8	COMMERCIAL
SPT11545M	4.5 VOLT OUTPUT	MFP-8	8	COMMERCIAL
SPT11547M	4.75 VOLT OUTPUT	MFP-8	8	COMMERCIAL
SPT11550M	5.0 VOLT OUTPUT	MFP-8	8	COMMERCIAL
SPT11555M	5.5 VOLT OUTPUT	MFP-8	8	COMMERCIAL
SPT11580M	8.0 VOLT OUTPUT	MFP-8	8	COMMERCIAL
SPT115xxMT**	TAPE AND REEL	MFP-8	8	COMMERCIAL

* ***CONSULT FACTORY FOR AVAILABILITY***

** ***DESIGNATOR xx DENOTES AVAILABILITY OF ANY STANDARD VOLTAGE OPTION.***

(XX) Denotes: BX Bulk/Bag
TX Paper Tape
TR Tape Right
TL Tape Left
MG Magazine

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ORDERING INFORMATION

VOLTAGE REGULATORS - CONTINUED

PART NUMBER	DESCRIPTION	PACKAGE TYPE	# PINS	TEMPERATURE RANGE
SPT11620N	2.0 VOLT OUTPUT	TO-92N	3	COMMERCIAL
SPT11625N	2.5 VOLT OUTPUT	TO-92N	3	COMMERCIAL
SPT11630N	3.0 VOLT OUTPUT	TO-92N	3	COMMERCIAL
SPT11635N	3.5 VOLT OUTPUT	TO-92N	3	COMMERCIAL
SPT11640N	4.0 VOLT OUTPUT	TO-92N	3	COMMERCIAL
SPT11645N	4.5 VOLT OUTPUT	TO-92N	3	COMMERCIAL
SPT11650N	5.0 VOLT OUTPUT	TO-92N	3	COMMERCIAL
SPT11655N	5.5 VOLT OUTPUT	TO-92N	3	COMMERCIAL
SPT116xxNT**	PLASTIC TAPE	TO-92N	3	COMMERCIAL
SPT11948MC(YY)	4.8 V REGULATOR	SOT23L	6	COMMERCIAL
SPT11948MI(YY)	4.8 V REGULATOR	SOT23L	6	INDUSTRIAL
SPT11950MC(YY)	5.0 V REGULATOR	SOT23L	6	COMMERCIAL
SPT11950MI(YY)	5.0 V REGULATOR	SOT23L	6	INDUSTRIAL
SPT120MC(YY)	1.5 to 6.0 V REGULATOR	SOT23L	6	COMMERCIAL
SPT120MI(YY)	1.5 to 6.0 V REGULATOR	SOT23L	6	INDUSTRIAL

RF AMPLIFIERS

PART NUMBER	DESCRIPTION	PACKAGE TYPE	# PINS	TEMPERATURE RANGE
SPT201	1,000 MHz RF AMPLIFIER	UPACK-5	6	INDUSTRIAL
SPT202	250 MHz RF AMPLIFIER	UPACK-5	6	INDUSTRIAL
SPT203	500 MHz RF AMPLIFIER	UPACK-5	6	INDUSTRIAL
SPT203	500 MHz RF AMPLIFIER	MFP-8	8	INDUSTRIAL

POWER CONVERSION PRODUCTS

PART NUMBER	DESCRIPTION	PACKAGE TYPE	# PINS	TEMPERATURE RANGE
SPT84819D	POWER FACTOR CONTROLLER	PLASTIC DIP	20	COMMERCIAL
SPT84819DA	POWER FACTOR CONTROLLER	PLASTIC DIP	20	INDUSTRIAL

EVALUATION BOARDS

EB104	HADC574Z/674Z and SPT774 DEMO BOARD
EB105	HSCF24040 DEMO BOARD
EB1175	SPT1175 DEMO BOARD
EB7710/25	SPT7710/25 DEMO BOARD
EB7750	SPT7750 DEMO BOARD
EB7810/14	SPT7810/7814 DEMO BOARD
EB7820/24	SPT7820/7824 DEMO BOARD
EB7840/50/60	SPT7840/50/60 DEMO BOARD
EB791	SPT791 DEMO BOARD
EB7910/12	SPT7910/7912 DEMO BOARD
EB7920/22	SPT7920/7922 DEMO BOARD

YY Denotes:
BX Bulk/Bag
TR Tape Right
TL Tape Left

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Section 3 Analog-to-Digital Converters

3

HADC574Z	12-Bit, 25 µsec BiCMOS	3-5
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SIGNAL PROCESSING TECHNOLOGIES

HADC574Z

FAST, COMPLETE 12-BIT µP COMPATIBLE A/D CONVERTER WITH SAMPLE/HOLD

3

FEATURES

- Improved Pin-To-Pin Compatible Monolithic Version of the HI574A and AD574A
- Complete 12-Bit A/D Converter with Sample/Hold, Reference and Clock
- Low Power Dissipation (150 mW Max)
- 12-Bit Linearity (Over Temp)
- 25 µs Max Conversion Time
- No Negative Supply Required
- Full Bipolar and Unipolar Input Range

APPLICATIONS

- Military/Industrial Data Acquisition Systems
- 8 or 12-Bit µP Input Functions
- Process Control Systems
- Test and Scientific Instruments
- Personal Computer Interface

GENERAL DESCRIPTION

The HADC574Z is a complete, 12-bit successive approximation A/D converter. The device is integrated on a *single die* to make it the first monolithic CMOS version of the industry standard device, HI574A and AD574A. Included on chip is an internal reference, clock, and a sample and hold. The S/H is an additional feature not available on similar devices.

The HADC574Z features 25 µs (Max) conversion time of 10 or 20 Volt input signals. Also, a three-state output buffer is added for direct interface to an 8, 12, or 16-bit µP bus.

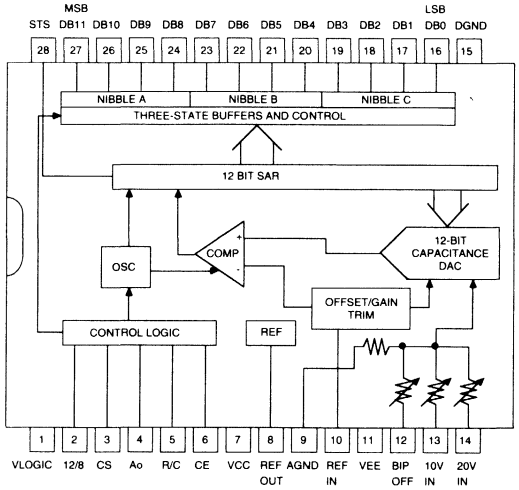
The HADC574Z is manufactured on a Bipolar Enhanced CMOS process (BEMOS) which combines CMOS logic and fast bipolar npn transistors to yield high performance digital and analog functions on one chip.

The BEMOS process and monolithic construction reduces power consumption, ground noise, and keeps parasitics to a minimum. In addition, the thin film option on this process allows active adjustment of DAC and comparator offsets, linearity errors, and gain errors.

The HADC574Z has standard bipolar and unipolar input ranges of 10 V and 20 V that are controlled by a bipolar offset pin and laser trimmed for specified linearity, gain and offset accuracy.

Power requirements are +5 V and +12 V to +15 V with a maximum dissipation of 150 mW at the specified voltages. Power consumption is about five times lower than currently available devices, and a negative power supply is not needed. A standard military drawing is published under DESC number 596281527.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATING (Beyond which damage may occur) [1] 25 °C

Supply Voltages

Positive Supply Voltage (V_{CC} to DGND) .....0 to +16.5 V
Logic Supply Voltage (V_{LOGIC} to DGND) .....0 to +7 V
Analog to Digital Ground (AGND to DGND) .-0.5 to +1 V

Input Voltages

Control Input Voltages (to DGND)
(CE, CS, Ao, 12/8, R/C) .....-0.5 to V_{LOGIC} +0.5 V
Analog Input Voltage (to AGND)
(REF IN, BIP OFF, 10 Vin) .....±16.5 V
20 V Vin Input Voltage (to AGND) .....±24 V

Output

Reference Output Voltage .....Indefinite short to GND
Momentary short to V_{CC}

Temperature

Operating Temperature, ambient .....-55 to +125 °C
junction .....+175 °C
Lead Temperature, (soldering 10 seconds).....+300 °C
Storage Temperature .....-65 to +150 °C
Power Dissipation .....1000 mW
Thermal Resistance (θ_{jA}) .....48 °C/W

Note: Operation at any Absolute Maximum Rating is not implied. See Operating Conditions for proper nominal applied conditions in typical applications.

ELECTRICAL SPECIFICATIONS

$T_A=T_{MIN}$ to T_{MAX}, V_{CC}=+15 V or +12 V, V_{LOGIC}=+5 V, unless otherwise specified.

PARAMETER	TEST CONDITIONS	TEST LEVEL	HADC574ZC MIN	HADC574ZC TYP	HADC574ZC MAX	HADC574ZB MIN	HADC574ZB TYP	HADC574ZB MAX	HADC574ZA MIN	HADC574ZA TYP	HADC574ZA MAX	UNITS
DC ELECTRICAL CHARACTERISTICS												
Resolution		VI			12			12			12	BITS
Linearity Error[1]	T_A=0 to 70 °C	VI			±1			±1/2			±1/2	LSB
	T_A = -25 to +85 °C	I			±1			±1/2			±1/2	LSB
	T_A = -55 to +125 °C	I			±1			±1			±1	LSB
Differential Linearity	No Missing Codes	VI	11			12			12			BITS
Unipolar Offset; 10 V, 20 V	+25 °C Adjustable to Zero	VI		±0.1	±2		±0.1	±2		±0.1	±2	LSB
Bipolar Offset1; ±5 V,±10 V	+25 °C Adjustable to Zero	VI			±10			±4			±4	LSB
Full Scale Calibration Error[2] All Input Ranges	+25 °C Adjustable to Zero	VI			0.3			0.3			0.3	% of FS
	No Adjustment at +25°											
	T_A = 0 to 70 °C	V		0.5			0.4			0.35		%of FS
	T_A = -25 to +85 °C	V		0.7			0.5			0.4		%of FS
	T_A = -55 to +125 °C	V		0.8			0.6			0.4		%of FS
	With Adjustment at +25 °C											
	T_A = 0 to 70 °C	V		0.22			0.12			0.05		%of FS
	T_A = -25 to +85 °C	V		0.4			0.2			0.1		%of FS
	T_A = -55 to +125 °C	V		0.5			0.25			0.12		%of FS
Temperature Coefficients[3]	Using Internal Reference											
Unipolar Offset	T_A = 0 to 70 °C	IV		±0.2	±2		±0.1	±1		±0.1	±1	LSB
					(10)			(5)			(5)	(ppm/°C)
	T_A = -25 to +85 °C	IV			±2			±1			±1	LSB
					(5)			(2.5)			(2.5)	(ppm/°C)
	T_A = -55 to +125 °C	IV			±2			±1			±1	LSB
					(5)			(2.5)			(2.5)	(ppm/°C)
Bipolar Offset	T_A = 0 to 70 °C	IV		±0.2	±2		±0.1	±1		±0.1	±1	LSB
					(10)			(5)			(5)	(ppm/°C)
	T_A = -25 to +85 °C	IV			±2			±1			±1	LSB
					(5)			(2.5)			(2.5)	(ppm/°C)

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ELECTRICAL SPECIFICATIONS

$T_A = T_{MIN}$ to T_{MAX}, V_{CC} = +15 V or +12 V, V_{LOGIC} = +5 V, unless otherwise specified.

PARAMETER	TEST CONDITIONS	TEST LEVEL	HADC574ZC MIN	HADC574ZC TYP	HADC574ZC MAX	HADC574ZB MIN	HADC574ZB TYP	HADC574ZB MAX	HADC574ZA MIN	HADC574ZA TYP	HADC574ZA MAX	UNITS
DC ELECTRICAL CHARACTERISTICS												
Bipolar Offset (Cont.)	T_A = -55 to +125 °C	IV			±4 (10)			±2 (5)			±1 (2.5)	LSB (ppm/°C)
Full Scale Calibration	T_A = 0 to 70 °C	IV			±9 (45)			±5 (25)			±2 (10)	LSB (ppm/°C)
	T_A = -25 to +85 °C	IV			±12 (50)			±7 (25)			±3 (12)	LSB (ppm/°C)
	T_A = -55 to +125 °C	IV			±20 (50)			±10 (25)			±5 (12.5)	LSB (ppm/°C)
Power Supply Rejection	Max change in full scale calibration											
+13.5 V<V_{CC}<+16.5 V or +11.4 V<V_{CC}<+12.6 V		VI		±0.5	±2		±0.5	±1		±0.5	±1	LSB
+4.5 V<V_{LOGIC}<+5.5 V		VI		±0.1	±0.5		±0.1	±0.5		±0.1	±0.5	LSB
Analog Input Ranges												
Bipolar		VI	-5		+5	-5		+5	-5		+5	Volts
			-10		+10	-10		+10	-10		+10	Volts
Unipolar		VI	0		+10	0		+10	0		+10	Volts
			0		+20	0		+20	0		+20	Volts
Input Impedance												
10 Volt Span		VI	3.75	5	6.25	3.75	5	6.25	3.75	5	6.25	kΩ
20 Volt Span			15	20	25	15	20	25	15	20	25	kΩ
Power Supplies Operating Voltage Range												
V_{LOGIC}		VI	+4.5		+5.5	+4.5		+5.5	+4.5		+5.5	Volts
V_{CC}		VI	+11.4		+16.5	+11.4		+16.5	+11.4		+16.5	Volts
V_{EE}	Not Required for circuit operation.											
Operating Current												
I_{LOGIC}		VI		0.5	1		0.5	1		0.5	1	mA
I_{CC}		VI		7	9		7	9		7	9	mA
I_{EE}	Not required for circuit operation.											
Power Dissipation +15 V, +5 V		VI		110	150		110	150		110	150	mW
Internal Reference Voltage		VI	9.97	10	10.03	9.97	10	10.03	9.97	10	10.03	Volts
Output Current[4]		VI			2			2			2	mA

ELECTRICAL SPECIFICATIONS

$T_A = T_{MIN}$ to T_{MAX}, V_{CC} = +15 V or +12 V, V_{LOGIC} = +5 V, unless otherwise specified.

PARAMETER	TEST CONDITIONS	TEST LEVEL	HADC574ZC MIN	HADC574ZC TYP	HADC574ZC MAX	HADC574ZB MIN	HADC574ZB TYP	HADC574ZB MAX	HADC574ZA MIN	HADC574ZA TYP	HADC574ZA MAX	UNITS
DIGITAL CHARACTERISTICS												
Logic Inputs (CE, $\overline{CS}$, R/$\overline{C}$, Ao, 12/$\overline{8}$)												
Logic "0"		VI	-0.5		+0.8	-0.5		+0.8	-0.5		+0.8	Volts
Logic "1"		VI	2.0		5.5	2.0		5.5	2.0		5.5	Volts
Current	0 to 5.5 V Input	VI		±.01	+1		±.01	+1		±.01	+1	µA
Capacitance		V		5			5			5		pF
Logic Outputs (DB11-DB0, STS)												
Logic "0"	(I_{Sink} = 1.6 mA)	VI			+0.4			+0.4			+0.4	Volts
Logic "1"	(I_{SOURCE} = 500 µA)	VI	+2.4			+2.4			+2.4			Volts
Leakage	(High Z State, DB11-DB0 Only)	VI	-5	±0.1	+5	-5	±0.1	+5	-5	±0.1	+5	µA
Capacitance		V		5			5			5		pF

Note 1: For military temperature range, the device linearity is guaranteed to be 1/2 LSB at 25 °C.
Note 2: Fixed 50 Ω resistor from REF OUT to REF IN and REF OUT to BIP OFF.
Note 3: Full Tempco testing is performed on all Grade A and MIL-STD-883 devices.
Note 4: Available for external loads, external load should not change during conversion. When supplying an external load and operating on a +12.0 V supply, a buffer amplifier must be provided for the reference output.

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ELECTRICAL SPECIFICATIONS

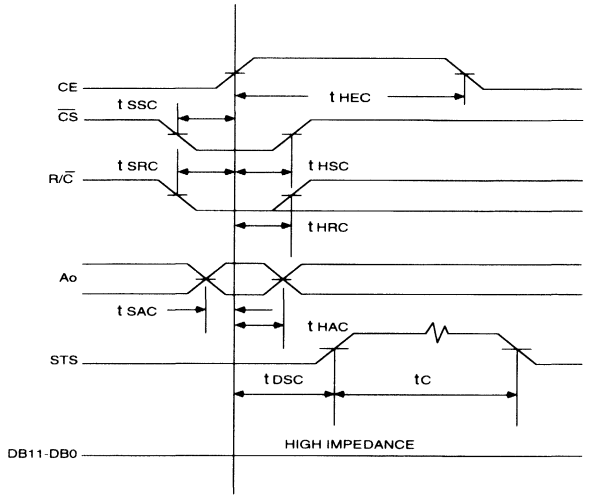
CONVERT MODE TIMING CHARACTERISTICS

T_A = +25 °C, V_{CC} = +15.0 V or +12 V, V_{LOGIC} = +5 V, unless otherwise specified.

PARAMETER	TEST CONDITIONS	TEST LEVEL	HADC574ZC MIN	HADC574ZC TYP	HADC574ZC MAX	HADC574ZB MIN	HADC574ZB TYP	HADC574ZB MAX	HADC574ZA MIN	HADC574ZA TYP	HADC574ZA MAX	UNITS
AC ELECTRICAL CHARACTERISTICS[1]												
t_{DSC} STS Delay from CE		I			200			200			200	ns
t_{HEC} CE Pulse Width		I	50			50			50			ns
t_{SSC} $\overline{CS}$ to CE Setup		I	50			50			50			ns
t_{HSC} $\overline{CS}$ Low during CE High		I	50			50			50			ns
t_{SRC} R/$\overline{C}$ to CE Setup		I	50			50			50			ns
t_{HRC} R/$\overline{C}$ Low During CE High		I	50			50			50			ns
t_{SAC} Ao to CE Setup		I	0			0			0			ns
t_{HAC} Ao Valid During CE High		I	50			50			50			ns
t_C Conversion Time												
12-Bit Cycle	T_{MIN} to T_{MAX}	I	13	18	25	15	18	25	15	18	25	µs
8-Bit Cycle	T_{MIN} to T_{MAX}	I	10	13	19	10	13	17	10	13	17	µs

Note 1: Time is measured from 50% level of digital transitions. Tested with a 100 pF and 3 kΩ load for high impedance to drive and tested with 10 pF and 3 kΩ load for drive to high impedance.

Figure 1 - Convert Mode Timing Diagram



ELECTRICAL SPECIFICATIONS

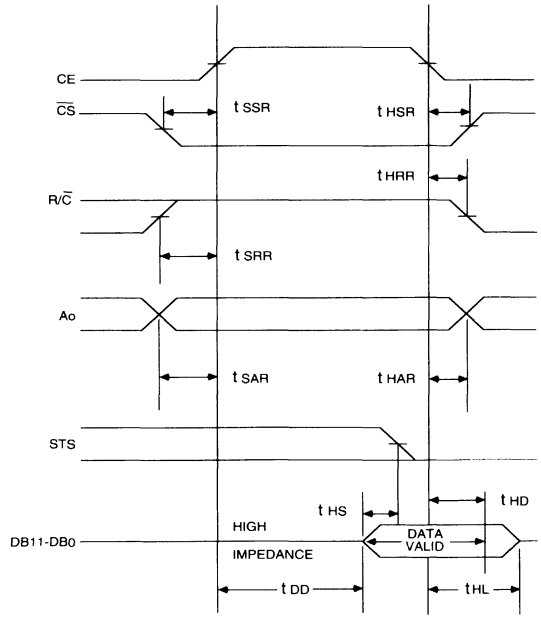
READ MODE TIMING CHARACTERISTICS

T_A = 25 °C, V_{CC} = +15.0 V or +12 V, V_{LOGIC} = +5 V, unless otherwise specified.

PARAMETER	TEST CONDITIONS	TEST LEVEL	HADC574ZC MIN	HADC574ZC TYP	HADC574ZC MAX	HADC574ZB MIN	HADC574ZB TYP	HADC574ZB MAX	HADC574ZA MIN	HADC574ZA TYP	HADC574ZA MAX	UNITS
AC ELECTRICAL CHARACTERISTICS[1]												
t_{DD} Access Time from CE		I			150			150			150	ns
t_{HD} Data Valid After CE Low		I	25			25			25			ns
t_{HL} Output Float Delay		I			150			150			150	ns
t_{SSR} $\overline{CS}$ to CE Setup		I	50	0		50	0		50	0		ns
t_{SRR} R/$\overline{C}$ to CE Setup		I	0	0		0	0		0	0		ns
t_{SAR} Ao to CE Setup		I	50			50			50			ns
t_{HSR} $\overline{CS}$ Valid After CE Low		I	0	0		0	0		0	0		ns
t_{HRR} R/$\overline{C}$ High After CE Low		I	50			50			50			ns
t_{HS} STS Delay After Data Valid		I	300		1000	300		1000	300		1000	ns
t_{HAR} Ao Valid after CE Low		I	50			50			50			ns

Note 1: Time is measured from 50% level of digital transitions. Tested with a 100 pF and 3 kΩ load for high impedance to drive and tested with 10 pF and 3 kΩ load for drive to high impedance.

Figure 2 - Read Mode Timing Diagram



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ELECTRICAL SPECIFICATIONS

STAND-ALONE MODE TIMING CHARACTERISTICS

T_A = 25 °C, V_{CC} = +15.0 V or +12 V, V_{LOGIC} = +5 V, unless otherwise specified.

PARAMETER	TEST CONDITIONS	LEVEL	HADC574ZC MIN	HADC574ZC TYP	HADC574ZC MAX	HADC574ZB MIN	HADC574ZB TYP	HADC574ZB MAX	HADC574ZA MIN	HADC574ZA TYP	HADC574ZA MAX	UNITS
AC ELECTRICAL CHARACTERISTICS												
t_{HRL} Low R/$\overline{C}$ Pulse Width		I	50			50			50			ns
t_{DS} STS Delay from R/$\overline{C}$		I			200			200			200	ns
t_{HDR} Data Valid After R/$\overline{C}$ Low		I	25			25			25			ns
t_{HS} STS Delay After Data Valid		I	300		1000	300		1000	300		1000	ns
t_{HRH} High R/$\overline{C}$ Pulse Width		I	150			150			150			ns
t_{DDR} Data Access Time		I			150			150			150	ns
SAMPLE AND HOLD												
Acquisition Time		IV	1.8	2.4	3.4	1.8	2.4	3.4	1.8	2.4	3.4	µs
Aperture Uncertainty Time		V		8			8			8		ns,RMS

Figure 3 - Low Pulse for R/$\overline{C}$ - Outputs Enabled After Conversion

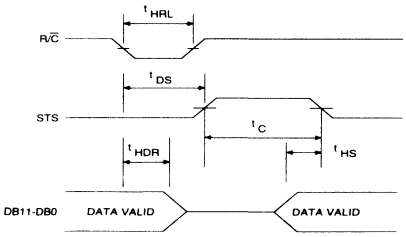
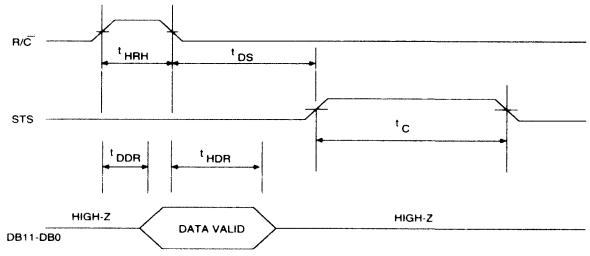


Figure 4 - High Pulse for R/$\overline{C}$ - Outputs Enabled While R/$\overline{C}$ is High, Otherwise High Impedance



TEST LEVEL CODES

All electrical characteristics are subject to the following conditions:

All parameters having min/max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality Assurance inspection. Any blank section in the data column indicates that the specification is not tested at the specified condition.

Unless otherwise noted, all tests are pulsed tests; therefore, $T_J = T_C = T_A$.

TEST LEVEL	TEST PROCEDURE
I	100% production tested at the specified temperature.
II	100% production tested at T_A=25 °C, and sample tested at the specified temperatures.
III	QA sample tested only at the specified temperatures.
IV	Parameter is guaranteed (but not tested) by design and characterization data.
V	Parameter is a typical value for information purposes only.
VI	100% production tested at T_A = 25 °C. Parameter is guaranteed over specified temperature range.

DEFINITION OF SPECIFICATIONS

INTEGRAL LINEARITY ERROR

Linearity error refers to the deviation of each individual code from a line drawn from "zero" through "full scale" with all offset errors nulled out (See Figure 5 and 6). The point used as "zero" occurs 1/2 LSB (1.22 mV for a 10 Volt span) before the first code transition (all zeros to only the LSB "on"). "Full scale" is defined as a level 1 and 1/2 LSB beyond the last code transition (to all ones). The deviation of a code from the true straight line is measured from the middle of each particular code.

The HADC574ZAC and BC grades are guaranteed for maximum nonlinearity of ±1/2 LSB. For these grades, this means that an analog value which falls exactly in the center of a given code width will result in the correct digital output code. Values nearer the upper or lower transition of the code width may produce the next upper or lower digital output code. The HADC574ZAM, BM, CC and CM grades are guaranteed to ±1 LSB maximum error. For these grades, an analog value which falls within a given code width will result in either the correct code for the region or either adjacent one. The linearity is not user-adjustable.

DIFFERENTIAL LINEARITY ERROR (NO MISSING CODES)

A specification which guarantees no missing codes requires that every code combination appear in a monotonically increasing sequence as the analog input level is increased. Thus every code must have a finite width. For the HADC574Z type BC, AC, BM and AM grades, which guarantee no missing codes to 12-bit resolution, all 4096 codes must be present over the entire operating temperature ranges. The HADC574Z CC and CM grades guarantee no missing codes to 11-bit resolution over temperature; this means that all code combinations of the upper 11-bits must be present; in practice, very few of the 12-bit codes are missing.

DIFFERENTIAL NONLINEARITY

Differential nonlinearity is a measure of how much the actual quantization step width varies from the ideal step width of 1 LSB. Figure 6 shows a differential nonlinearity of 2 LSB - the actual step width is 3 LSB. The HADC574Z's specification gives the worst case differential nonlinearity in the A/D transfer function under specified dynamic operating conditions. Small, localized differential nonlinearities may be insignificant when digitizing full scale signals. However, if a low level input signal happens to fall on the part of the A/D transfer function with the differential nonlinearity error, the effect will be significant.

MISSING CODES

Missing codes represent a special kind of differential nonlinearity. The quantization step width for a missing code is 0 LSB, which results in a differential nonlinearity of -1 LSB. Figure 6 points out two missed codes in the transfer function.

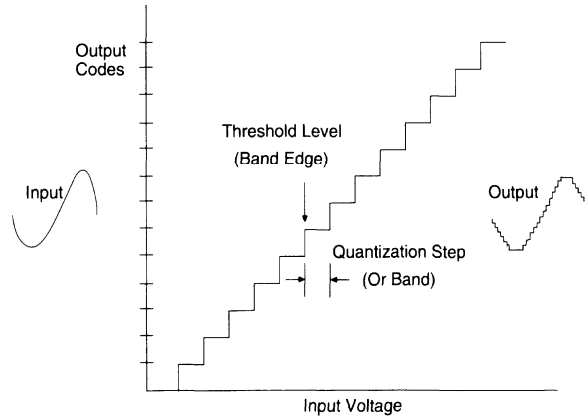
QUANTIZATION UNCERTAINTY

Analog-to-digital converters exhibit an inherent quantization uncertainty of ±1/2 LSB. This uncertainty is a fundamental characteristic of the quantization process and cannot be reduced for a converter of a given resolution.

QUANTIZATION ERROR

Quantization error is the fundamental, irreducible error associated with the perfect quantizing of a continuous (analog) signal into a finite number of digital bits (A/D transfer function). A 12-bit A/D converter can represent an input voltage with a best case uncertainty of 1 part in 2^{12} (1 part in 4096). In real A/Ds under dynamic operating conditions, the quantization bands (bit change step vs input amplitude) for certain codes can be significantly larger (or smaller) than the ideal. The ideal width of each quantization step (or band) is Q=FSR/2^N where FSR=full scale range and N=12. Nonideal quantization bands represent differential non linearity errors (See figures 5, 6 and 7).

Figure 5 - Static Input Conditions



RESOLUTION - ACTUAL vs AVAILABLE

The available resolution of an N-bit converter is 2^N. This means it is theoretically possible to generate 2^N unique output codes.

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Figure 6 - Dynamic Conditions

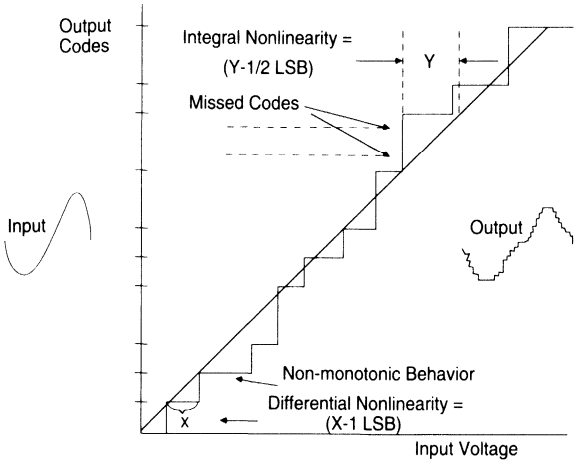
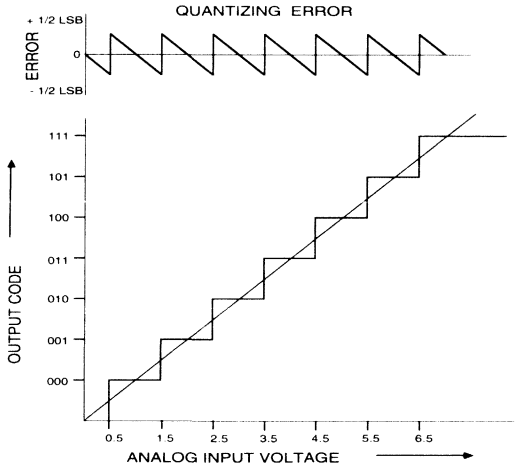


Figure 7 - Quantizing Error



THROUGHPUT

Maximum throughput is the greatest number of conversions per second at which an ADC will deliver its full rate performance. This is equivalent to the inverse of the sum of the multiplex time (if applicable), the S/H settling time and the conversion time.

GAIN

The slope of the transfer curve. Gain is generally user adjustable to compensate for long term drift.

ACQUISITION TIME/APERTURE DELAY TIME

In the HADC574Z, this is the time delay between the R/$\overline{C}$ falling edge and the actual start of the HOLD mode in a sample and HOLD function.

APERTURE JITTER

A specification indicating how much the aperture delay time varies between samples.

SUCCESSIVE APPROXIMATION ADC

The successive approximation converter uses an architecture with inherently high throughput rates which converts high frequency signals with great accuracy. A sample and hold type circuit can be used on the input to freeze these signals during conversion.

A N-bit successive approximation converter performs a sequence of tests comparing the input voltage to a successively narrower voltage range. The first range is half full scale, the next is quarter full scale, etc., until it reaches the Nth test which narrows it to a range of $1/2^N$ of full scale. The conversion time is fixed by the clock frequency and is thus independent of the input voltage.

UNIPOLAR OFFSET

The first transition should occur at a level 1/2 LSB above analog common. Unipolar offset is defined as the deviation of the actual transition from that point. This offset can be adjusted as discussed on the following pages. The unipolar offset temperature co-efficient specifies the maximum change of the transition point over temperature, with and without external adjustment.

BIPOLAR OFFSET

In the bipolar mode, the major carry transition (0111 1111 1111 to 1000 0000 0000) should occur for an analog value 1/2 LSB below analog common. The bipolar offset error and temperature co-efficient specify the initial deviation and maximum change in the error over temperature.

CONVERSION TIME

The time required to complete a conversion over the specified operating range. Conversion time can be expressed as time/bit for a converter with selectable resolution or as time/conversion when the number of bits is constant. The HADC574Z is specified as time/conversion for all 12-bits. Conversion time should not be confused with maximum allowable analog input frequency which is discussed later.

FULL SCALE CALIBRATION ERROR

The last transition (from 1111 1111 1110 to 1111 1111 1111 1111) should occur for an analog value 1 and 1/2 LSB below the nominal full scale (9.9963 Volts for 10.000 Volts full scale). The full scale calibration error is the deviation of the actual level at the last transition from the ideal level. This error, which typically is 0.05 to 0.1% of full scale, can be trimmed out as show in Figure 11 and 12 on page 17. The full scale calibration error over temperature is given with and without the initial error trimmed out. The temperature coefficients for each grade indicate the maximum change in the full scale gain from the initial value using the internal 10 Volt reference.

TEMPERATURE COEFFICIENTS

The temperature coefficients for full scale calibration, unipolar offset, and bipolar offset specify the maximum change from the initial (25 °C) value to the value at Tmin or Tmax.

POWER SUPPLY REJECTION

The standard specifications for the HADC574Z assume +5.00 and +15.00 or +12.00 Volt supplies. The only effect of power supply error on the performance of the device will be a small change in the full scale calibration. This will result in a linear change in all lower order codes. The specifications show the maximum change in calibration from the initial value with the supplies at the various limits.

CODE WIDTH

The fundamental unit for A/D converter specifications is the code width. This is defined as the range of analog input values for which a given digital output code will occur. The nominal value of a code width is equivalent to 1 least significant bit (LSB) of the full scale range or 2.44 mV out of 10 Volts for a 12-bit ADC.

LEFT-JUSTIFIED DATA

The data format used in the HADC574Z is left-justified. This means that the data represents the analog input as fraction of full scale, ranging from 0 to 4095/4096. This implies a binary point to the left of the MSB.

MONOTONICITY

This characteristic describes an aspect of the code to code progression from minimum to maximum input. A device is said to be monotonic if the output code continuously increases as the input signal increases, and if the output code continuously decreases as the input signal decreases. Figure 6 demonstrates non-monotonic behavior.

CIRCUIT OPERATION

The HADC574Z is a complete 12-bit analog-to-digital converter which consists of a single chip version of the industry standard 574. This single chip contains a precision 12-bit capacitor digital-to-analog converter (CDAC) with voltage reference, comparator, successive approximation register (SAR), sample and hold, clock, output buffers and control circuitry to make possible to use the HADC574Z with few external components.

When the control section of the HADC574Z initiates a conversion command, the clock is enabled and the successive-approximation register is reset to all zeros. Once the conversion cycle begins, it can not be stopped or re-started and data is not available from the output buffers.

The SAR, timed by the clock, sequences through the conversion cycle and returns an end-of-convert flag to the control section of the ADC. The clock is then disabled by the control section, the output status goes low, and the control section is enabled to allow the data to be read by external command.

The internal HADC574Z 12-bit CDAC is sequenced by the SAR starting from the MSB to the LSB at the beginning of the conversion cycle to provide an output voltage from the CDAC that is equal to the input signal voltage (which is divided by the input voltage divider network). The comparator determines whether the addition of each successively-weighted bit voltage causes the CDAC output voltage summation to greater or less than the input voltage; it the sum is less, the bit is left on; if more, the bit is turned off. After testing all the bits, the SAR contains a 12-bit binary code which accurately represents the input signal to within ±1/2 LSB.

The internal reference provides the voltage reference to the CDAC with excellent stability over temperature and time. The reference is trimmed to 10.00 Volts ±1% and can supply up to 2 mA to an external load in addition to that required to drive the reference input resistor (1 mA) and offset resistor (1 mA) when operating with ±15 V supplies. If the HADC574Z is used with ±12 V supplies, or if external current must be supplied over the full temperature range, and external buffer amplifier is recommended. Any external load on the HADC574Z reference must remain constant during conversion.

The sample and hold feature is a bonus of the CDAC architecture. Therefore the majority of the S/H specifications are included within the A/D specifications.

Although the sample and hold circuit is not implemented in the classical sense, the sampling nature of the capacitive DAC makes the HADC574Z appear to have a built in sample and hold. This sample and hold action substantially increases the signal bandwidth of the HADC574Z over that of similar competing devices.

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Note that even though the user may use an external sample and hold for very high frequency inputs, the internal sample and hold still provides a very useful isolation function. Once the internal sample is taken by the CDAC capacitance, the input of the HADC574Z is disconnected from the user's sample and hold. This prevents transients occurring during conversion from being inflicted upon the attached sample and hold buffer. All other 574 circuits will cause a transient load current on the sample and hold which will upset the buffer output and may add error to the conversion itself.

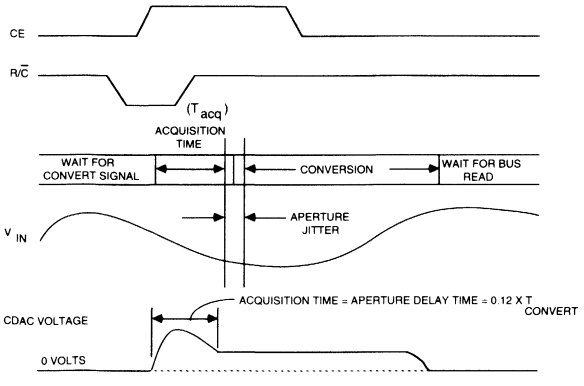
Furthermore, the isolation of the input after the acquisition time in the HADC574Z allows the user an opportunity to release the hold on an external sample and hold and start it tracking the next sample. This will increase system throughput with the user's existing components.

SAMPLE AND HOLD FUNCTION

When using an external S/H, the HADC574Z acts as any other 574 device because the internal S/H is transparent. The sample/hold function in the HADC574Z is inherent to the capacitor DAC structure, and its timing characteristics are determined by the internally generated clock. However, for limited frequency ranges, the internal S/H may eliminate the need for an external S/H. This function will be explained in the next two sections.

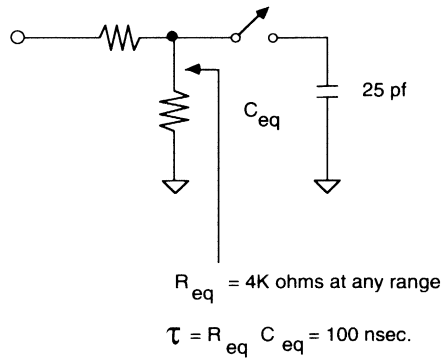
The operation of the S/H function is internal to the HADC574Z and is controlled through the normal R/$\overline{C}$ control line (refer to Figure 8). When the R/$\overline{C}$ line makes a negative transition, the HADC574Z starts the timing of the sampling and conversion. The first 2 clock cycles are allocated to signal acquisition of the input by the CDAC (this time is defined as T_{acq}). Following these two cycles, the input sample is taken and held. The A/D conversion follows this cycle with the duration controlled by the internal clock cycle.

Figure 8 - Sample and Hold Function



During T_{acq}, the equivalent circuit of the HADC574Z input is as shown in Figure 9 (the time constant of the input is independent of which input level is used). This CDAC capacitance must be charged up to the input voltage during T_{acq}. Since the CDAC time constant is 100 nsecs, there is more than enough time for settling the input to 12-bits of accuracy during T_{acq}. The excess time left during T_{acq} allows the user's buffer amp to settle after being switched to the CDAC load.

Figure 9 - Equivalent HADC574Z Input Circuit



Note that because the sample is taken relative to the R/$\overline{C}$ transition, Tacq is also the traditional "aperture delay" of this internal sample and hold.

Since T_{acq} is measured in clock cycles, its duration will vary with the internal clock frequency. This results in T_{acq} =2.4 µsec between units and over temperature.

Offset, gain and linearity errors of the S/H circuit, as well as the effects of its droop rate, are included in the overall specs for the HADC574Z.

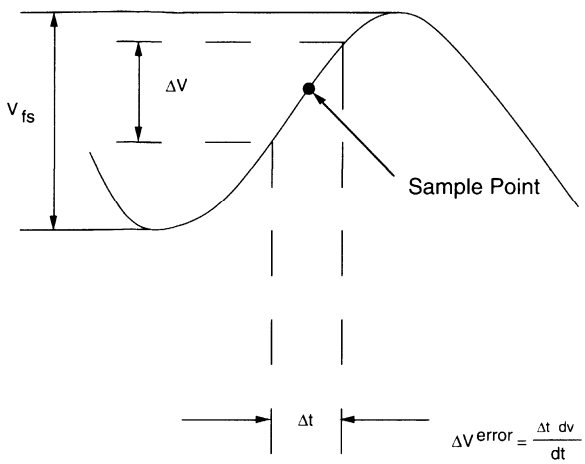
APERTURE UNCERTAINTY

Often the limiting factor in the application of the sample and hold is the uncertainty in the time that the actual sample is taken i.e. the "aperture jitter' or T_{AJ}. The HADC574Z has a nominal aperture jitter of 8 nsecs between samples. With this jitter, it is possible to accurately sample a wide range of input signals.

The aperture jitter causes an amplitude uncertainty for any input where the voltage is changing. The approximate voltage error due to aperture jitter depends on the slew rate of the signal at the sample point (see Figure 10). The magnitude of this change for a sine wave can be calculated:

$Verr \leq V_{fs}/2^{N+1}$ (where Verr is the allowable error voltage and Vfs is the full scale voltage)

Figure 10 - Aperture Uncertainty



From Figure 10:

$Sr=\Delta V/\Delta T=2\ \pi fVp$

Let $\Delta V=Verr=V_{fs}2^{-(N+1)}$, $Vp=Vin/2$ and $\Delta T=t_{AJ}$ (The time during which unwanted voltage change occurs)

The above conditions then yield:

$V_{fs}/2^{N+1} \geq \pi fVin\ t_{AJ}$ or $f_{max} \leq V_{fs}/(\pi Vin\ t_{AJ})2N+1$

For the HADC574Z, T_{AJ}=8 nsec, therefore $f_{max} \leq 5$ kHz.

For higher frequency signal inputs, an external sample and hold is recommended.

TYPICAL INTERFACE CIRCUIT

The HADC574Z is a complete A/D converter that is fully operational when powered up and issued a Start Convert Signal. Only a few external components are necessary as shown in Figure 11 and 12. The two typical interface circuits are for operating the HADC574Z in either an unipolar or bipolar input mode. Further information is given in the following sections on these connections, but first a few conditions concerning board layout to achieve the best operation.

For each application of this device, strict attention must be given to power supply decoupling, board layout (to reduce pickup between analog and digital sections), and grounding. Digital timing, calibration and the analog signal source must be considered for correct operation.

To achieve specified accuracy, a double-sided printed circuit board with a copper ground plane on the component side is recommended. Keep analog signal traces away from digital lines. It is best to lay the PC board out such that there is an analog section and a digital section with a single point ground connection between the two through an RF bead located as close to the device as possible. If possible, run analog signals between ground traces and cross digital lines at right angles only.

POWER SUPPLIES

The supply voltages for the HADC574Z must be kept as quiet as possible from noise pickup and also regulated from transients or drops. Because the part has 12-bit accuracy, voltage spikes on the supply lines can cause several LSB deviations on the output. Switching power supply noise can be a problem. Careful filtering and shielding should be employed to prevent the noise from being pickup by the converter.

Capacitor bypass pairs are needed from each supply pin to it's respective ground to filter noise and counter the problems caused by the variations in supply current. A 10 µF tantalum and a 0.1 µF ceramic type in parallel between V_{LOGIC} (pin 1) and digital common (pin 15), and V_{CC} (pin 7) and analog common (pin 9) is sufficient. V_{EE} is generated internally so pin 11 may be grounded or connected to a negative supply if the HADC574Z is being used to upgrade an already existing design.

GROUNDING CONSIDERATIONS

Any ground path from the analog and digital ground should be as low resistance as possible to accommodate the ground currents present with this device.

The analog ground current is approximately 6 mADC while the digital ground is 3 mADC The analog and digital common pins should be tied together as close to the package as possible to guarantee best performance. The code dependent currents flow through the V_{LOGIC} and V_{CC} terminals and not through the analog and digital common pins.

The HADC574Z may be operated by a µP or in the stand-alone mode. The part has four standard input ranges: 0 V to +10 V, 0 V to +20 V, ±5 V and ±10 V The maximum errors that are listed in the specifications for gain and offset may be adjusted externally to zero as explained in the next two sections.

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CALIBRATION AND CONNECTION PROCEDURES

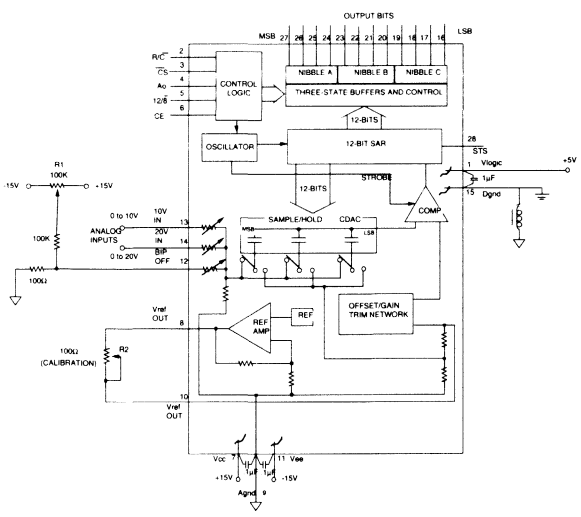
UNIPOLAR

The calibration procedure consists of adjusting the converter's most negative output to its ideal value for offset adjustment, and then adjusting the most positive output to its ideal value for gain adjustment.

Starting with offset adjustment and referring to Figure 11, the midpoint of the first LSB increment should be positioned at the origin to get an output code of all 0s. To do this, an input of +1/2 LSB or +1.22 mV for the 10 V range and +2.44 mV for the 20 V range should be applied to the HADC574Z. Adjust the offset potentiometer R1 for code transition flickers between 0000 0000 0000 and 0000 0000 0001.

The gain adjustment should be done at positive full scale. The ideal input corresponding to the last code change is applied. This is 1 and 1/2 LSB below the nominal full scale which is +9.9963 V for the 10 V range and +19.9927 V for the 20 V range. Adjust the gain potentiometer R2 for flicker between codes 1111 1111 1110 and 1111 1111 1111. If calibration is not necessary for the intended application, replace R2 with a 50 Ω, 1% metal film resister and remove the network from pin 12. Connect pin 12 to pin 9. Connect the analog input to pin 13 for the 0 V to 10 V range or to pin 14 for the 0 V to 20 V range.

Figure 11 - Unipolar Input Connections



BIPOLAR

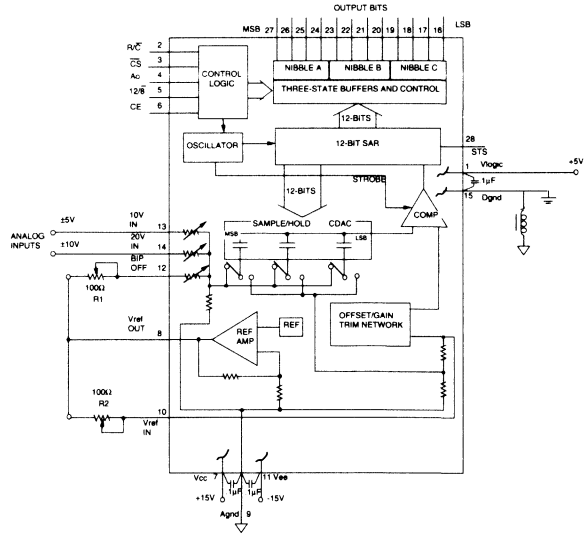
The gain and offset errors listed in the specification may be adjusted to zero using the potentiometers R1 and R2 (See Figure 12). If adjustment is not needed, either or both pots may be replaced by a 50 Ω, 1% metal film resistor.

To calibrate, connect the analog input signal to pin 13 for a ±5 V range or to pin 14 for a ±10 V range. First apply a DC input voltage 1/2 LSB above negative full scale which is -4.9988 V for the ±5 V range or -9.9976 V for the ±10 V range. Adjust the offset potentiometer R1 for flicker between output codes 0000 0000 0000 and 0000 0000 0001. Next, apply a DC input voltage 1 and 1/2 LSB below positive full scale which is +4.9963 V for the ±5 V range or +9.9927 V for the ±10 V range. Adjust the gain potentiometer R2 for flicker between codes 1111 1111 1110 and 1111 1111 1111.

ALTERNATIVE

In some applications, a full scale of 10.24 V (for an LSB of 2.5 mV) or 20.48 V (for an LSB of 5.0 mV) is more convenient. In the Unipolar mode of operation, replace R2 by 200 Ω potentiometer and add 150 Ω in series with pin 13 for 10.24 V input range or 500 Ω in series with pin 14 for 20.48 V input range. In bipolar mode of operation, replace R1 by 500 Ω potentiometer (in addition to the previous changes). The calibration will remain similar to the standard calibration procedure.

Figure 12 - Bipolar Input Connections



CONTROLLING THE HADC574Z

The HADC574Z can be operated by most microprocessor systems due to the control input pins and on-chip logic. It may also be operated in the "stand-alone" mode and enabled by the R/$\overline{C}$ input pin. Full µP control consists of selecting an 8 or 12-bit conversion cycle, initiating the conversion, and reading the output data when ready. The output read has the options of choosing either 12-bits at once or 8 following by 4-bits in a left-justified format. All five control inputs are TTL/CMOS compatible and include 12/$\overline{8}$, $\overline{CS}$, Ao, R/$\overline{C}$ and CE. The use of these inputs in controlling the converter's operations is shown in Table I, and the internal control logic is shown in a simplified schematic in Figure 14.

STAND-ALONE OPERATION

The simplest interface is a control line connected to R/$\overline{C}$. The other controls must be tied to known states as follows: CE and 12/$\overline{8}$ are wired high, Ao and $\overline{CS}$ are wired low. The output controls must be tied to known states as follows: CE and 12/$\overline{8}$ are wired high, Ao and $\overline{CS}$ are wired low. The output data arrives in words of 12-bits each. The limits on R/$\overline{C}$ duty cycle are shown in Figures 3 and 4. It may have a duty cycle within and including the extremes shown in the specifications on the pages. In general, data may be read when R/$\overline{C}$ is high unless STS is also high, indicating a conversion is in progress.

Figure 13 - Interfacing the HADC574Z to an 8-bit Data Bus

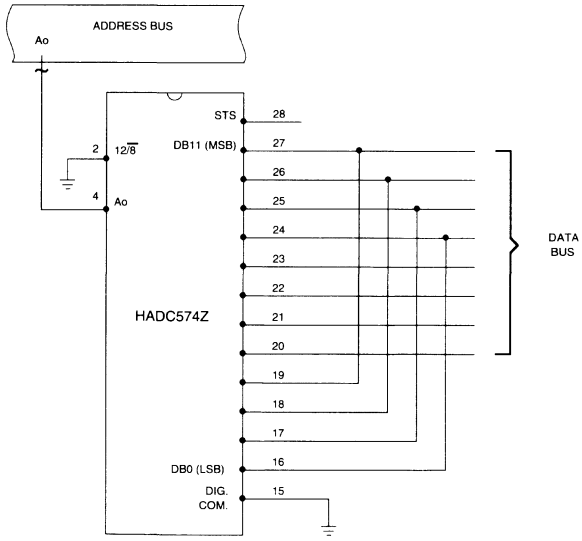


Table I - Truth Table for the HADC574Z Control Inputs

CE	$\overline{CS}$	R/$\overline{C}$	12/$\overline{8}$	Ao	Operation
0	X	X	X	X	None
X	1	X	X	X	None
↑	0	0	X	0	Initiate 12 bit conversion
↑	0	0	X	1	Initiate 8 bit conversion
1	↓	0	X	0	Initiate 12 bit conversion
1	↓	0	X	1	Initiate 8 bit conversion
1	0	↓	X	0	Initiate 12 bit conversion
1	0	↓	X	1	Initiate 8 bit conversion
1	0	1	1	X	Enable 12 bit Output
1	0	1	0	0	Enable 8 MSB's Only
1	0	1	0	1	Enable 4 LSB's Plus 4 Trailing Zeroes

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CONVERSION LENGTH

A conversion start transition latches the state of Ao as shown in Figure 13 and Table I. The latched state determines if the conversion stops with 8-bit (Ao high) or continues for 12-bits (Ao low). If all 12-bits are read following an 8-bit conversion, the three LSB's will be a logic "0" and DB3 will be a logic "1". Ao is latched because it is also involved in enabling the output buffers as will be explained later. No other control inputs are latched.

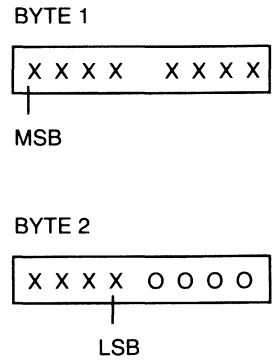
CONVERSION START

A conversion may be initiated by a logic transition on any of the three inputs: CE, $\overline{CS}$, R/$\overline{C}$, as shown in Table I. The last of the three to reach the correct state starts the conversions, so one, two or all three may be dynamically controlled. The nominal delay from each is the same and all three may change state simultaneously. In order to assure that a particular input controls the start of conversion, the other two should be setup at least 50 ns earlier. Refer to the convert mode timing specifications. The Convert Start timing diagram is illustrated in Figure 1.

The output signal STS is the status flag and goes high only when a conversion is in progress. While STS is high, the output buffers remain in a high impedance state so that data can not be read. Also, when STS is high, an additional Start Convert will not reset the converter or reinitiate a conversion. Note, if Ao changes state after a conversion begins, an additional Start Convert command will latch the new start of Ao and possible cause a wrong cycle length for that conversion (8 versus 12-bits).

READING THE OUTPUT DATA

The output data buffers remain in a high impedance state until the following four conditions are met: R/$\overline{C}$ is high, STS is low, CE is high, and $\overline{CS}$ is low. That data lines become active in response to the four conditions and output data according to the conditions of 12/$\overline{8}$ and Ao. The timing diagram for this process is shown in Figure 2. When 12/$\overline{8}$ is high, all 12 data outputs become active simultaneously and the Ao input is ignored. This is for easy interface to a 12 or 16-bit data bus. The 12/$\overline{8}$ input is usually tied high or low, although it is TTL/CMOS compatible. When 12/$\overline{8}$ is low, the output is separated into two 8-bit bytes as shown below:



This configuration makes it easy to connect to an 8-bit data bus as shown in Figure 13. The Ao control can be connected to the least significant bit of the address bus in order to store the output data into two consecutive memory locations. When Ao is pulled low, the 8 MSBs are enabled only. When Ao is high, the 4 MSBs are disabled, bits 4 through 7 are forced to a zero and the four LSBs are enabled. The two byte format is "left justified data" as shown above and can be considered to have a decimal point or binary to the left of byte 1.

Ao may be toggled without damage to the converter at any time. Break-before-make action is guaranteed between the two data bytes. This assures that the outputs which are strapped together in Figure 13 will never be enabled at the same time.

In Figure 2, it can be seen that a read operation usually begins after the conversion is completed and STS is low. If earlier access is needed, the read can begin no later than the addition of time t_{DD} and t_{HS} before STS goes low.

LEADERSHIP IN DATA CONVERSION AND SIGNAL PROCESSING

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SIGNAL PROCESSING TECHNOLOGIES

HADC674Z

FAST, COMPLETE 12-BIT μP COMPATIBLE A/D CONVERTER WITH SAMPLE/HOLD

3

FEATURES

- Improved Pin-To-Pin Compatible Monolithic Version of the HI674A
- Complete 12-Bit A/D Converter with Sample/Hold, Reference and Clock
- Low Power Dissipation (150 mW Max)
- 12-Bit Linearity (Over Temp)
- 15 μs Max Conversion Time
- No Negative Supply Required
- Full Bipolar and Unipolar Input Range

APPLICATIONS

- Military/Industrial Data Acquisition Systems
- 8 or 12-Bit μP Input Functions
- Process Control Systems
- Test and Scientific Instruments
- Personal Computer Interface

GENERAL DESCRIPTION

The HADC674Z is a complete, 12-bit successive approximation A/D converter. The device is integrated on a *single die* to make it the first monolithic CMOS version of the industry standard device, HI674A. Included on chip is an internal reference, clock, and a sample and hold. The S/H is an additional feature not available on similar devices.

The HADC674Z features 15 μs (Max) conversion time of 10 or 20 Volt input signals. Also, a three-state output buffer is added for direct interface to an 8, 12, or 16-bit μP bus.

The HADC674Z is manufactured on a Bipolar Enhanced CMOS process (BEMOS) which combines CMOS logic and fast bipolar npn transistors to yield high performance digital and analog functions on one chip.

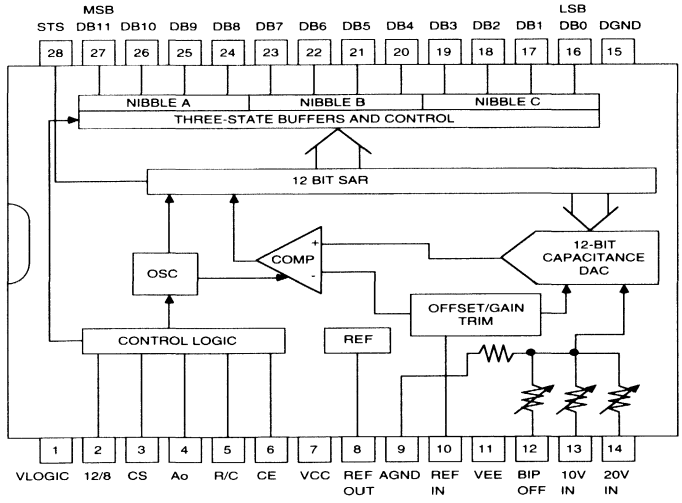
The BEMOS process and monolithic construction reduces power consumption, ground noise, and keeps parasitics to a minimum. In addition, the thin film option on this process allows active adjustment of DAC and comparator offsets, linearity errors, and gain errors.

The HADC674Z has standard bipolar and unipolar input ranges of 10 V and 20 V that are controlled by a bipolar offset pin and laser trimmed for specified linearity, gain and offset accuracy.

Power requirements are +5 V and +12 V to +15 V with a maximum dissipation of 150 mW at the specified voltages. Power consumption is about five times lower than currently available devices, and a negative power supply is not needed.

A standard military drawing is published under DESC number 5962-91690.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATING (Beyond which damage may occur) [1] 25 °C

Supply Voltages

Positive Supply Voltage (V_{CC} to DGND) .....0 to +16.5 V
Logic Supply Voltage (V_{LOGIC} to DGND) .....0 to +7 V
Analog to Digital Ground (AGND to DGND) .-0.5 to +1 V

Input Voltages

Control Input Voltages (to DGND)
(CE, CS, Ao, 12/8, R/C) .....-0.5 to V_{LOGIC} +0.5 V
Analog Input Voltage (to AGND)
(REF IN, BIP OFF, 10 Vin) .....±16.5 V
20 V Vin Input Voltage (to AGND) .....±24 V

Output

Reference Output Voltage .....Indefinite short to GND
Momentary short to V_{CC}

Temperature

Operating Temperature, ambient .....-55 to +125 °C
junction .....+175 °C
Lead Temperature, (soldering 10 seconds).....+300 °C
Storage Temperature .....-65 to +150 °C
Power Dissipation .....1000 mW
Thermal Resistance (θ_{JA}) .....48 °C/W

Note: Operation at any Absolute Maximum Rating is not implied. See Operating Conditions for proper nominal applied conditions in typical applications.

ELECTRICAL SPECIFICATIONS

$T_A=T_{MIN}$ to T_{MAX}, V_{CC}=+15 V or +12 V, V_{LOGIC}=+5 V, unless otherwise specified.

PARAMETER	TEST CONDITIONS	TEST LEVEL	HADC674ZC MIN	HADC674ZC TYP	HADC674ZC MAX	HADC674ZB MIN	HADC674ZB TYP	HADC674ZB MAX	HADC674ZA MIN	HADC674ZA TYP	HADC674ZA MAX	UNITS
DC ELECTRICAL CHARACTERISTICS												
Resolution		VI			12			12			12	BITS
Linearity Error[1]	T_A=0 to 70 °C	VI			±1			±1/2			±1/2	LSB
	T_A = -25 to +85 °C	I			±1			±1/2			±1/2	LSB
	T_A = -55 to +125 °C	I			±1			±1			±1	LSB
Differential Linearity	No Missing Codes	VI	11			12			12			BITS
Unipolar Offset; 10 V, 20 V	+25 °C Adjustable to Zero	VI		±0.1	±2		±0.1	±2		±0.1	±2	LSB
Bipolar Offset1; ±5 V,±10 V	+25 °C Adjustable to Zero	VI			±10			±4			±4	LSB
Full Scale Calibration Error[2] All Input Ranges	+25 °C Adjustable to Zero	VI			0.3			0.3			0.3	% of FS
	No Adjustment at +25°											
	T_A = 0 to 70 °C	V		0.5			0.4			0.35		%of FS
	T_A = -25 to +85 °C	V		0.7			0.5			0.4		%of FS
	T_A = -55 to +125 °C	V		0.8			0.6			0.4		%of FS
	With Adjustment at +25 °C											
	T_A = 0 to 70 °C	V		0.22			0.12			0.05		%of FS
	T_A = -25 to +85 °C	V		0.4			0.2			0.1		%of FS
	T_A = -55 to +125 °C	V		0.5			0.25			0.12		%of FS
Temperature Coefficients[3]	Using Internal Reference											
Unipolar Offset	T_A = 0 to 70 °C	IV		±0.2	±2		±0.1	±1		±0.1	±1	LSB
					(10)			(5)			(5)	(ppm/°C)
	T_A = -25 to +85 °C	IV			±2			±1			±1	LSB
					(5)			(2.5)			(2.5)	(ppm/°C)
	T_A = -55 to +125 °C	IV			±2			±1			±1	LSB
					(5)			(2.5)			(2.5)	(ppm/°C)
Bipolar Offset	T_A = 0 to 70 °C	IV		±0.2	±2		±0.1	±1		±0.1	±1	LSB
					(10)			(5)			(5)	(ppm/°C)
	T_A = -25 to +85 °C	IV			±2			±1			±1	LSB
					(5)			(2.5)			(2.5)	(ppm/°C)

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ELECTRICAL SPECIFICATIONS

$T_A = T_{MIN}$ to T_{MAX}, V_{CC} = +15 V or +12 V, V_{LOGIC} = +5 V, unless otherwise specified.

PARAMETER	TEST CONDITIONS	TEST LEVEL	HADC674ZC MIN	HADC674ZC TYP	HADC674ZC MAX	HADC674ZB MIN	HADC674ZB TYP	HADC674ZB MAX	HADC674ZA MIN	HADC674ZA TYP	HADC674ZA MAX	UNITS
DC ELECTRICAL CHARACTERISTICS												
Bipolar Offset (Cont.)	T_A = -55 to +125 °C	IV			±4 (10)			±2 (5)			±1 (2.5)	LSB (ppm/°C)
Full Scale Calibration	T_A = 0 to 70 °C	IV			±9 (45)			±5 (25)			±2 (10)	LSB (ppm/°C)
	T_A = -25 to +85 °C	IV			±12 (50)			±7 (25)			±3 (12)	LSB (ppm/°C)
	T_A = -55 to +125 °C	IV			±20 (50)			±10 (25)			±5 (12.5)	LSB (ppm/°C)
Power Supply Rejection	Max change in full scale calibration											
+13.5 V<V_{CC}<+16.5 V or +11.4 V<V_{CC}<+12.6 V		VI		±0.5	±2		±0.5	±1		±0.5	±1	LSB
+4.5 V<V_{LOGIC}<+5.5 V		VI		±0.1	±0.5		±0.1	±0.5		±0.1	±0.5	LSB
Analog Input Ranges												
Bipolar		VI	-5		+5	-5		+5	-5		+5	Volts
			-10		+10	-10		+10	-10		+10	Volts
Unipolar		VI	0		+10	0		+10	0		+10	Volts
			0		+20	0		+20	0		+20	Volts
Input Impedance												
10 Volt Span		VI	3.75	5	6.25	3.75	5	6.25	3.75	5	6.25	kΩ
20 Volt Span			15	20	25	15	20	25	15	20	25	kΩ
Power Supplies Operating Voltage Range												
V_{LOGIC}		VI	+4.5		+5.5	+4.5		+5.5	+4.5		+5.5	Volts
V_{CC}		VI	+11.4		+16.5	+11.4		+16.5	+11.4		+16.5	Volts
V_{EE}	Not Required for circuit operation.											
Operating Current												
I_{LOGIC}		VI		0.5	1		0.5	1		0.5	1	mA
I_{CC}		VI		7	9		7	9		7	9	mA
I_{EE}	Not required for circuit operation.											
Power Dissipation +15 V, +5 V		VI		110	150		110	150		110	150	mW
Internal Reference Voltage		VI	9.97	10	10.03	9.97	10	10.03	9.97	10	10.03	Volts
Output Current[4]		VI			2			2			2	mA

ELECTRICAL SPECIFICATIONS

$T_A = T_{MIN}$ to T_{MAX}, V_{CC} = +15 V or +12 V, V_{LOGIC} = +5 V, unless otherwise specified.

PARAMETER	TEST CONDITIONS	TEST LEVEL	HADC674ZC MIN	HADC674ZC TYP	HADC674ZC MAX	HADC674ZB MIN	HADC674ZB TYP	HADC674ZB MAX	HADC674ZA MIN	HADC674ZA TYP	HADC674ZA MAX	UNITS
DIGITAL CHARACTERISTICS												
Logic Inputs (CE, $\overline{CS}$, R/$\overline{C}$, Ao, 12/$\overline{8}$)												
Logic "0"		VI	-0.5		+0.8	-0.5		+0.8	-0.5		+0.8	Volts
Logic "1"		VI	2.0		5.5	2.0		5.5	2.0		5.5	Volts
Current	0 to 5.5 V Input	VI		±.01	+1		±.01	+1		±.01	+1	µA
Capacitance		V		5			5			5		pF
Logic Outputs (DB11-DB0, STS)												
Logic "0"	(I_{Sink} = 1.6 mA)	VI			+0.4			+0.4			+0.4	Volts
Logic "1"	(I_{SOURCE} = 500 µA)	VI	+2.4			+2.4			+2.4			Volts
Leakage	(High Z State, DB11-DB0 Only)	VI	-5	±0.1	+5	-5	±0.1	+5	-5	±0.1	+5	µA
Capacitance		V		5			5			5		pF

Note 1: For military temperature range, the device linearity is guaranteed to be 1/2 LSB at 25 °C.
Note 2: Fixed 50 Ω resistor from REF OUT to REF IN and REF OUT to BIP OFF.
Note 3: Full Tempco testing is performed on all Grade A and MIL-STD-883 devices.
Note 4: Available for external loads, external load should not change during conversion. When supplying an external load and operating on a +12.0 V supply, a buffer amplifier must be provided for the reference output.

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ELECTRICAL SPECIFICATIONS

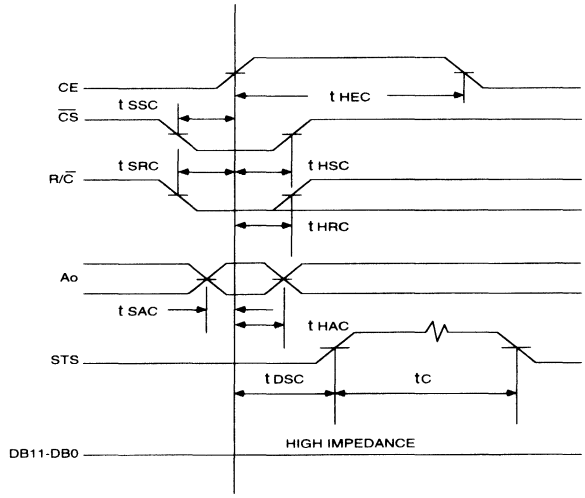
CONVERT MODE TIMING CHARACTERISTICS

T_A = +25 °C, V_{CC} = +15.0 V or +12 V, V_{LOGIC} = +5 V, unless otherwise specified.

PARAMETER	TEST CONDITIONS	TEST LEVEL	HADC674ZC MIN	HADC674ZC TYP	HADC674ZC MAX	HADC674ZB MIN	HADC674ZB TYP	HADC674ZB MAX	HADC674ZA MIN	HADC674ZA TYP	HADC674ZA MAX	UNITS
AC ELECTRICAL CHARACTERISTICS[1]												
t_{DSC} STS Delay from CE		I			200			200			200	ns
t_{HEC} CE Pulse Width		I	50			50			50			ns
t_{SSC} $\overline{CS}$ to CE Setup		I	50			50			50			ns
t_{HSC} $\overline{CS}$ Low during CE High		I	50			50			50			ns
t_{SRC} R/$\overline{C}$ to CE Setup		I	50			50			50			ns
t_{HRC} R/$\overline{C}$ Low During CE High		I	50			50			50			ns
t_{SAC} Ao to CE Setup		I	0			0			0			ns
t_{HAC} Ao Valid During CE High		I	50			50			50			ns
t_C Conversion Time												
12-Bit Cycle	T_{MIN} to T_{MAX}	I	9	13	15	9	13	15	9	13	15	µs
8-Bit Cycle	T_{MIN} to T_{MAX}	I	6	8	10	6	8	10	6	8	10	µs

Note 1: Time is measured from 50% level of digital transitions. Tested with a 100 pF and 3 kΩ load for high impedance to drive and tested with 10 pF and 3 kΩ load for drive to high impedance.

Figure 1 - Convert Mode Timing Diagram



ELECTRICAL SPECIFICATIONS

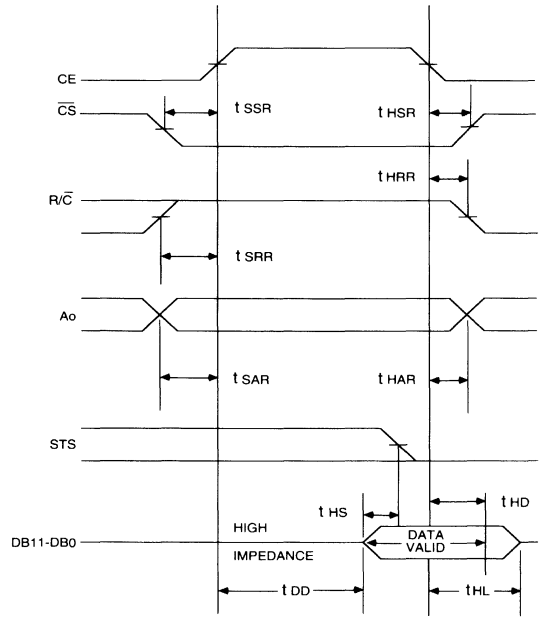
READ MODE TIMING CHARACTERISTICS

T_A = 25 °C, V_{CC} = +15.0 V or +12 V, V_{LOGIC} = +5 V, unless otherwise specified.

PARAMETER	TEST CONDITIONS	TEST LEVEL	HADC674ZC MIN	HADC674ZC TYP	HADC674ZC MAX	HADC674ZB MIN	HADC674ZB TYP	HADC674ZB MAX	HADC674ZA MIN	HADC674ZA TYP	HADC674ZA MAX	UNITS
AC ELECTRICAL CHARACTERISTICS[1]												
t_{DD} Access Time from CE		I			150			150			150	ns
t_{HD} Data Valid After CE Low		I	25			25			25			ns
t_{HL} Output Float Delay		I			150			150			150	ns
t_{SSR} $\overline{CS}$ to CE Setup		I	50	0		50	0		50	0		ns
t_{SRR} R/$\overline{C}$ to CE Setup		I	0	0		0	0		0	0		ns
t_{SAR} Ao to CE Setup		I	50			50			50			ns
t_{HSR} $\overline{CS}$ Valid After CE Low		I	0	0		0	0		0	0		ns
t_{HRR} R/$\overline{C}$ High After CE Low		I	50			50			50			ns
t_{HS} STS Delay After Data Valid		I	100		600	100		600	100		600	ns
t_{HAR} Ao Valid after CE Low		I	50			50			50			ns

Note 1: Time is measured from 50% level of digital transitions. Tested with a 100 pF and 3 kΩ load for high impedance to drive and tested with 10 pF and 3 kΩ load for drive to high impedance.

Figure 2 - Read Mode Timing Diagram



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ELECTRICAL SPECIFICATIONS

STAND-ALONE MODE TIMING CHARACTERISTICS

T_A = 25 °C, V_{CC} = +15.0 V or +12 V, V_{LOGIC} = +5 V, unless otherwise specified.

PARAMETER	TEST CONDITIONS	LEVEL	HADC674ZC MIN	HADC674ZC TYP	HADC674ZC MAX	HADC674ZB MIN	HADC674ZB TYP	HADC674ZB MAX	HADC674ZA MIN	HADC674ZA TYP	HADC674ZA MAX	UNITS
AC ELECTRICAL CHARACTERISTICS												
t_{HRL} Low R/$\overline{C}$ Pulse Width		I	50			50			50			ns
t_{DS} STS Delay from R/$\overline{C}$		I			200			200			200	ns
t_{HDR} Data Valid After R/$\overline{C}$ Low		I	25			25			25			ns
t_{HS} STS Delay After Data Valid		I	100		600	100		600	100		600	ns
t_{HRH} High R/$\overline{C}$ Pulse Width		I	150			150			150			ns
t_{DDR} Data Access Time		I			150			150			150	ns
SAMPLE AND HOLD												
Acquisition Time		IV	1.2	1.7	2.0	1.2	1.7	2.0	1.2	1.7	2.0	µs
Aperture Uncertainty Time		V		8			8			8		ns,RMS

Figure 3 - Low Pulse for R/$\overline{C}$ - Outputs Enabled After Conversion

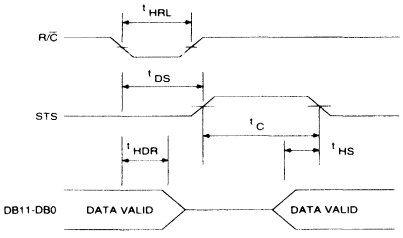
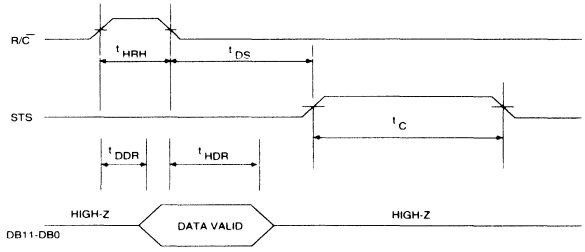


Figure 4 - High Pulse for R/$\overline{C}$ - Outputs Enabled While R/$\overline{C}$ is High, Otherwise High Impedance



TEST LEVEL CODES

All electrical characteristics are subject to the following conditions:

All parameters having min/max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality Assurance inspection. Any blank section in the data column indicates that the specification is not tested at the specified condition.

Unless otherwise noted, all tests are pulsed tests; therefore, $T_J = T_C = T_A$.

TEST LEVEL	TEST PROCEDURE
I	100% production tested at the specified temperature.
II	100% production tested at T_A=25 °C, and sample tested at the specified temperatures.
III	QA sample tested only at the specified temperatures.
IV	Parameter is guaranteed (but not tested) by design and characterization data.
V	Parameter is a typical value for information purposes only.
VI	100% production tested at T_A = 25 °C. Parameter is guaranteed over specified temperature range.

DEFINITION OF SPECIFICATIONS

INTEGRAL LINEARITY ERROR

Linearity error refers to the deviation of each individual code from a line drawn from "zero" through "full scale" with all offset errors nulled out (See Figure 5 and 6). The point used as "zero" occurs 1/2 LSB (1.22 mV for a 10 Volt span) before the first code transition (all zeros to only the LSB "on"). "Full scale" is defined as a level 1 and 1/2 LSB beyond the last code transition (to all ones). The deviation of a code from the true straight line is measured from the middle of each particular code.

The HADC674ZAC and BC grades are guaranteed for maximum nonlinearity of ±1/2 LSB. For these grades, this means that an analog value which falls exactly in the center of a given code width will result in the correct digital output code. Values nearer the upper or lower transition of the code width may produce the next upper or lower digital output code. The HADC674ZAM, BM, CC and CM grades are guaranteed to ±1 LSB maximum error. For these grades, an analog value which falls within a given code width will result in either the correct code for the region or either adjacent one. The linearity is not user-adjustable.

DIFFERENTIAL LINEARITY ERROR (NO MISSING CODES)

A specification which guarantees no missing codes requires that every code combination appear in a monotonically increasing sequence as the analog input level is increased. Thus every code must have a finite width. For the HADC674Z type BC, AC, BM and AM grades, which guarantee no missing codes to 12-bit resolution, all 4096 codes must be present over the entire operating temperature ranges. The HADC674Z CC and CM grades guarantee no missing codes to 11-bit resolution over temperature; this means that all code combinations of the upper 11-bits must be present; in practice, very few of the 12-bit codes are missing.

DIFFERENTIAL NONLINEARITY

Differential nonlinearity is a measure of how much the actual quantization step width varies from the ideal step width of 1 LSB. Figure 6 shows a differential nonlinearity of 2 LSB - the actual step width is 3 LSB. The HADC674Z's specification gives the worst case differential nonlinearity in the A/D transfer function under specified dynamic operating conditions. Small, localized differential nonlinearities may be insignificant when digitizing full scale signals. However, if a low level input signal happens to fall on the part of the A/D transfer function with the differential nonlinearity error, the effect will be significant.

MISSING CODES

Missing codes represent a special kind of differential nonlinearity. The quantization step width for a missing code is 0 LSB, which results in a differential nonlinearity of -1 LSB. Figure 6 points out two missed codes in the transfer function.

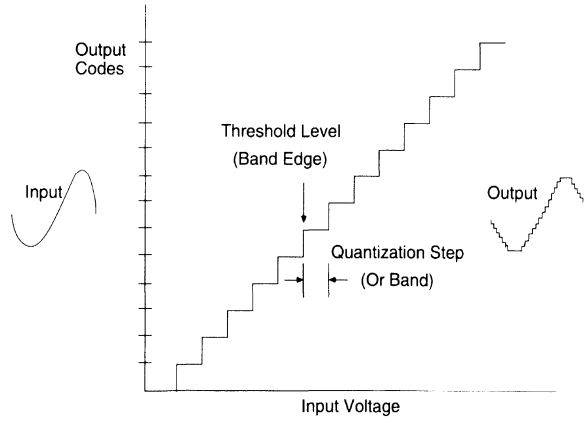
QUANTIZATION UNCERTAINTY

Analog-to-digital converters exhibit an inherent quantization uncertainty of ±1/2 LSB. This uncertainty is a fundamental characteristic of the quantization process and cannot be reduced for a converter of a given resolution.

QUANTIZATION ERROR

Quantization error is the fundamental, irreducible error associated with the perfect quantizing of a continuous (analog) signal into a finite number of digital bits (A/D transfer function). A 12-bit A/D converter can represent an input voltage with a best case uncertainty of 1 part in 2^{12} (1 part in 4096). In real A/Ds under dynamic operating conditions, the quantization bands (bit change step vs input amplitude) for certain codes can be significantly larger (or smaller) than the ideal. The ideal width of each quantization step (or band) is Q=FSR/2^N where FSR=full scale range and N=12. Nonideal quantization bands represent differential non linearity errors (See figures 5, 6 and 7).

Figure 5 - Static Input Conditions



RESOLUTION - ACTUAL vs AVAILABLE

The available resolution of an N-bit converter is 2^N. This means it is theoretically possible to generate 2^N unique output codes.

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Figure 6 - Dynamic Conditions

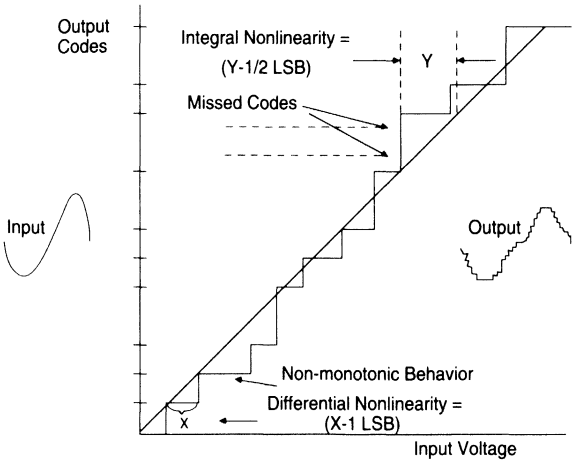
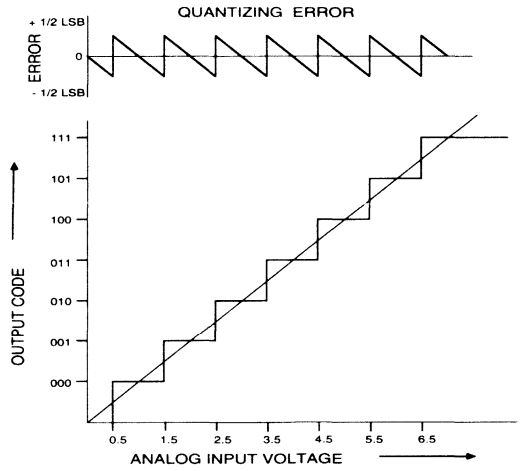


Figure 7 - Quantizing Error



THROUGHPUT

Maximum throughput is the greatest number of conversions per second at which an ADC will deliver its full rate performance. This is equivalent to the inverse of the sum of the multiplex time (if applicable), the S/H settling time and the conversion time.

GAIN

The slope of the transfer curve. Gain is generally user adjustable to compensate for long term drift.

ACQUISITION TIME/APERTURE DELAY TIME

In the HADC674Z, this is the time delay between the R/$\overline{C}$ falling edge and the actual start of the HOLD mode in a sample and HOLD function.

APERTURE JITTER

A specification indicating how much the aperture delay time varies between samples.

SUCCESSIVE APPROXIMATION ADC

The successive approximation converter uses an architecture with inherently high throughput rates which converts high frequency signals with great accuracy. A sample and hold type circuit can be used on the input to freeze these signals during conversion.

A N-bit successive approximation converter performs a sequence of tests comparing the input voltage to a successively narrower voltage range. The first range is half full scale, the next is quarter full scale, etc., until it reaches the Nth test which narrows it to a range of $1/2^N$ of full scale. The conversion time is fixed by the clock frequency and is thus independent of the input voltage.

UNIPOLAR OFFSET

The first transition should occur at a level 1/2 LSB above analog common. Unipolar offset is defined as the deviation of the actual transition from that point. This offset can be adjusted as discussed on the following pages. The unipolar offset temperature co-efficient specifies the maximum change of the transition point over temperature, with and without external adjustment.

BIPOLAR OFFSET

In the bipolar mode, the major carry transition (0111 1111 1111 to 1000 0000 0000) should occur for an analog value 1/2 LSB below analog common. The bipolar offset error and temperature co-efficient specify the initial deviation and maximum change in the error over temperature.

CONVERSION TIME

The time required to complete a conversion over the specified operating range. Conversion time can be expressed as time/bit for a converter with selectable resolution or as time/conversion when the number of bits is constant. The HADC674Z is specified as time/conversion for all 12-bits. Conversion time should not be confused with maximum allowable analog input frequency which is discussed later.

FULL SCALE CALIBRATION ERROR

The last transition (from 1111 1111 1110 to 1111 1111 1111 1111) should occur for an analog value 1 and 1/2 LSB below the nominal full scale (9.9963 Volts for 10.000 Volts full scale). The full scale calibration error is the deviation of the actual level at the last transition from the ideal level. This error, which typically is 0.05 to 0.1% of full scale, can be trimmed out as show in Figure 11 and 12 on page 17. The full scale calibration error over temperature is given with and without the initial error trimmed out. The temperature coefficients for each grade indicate the maximum change in the full scale gain from the initial value using the internal 10 Volt reference.

TEMPERATURE COEFFICIENTS

The temperature coefficients for full scale calibration, unipolar offset, and bipolar offset specify the maximum change from the initial (25 °C) value to the value at Tmin or Tmax.

POWER SUPPLY REJECTION

The standard specifications for the HADC674Z assume +5.00 and +15.00 or +12.00 Volt supplies. The only effect of power supply error on the performance of the device will be a small change in the full scale calibration. This will result in a linear change in all lower order codes. The specifications show the maximum change in calibration from the initial value with the supplies at the various limits.

CODE WIDTH

The fundamental unit for A/D converter specifications is the code width. This is defined as the range of analog input values for which a given digital output code will occur. The nominal value of a code width is equivalent to 1 least significant bit (LSB) of the full scale range or 2.44 mV out of 10 Volts for a 12-bit ADC.

LEFT-JUSTIFIED DATA

The data format used in the HADC674Z is left-justified. This means that the data represents the analog input as fraction of full scale, ranging from 0 to 4095/4096. This implies a binary point to the left of the MSB.

MONOTONICITY

This characteristic describes an aspect of the code to code progression from minimum to maximum input. A device is said to be monotonic if the output code continuously increases as the input signal increases, and if the output code continuously decreases as the input signal decreases. Figure 6 demonstrates non-monotonic behavior.

CIRCUIT OPERATION

The HADC674Z is a complete 12-bit analog-to-digital converter which consists of a single chip version of the industry standard 674. This single chip contains a precision 12-bit capacitor digital-to-analog converter (CDAC) with voltage reference, comparator, successive approximation register (SAR), sample and hold, clock, output buffers and control circuitry to make possible to use the HADC674Z with few external components.

When the control section of the HADC674Z initiates a conversion command, the clock is enabled and the successive-approximation register is reset to all zeros. Once the conversion cycle begins, it can not be stopped or restarted and data is not available from the output buffers.

The SAR, timed by the clock, sequences through the conversion cycle and returns an end-of-convert flag to the control section of the ADC. The clock is then disabled by the control section, the output status goes low, and the control section is enabled to allow the data to be read by external command.

The internal HADC674Z 12-bit CDAC is sequenced by the SAR starting from the MSB to the LSB at the beginning of the conversion cycle to provide an output voltage from the CDAC that is equal to the input signal voltage (which is divided by the input voltage divider network). The comparator determines whether the addition of each successively-weighted bit voltage causes the CDAC output voltage summation to greater or less than the input voltage; it the sum is less, the bit is left on; if more, the bit is turned off. After testing all the bits, the SAR contains a 12-bit binary code which accurately represents the input signal to within ±1/2 LSB.

The internal reference provides the voltage reference to the CDAC with excellent stability over temperature and time. The reference is trimmed to 10.00 Volts ±1% and can supply up to 2 mA to an external load in addition to that required to drive the reference input resistor (1 mA) and offset resistor (1 mA) when operating with ±15 V supplies. If the HADC674Z is used with ±12 V supplies, or if external current must be supplied over the full temperature range, and external buffer amplifier is recommended. Any external load on the HADC674Z reference must remain constant during conversion.

The sample and hold feature is a bonus of the CDAC architecture. Therefore the majority of the S/H specifications are included within the A/D specifications.

Although the sample and hold circuit is not implemented in the classical sense, the sampling nature of the capacitive DAC makes the HADC674Z appear to have a built in sample and hold. This sample and hold action substantially increases the signal bandwidth of the HADC674Z over that of similar competing devices.

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Note that even though the user may use an external sample and hold for very high frequency inputs, the internal sample and hold still provides a very useful isolation function. Once the internal sample is taken by the CDAC capacitance, the input of the HADC674Z is disconnected from the user's sample and hold. This prevents transients occurring during conversion from being inflicted upon the attached sample and hold buffer. All other 674 circuits will cause a transient load current on the sample and hold which will upset the buffer output and may add error to the conversion itself.

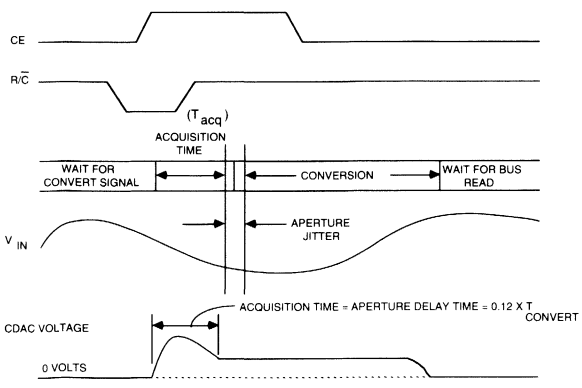
Furthermore, the isolation of the input after the acquisition time in the HADC674Z allows the user an opportunity to release the hold on an external sample and hold and start it tracking the next sample. This will increase system throughput with the user's existing components.

SAMPLE AND HOLD FUNCTION

When using an external S/H, the HADC674Z acts as any other 674 device because the internal S/H is transparent. The sample/hold function in the HADC674Z is inherent to the capacitor DAC structure, and its timing characteristics are determined by the internally generated clock. However, for limited frequency ranges, the internal S/H may eliminate the need for an external S/H. This function will be explained in the next two sections.

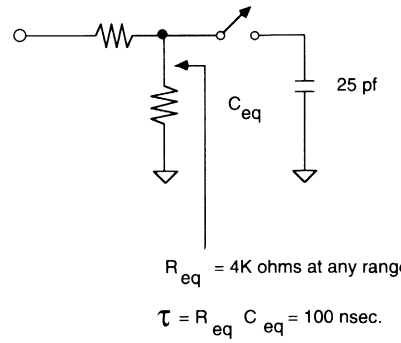
The operation of the S/H function is internal to the HADC674Z and is controlled through the normal R/$\overline{C}$ control line (refer to Figure 8). When the R/$\overline{C}$ line makes a negative transition, the HADC674Z starts the timing of the sampling and conversion. The first 2 clock cycles are allocated to signal acquisition of the input by the CDAC (this time is defined as T_{acq}). Following these two cycles, the input sample is taken and held. The A/D conversion follows this cycle with the duration controlled by the internal clock cycle.

Figure 8 - Sample and Hold Function



During T_{acq}, the equivalent circuit of the HADC674Z input is as shown in Figure 9 (the time constant of the input is independent of which input level is used). This CDAC capacitance must be charged up to the input voltage during T_{acq}. Since the CDAC time constant is 100 nsecs, there is more than enough time for settling the input to 12-bits of accuracy during T_{acq}. The excess time left during T_{acq} allows the user's buffer amp to settle after being switched to the CDAC load.

Figure 9 - Equivalent HADC674Z Input Circuit



Note that because the sample is taken relative to the R/$\overline{C}$ transition, Tacq is also the traditional "aperturedelay" of this internal sample and hold.

Since T_{acq} is measured in clock cycles, its duration will vary with the internal clock frequency. This results in T_{acq} =1.7 µsec between units and over temperature.

Offset, gain and linearity errors of the S/H circuit, as well as the effects of its droop rate, are included in the overall specs for the HADC674Z.

APERTURE UNCERTAINTY

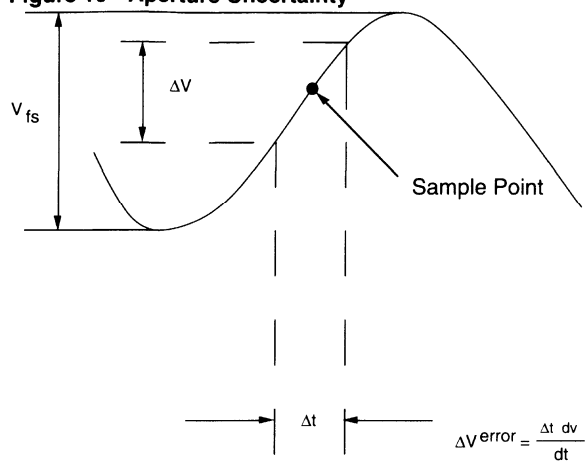
Often the limiting factor in the application of the sample and hold is the uncertainty in the time that the actual sample is taken, i.e., the "aperture jitter" or T_{AJ}. The HADC674Z has a nominal aperture jitter of 8 nsecs between samples. With this jitter, it is possible to accurately sample a wide range of input signals.

The aperture jitter causes an amplitude uncertainty for any input where the voltage is changing. The approximate voltage error due to aperture jitter depends on the slew rate of the signal at the sample point (see Figure 10). The magnitude of this change for a sine wave can be calculated:

$Verr \leq V_{fs}/2^{N+1}$ (where Verr is the allowable error voltage

and Vfs is the full scale voltage)

Figure 10 - Aperture Uncertainty



From Figure 10:

$Sr=\Delta V/\Delta T=2\ \pi fVp$

Let $\Delta V=Verr=V_{fs}2^{-(N+1)}$, $Vp=Vin/2$ and $\Delta T=t_{AJ}$ (The time during which unwanted voltage change occurs)

The above conditions then yield:

$V_{fs}/2^{N+1} \geq \pi f Vin\ t_{AJ}$ or $f_{max} \leq V_{fs}/(\pi Vin\ t_{AJ})2N+1$

For the HADC674Z, T_{AJ}=8 nsec, therefore $f_{max} \leq 5$ kHz.

For higher frequency signal inputs, an external sample and hold is recommended.

TYPICAL INTERFACE CIRCUIT

The HADC674Z is a complete A/D converter that is fully operational when powered up and issued a Start Convert Signal. Only a few external components are necessary as shown in Figure 11 and 12. The two typical interface circuits are for operating the HADC674Z in either an unipolar or bipolar input mode. Further information is given in the following sections on these connections, but first a few conditions concerning board layout to achieve the best operation.

For each application of this device, strict attention must be given to power supply decoupling, board layout (to reduce pickup between analog and digital sections), and grounding. Digital timing, calibration and the analog signal source must be considered for correct operation.

To achieve specified accuracy, a double-sided printed circuit board with a copper ground plane on the component side is recommended. Keep analog signal traces away from digital lines. It is best to lay the PC board out such that there is an analog section and a digital section with a single point ground connection between the two through an RF bead located as close to the device as possible. If possible, run analog signals between ground traces and cross digital lines at right angles only.

POWER SUPPLIES

The supply voltages for the HADC674Z must be kept as quiet as possible from noise pickup and also regulated from transients or drops. Because the part has 12-bit accuracy, voltage spikes on the supply lines can cause several LSB deviations on the output. Switching power supply noise can be a problem. Careful filtering and shielding should be employed to prevent the noise from being pickup by the converter.

Capacitor bypass pairs are needed from each supply pin to it's respective ground to filter noise and counter the problems caused by the variations in supply current. A 10 µF tantalum and a 0.1 µF ceramic type in parallel between V_{LOGIC} (pin 1) and digital common (pin 15), and V_{CC} (pin 7) and analog common (pin 9) is sufficient. V_{EE} is generated internally so pin 11 may be grounded or connected to a negative supply if the HADC674Z is being used to upgrade an already existing design.

GROUNDING CONSIDERATIONS

Any ground path from the analog and digital ground should be as low resistance as possible to accommodate the ground currents present with this device.

The analog ground current is approximately 6 mADC while the digital ground is 3 mADC The analog and digital common pins should be tied together as close to the package as possible to guarantee best performance. The code dependent currents flow through the V_{LOGIC} and V_{CC} terminals and not through the analog and digital common pins.

The HADC674Z may be operated by a µP or in the stand-alone mode. The part has four standard input ranges: 0 V to +10 V, 0 V to +20 V, ±5 V and ±10 V The maximum errors that are listed in the specifications for gain and offset may be adjusted externally to zero as explained in the next two sections.

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CALIBRATION AND CONNECTION PROCEDURES

UNIPOLAR

The calibration procedure consists of adjusting the converter's most negative output to its ideal value for offset adjustment, and then adjusting the most positive output to its ideal value for gain adjustment.

Starting with offset adjustment and referring to Figure 11, the midpoint of the first LSB increment should be positioned at the origin to get an output code of all 0s. To do this, an input of +1/2 LSB or +1.22 mV for the 10 V range and +2.44 mV for the 20 V range should be applied to the HADC674Z. Adjust the offset potentiometer R1 for code transition flickers between 0000 0000 0000 and 0000 0000 0001.

The gain adjustment should be done at positive full scale. The ideal input corresponding to the last code change is applied. This is 1 and 1/2 LSB below the nominal full scale which is +9.9963 V for the 10 V range and +19.9927 V for the 20 V range. Adjust the gain potentiometer R2 for flicker between codes 1111 1111 1110 and 1111 1111 1111. If calibration is not necessary for the intended application, replace R2 with a 50 Ω, 1% metal film resister and remove the network from pin 12. Connect pin 12 to pin 9. Connect the analog input to pin 13 for the 0 V to 10 V range or to pin 14 for the 0 V to 20 V range.

BIPOLAR

The gain and offset errors listed in the specification may be adjusted to zero using the potentiometers R1 and R2 (See Figure 12). If adjustment is not needed, either or both pots may be replaced by a 50 Ω, 1% metal film resistor.

To calibrate, connect the analog input signal to pin 13 for a ±5 V range or to pin 14 for a ±10 V range. First apply a DC input voltage 1/2 LSB above negative full scale which is -4.9988 V for the ±5 V range or -9.9976 V for the ±10 V range. Adjust the offset potentiometer R1 for flicker between output codes 0000 0000 0000 and 0000 0000 0001. Next, apply a DC input voltage 1 and 1/2 LSB below positive full scale which is +4.9963 V for the ±5 V range or +9.9927 V for the ±10 V range. Adjust the gain potentiometer R2 for flicker between codes 1111 1111 1110 and 1111 1111 1111.

ALTERNATIVE

In some applications, a full scale of 10.24 V (for an LSB of 2.5 mV) or 20.48 V (for an LSB of 5.0 mV) is more convenient. In the Unipolar mode of operation, replace R2 by 200 Ω potentiometer and add 150 Ω in series with pin 13 for 10.24 V input range or 500 Ω in series with pin 14 for 20.48 V input range. In bipolar mode of operation, replace R1 by 500 Ω potentiometer (in addition to the previous changes). The calibration will remain similar to the standard calibration procedure.

Figure 11 - Unipolar Input Connections

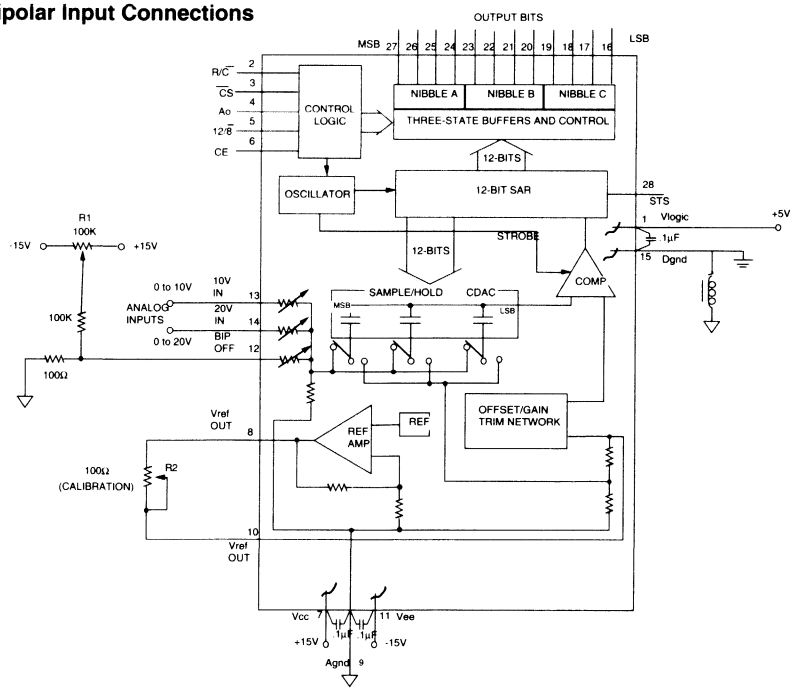


Figure 14 - Control Logic

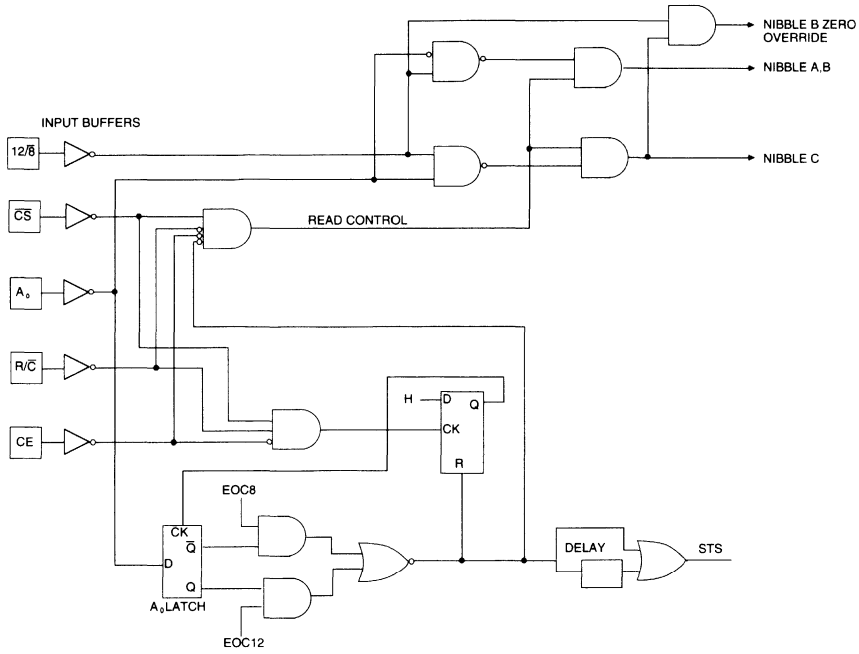
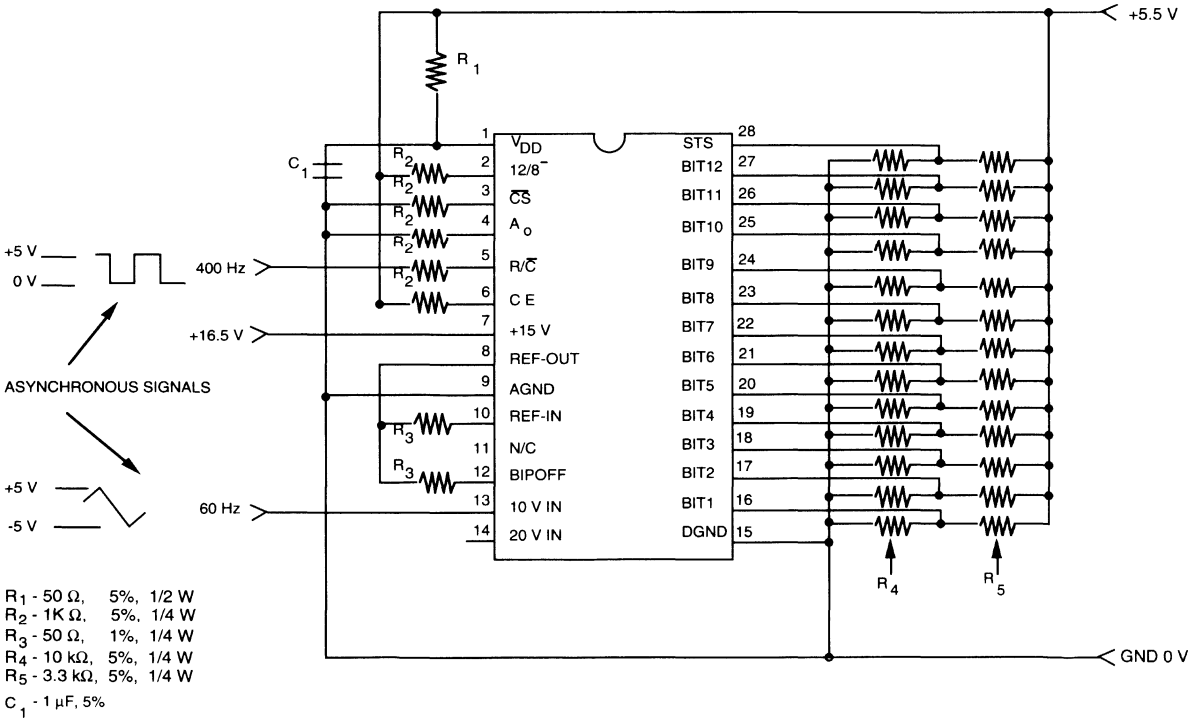


Figure 15 - Burn-In Schematic



R_1 - 50 Ω, 5%, 1/2 W
R_2 - 1K Ω, 5%, 1/4 W
R_3 - 50 Ω, 1%, 1/4 W
R_4 - 10 kΩ, 5%, 1/4 W
R_5 - 3.3 kΩ, 5%, 1/4 W
C_1 - 1 µF, 5%

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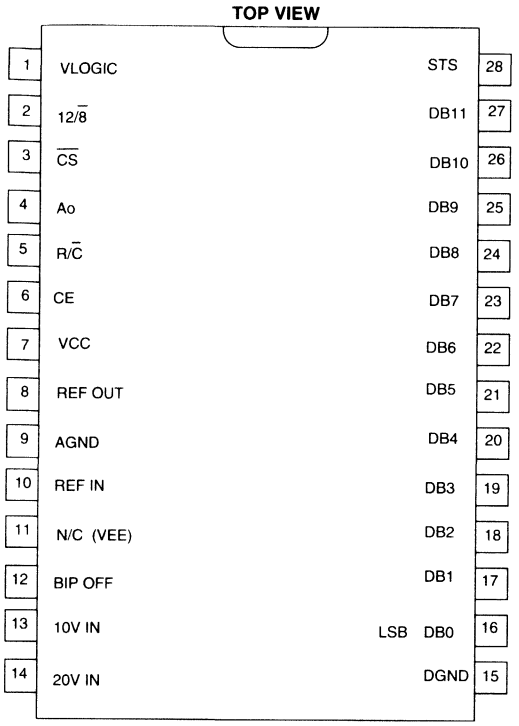
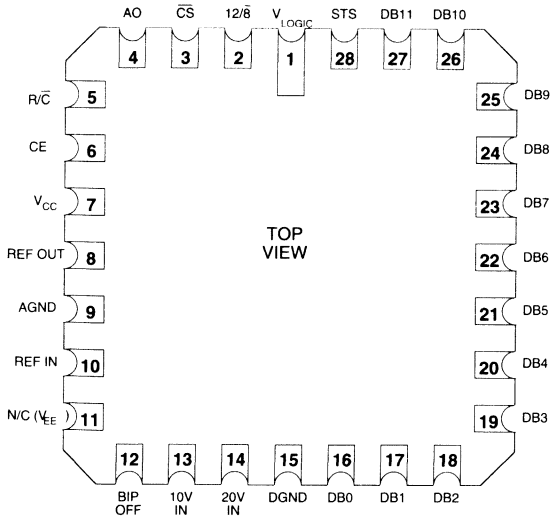
PIN Assignment HADC674Z



28-LEAD DIP



28-LEAD LCC

PIN Functions HADC674Z

NAME	FUNCTION
V_{LOGIC}	Logic Supply Voltage, Nominally +5 V
12/$\overline{8}$	Data Mode Selection
$\overline{CS}$	Chip Selection
Ao	Byte Address/Short Cycle
R/$\overline{C}$	Read/Convert
CE	Chip Enable
V_{CC}	Analog Positive Supply Voltage, Nominally +15 V
REF OUT	Reference Output, Nominally +10 V
AGND*	Analog Ground
REF IN	Reference Input
N/C (V_{EE})	This pin is not connected to the device.
BIP OFF	Bipolar Offset
10 V IN	10 Volt Analog Input
20 V IN	20 Volt Analog Input
DGND	Digital Ground
DB0 - DB11	Digital Data Output DB11 - MSB DB0 - LSB
STS	Status

* The lid on the sidebrazed and LCC packages are internally connected to AGND.

LEADERSHIP IN DATA CONVERSION AND SIGNAL PROCESSING

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SIGNAL PROCESSING TECHNOLOGIES

SPT774

FAST, COMPLETE 12-BIT μP COMPATIBLE A/D CONVERTER WITH SAMPLE/HOLD

3

FEATURES

- Improved Pin-To-Pin Compatible Monolithic Version of the HI774
- Complete 12-Bit A/D Converter with Sample/Hold, Reference and Clock
- Low Power Dissipation (150 mW Max)
- 12-Bit Linearity (Over Temp)
- 8 μs Max Conversion Time Including S/H Acquisition
- No Negative Supply Required
- Full Bipolar and Unipolar Input Range

APPLICATIONS

- Military/Industrial Data Acquisition Systems
- 8 or 12-Bit μP Input Functions
- Process Control Systems
- Test and Scientific Instruments
- Personal Computer Interface

GENERAL DESCRIPTION

The SPT774 is a complete, 12-bit successive approximation A/D converter. Included on chip is an internal reference, clock, and a sample and hold. The S/H allows full nyquist sampling of input signals.

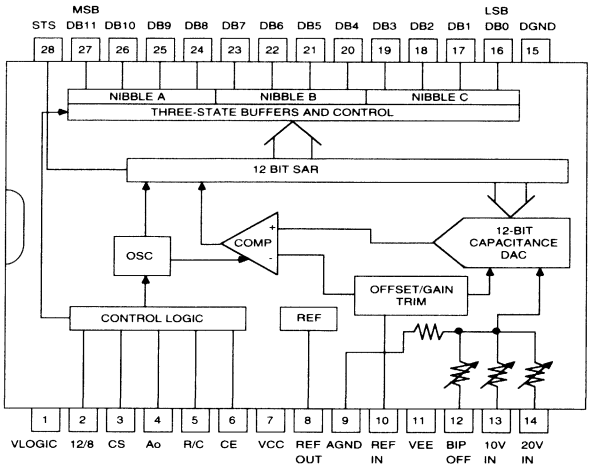
The SPT774 features 8 μs (Max) conversion time of 10 or 20 Volt input signals. Also, a three-state output buffer is added for direct interface to an 8, 12, or 16-bit μP bus.

The BEMOS process and monolithic construction reduces power consumption, ground noise, and keeps parasitics to a minimum. In addition, the thin film available on this process allows active adjustment of DAC and comparator offsets, linearity errors, and gain errors.

The SPT774 has standard bipolar and unipolar input ranges of 10 V and 20 V that are controlled by a bipolar offset pin and laser trimmed for specified linearity, gain and offset accuracy.

Power requirements are +5 V and +12 V to +15 V with a maximum dissipation of 150 mW at the specified voltages. Power consumption is about five times lower than currently available devices, and a negative power supply is not needed.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATING (Beyond which damage may occur) [1] 25 °C

Supply Voltages

Positive Supply Voltage (V_{CC} to DGND) ..... 0 to +16.5 V
Logic Supply Voltage (V_{LOGIC} to DGND) ..... 0 to +7 V
Analog to Digital Ground (AGND to DGND) . -0.5 to +1 V

Input Voltages

Control Input Voltages (to DGND)
(CE, CS, Ao, 12/8, R/C) ..... -0.5 to V_{LOGIC} +0.5 V
Analog Input Voltage (to AGND)
(REF IN, BIP OFF, 10 Vin) ..... ±16.5 V
20 V Vin Input Voltage (to AGND) ..... ±24 V

Output

Reference Output Voltage ..... Indefinite short to GND
Momentary short to V_{CC}

Temperature

Operating Temperature, ambient ..... -55 to +125 °C
junction ..... +175 °C
Lead Temperature, (soldering 10 seconds) ..... +300 °C
Storage Temperature ..... -65 to +150 °C
Power Dissipation ..... 1000 mW
Thermal Resistance (θ_{jA}) ..... 48 °C/W

Note: Operation at any Absolute Maximum Rating is not implied. See Operating Conditions for proper nominal applied conditions in typical applications.

ELECTRICAL SPECIFICATIONS

$T_A=T_{MIN}$ to T_{MAX}, V_{CC}=+15 V or +12 V, V_{LOGIC}=+5 V, unless otherwise specified.

PARAMETER	TEST CONDITIONS	TEST LEVEL	SPT774C MIN	SPT774C TYP	SPT774C MAX	SPT774B MIN	SPT774B TYP	SPT774B MAX	SPT774A MIN	SPT774A TYP	SPT774A MAX	UNITS
DC ELECTRICAL CHARACTERISTICS												
Resolution		VI			12			12			12	BITS
Linearity Error[1]	T_A=0 to 70 °C	VI			±1			±1/2			±1/2	LSB
	T_A = -25 to +85 °C	I			±1			±1/2			±1/2	LSB
	T_A = -55 to +125 °C	I			±1			±1			±1	LSB
Differential Linearity	No Missing Codes	VI	11			12			12			BITS
Unipolar Offset; 10 V, 20 V	+25 °C Adjustable to Zero	VI		±0.1	±2		±0.1	±2		±0.1	±2	LSB
Bipolar Offset1; ±5 V,±10 V	+25 °C Adjustable to Zero	VI			±10			±4			±4	LSB
Full Scale Calibration Error[2] All Input Ranges	+25 °C Adjustable to Zero	VI			0.3			0.3			0.3	% of FS
	No Adjustment at +25°											
	T_A = 0 to 70 °C	V		0.5			0.4			0.35		%of FS
	T_A = -25 to +85 °C	V		0.7			0.5			0.4		%of FS
	T_A = -55 to +125 °C	V		0.8			0.6			0.4		%of FS
	With Adjustment at +25 °C											
	T_A = 0 to 70 °C	V		0.22			0.12			0.05		%of FS
	T_A = -25 to +85 °C	V		0.4			0.2			0.1		%of FS
	T_A = -55 to +125 °C	V		0.5			0.25			0.12		%of FS
Temperature Coefficients[3]	Using Internal Reference											
Unipolar Offset	T_A = 0 to 70 °C	IV		±0.2	±2		±0.1	±1		±0.1	±1	LSB
					(10)			(5)			(5)	(ppm/°C)
	T_A = -25 to +85 °C	IV			±2			±1			±1	LSB
					(5)			(2.5)			(2.5)	(ppm/°C)
	T_A = -55 to +125 °C	IV			±2			±1			±1	LSB
					(5)			(2.5)			(2.5)	(ppm/°C)
Bipolar Offset	T_A = 0 to 70 °C	IV		±0.2	±2		±0.1	±1		±0.1	±1	LSB
					(10)			(5)			(5)	(ppm/°C)
	T_A = -25 to +85 °C	IV			±2			±1			±1	LSB
					(5)			(2.5)			(2.5)	(ppm/°C)

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ELECTRICAL SPECIFICATIONS

$T_A = T_{MIN}$ to T_{MAX}, V_{CC} = +15 V or +12 V, V_{LOGIC} = +5 V, unless otherwise specified.

PARAMETER	TEST CONDITIONS	TEST LEVEL	SPT774C MIN	SPT774C TYP	SPT774C MAX	SPT774B MIN	SPT774B TYP	SPT774B MAX	SPT774A MIN	SPT774A TYP	SPT774A MAX	UNITS
DC ELECTRICAL CHARACTERISTICS												
Bipolar Offset (Cont.)	T_A = -55 to +125 °C	IV			±4 (10)			±2 (5)			±1 (2.5)	LSB (ppm/°C)
Full Scale Calibration	T_A = 0 to 70 °C	IV			±9 (45)			±5 (25)			±2 (10)	LSB (ppm/°C)
	T_A = -25 to +85 °C	IV			±12 (50)			±7 (25)			±3 (12)	LSB (ppm/°C)
	T_A = -55 to +125 °C	IV			±20 (50)			±10 (25)			±5 (12.5)	LSB (ppm/°C)
Power Supply Rejection	Max change in full scale calibration											
+13.5 V<V_{CC}<+16.5 V or +11.4 V<V_{CC}<+12.6 V		VI		±0.5	±2		±0.5	±1		±0.5	±1	LSB
+4.5 V<V_{LOGIC}<+5.5 V		VI		±0.1	±0.5		±0.1	±0.5		±0.1	±0.5	LSB
Analog Input Ranges												
Bipolar		VI	-5 -10		+5 +10	-5 -10		+5 +10	-5 -10		+5 +10	Volts Volts
Unipolar		VI	0 0		+10 +20	0 0		+10 +20	0 0		+10 +20	Volts Volts
Input Impedance 10 Volt Span 20 Volt Span		VI	 3.75 15	 5 20	 6.25 25	 3.75 15	 5 20	 6.25 25	 3.75 15	 5 20	 6.25 25	 kΩ kΩ
Power Supplies Operating Voltage Range												
V_{LOGIC}		VI	+4.5		+5.5	+4.5		+5.5	+4.5		+5.5	Volts
V_{CC}		VI	+11.4		+16.5	+11.4		+16.5	+11.4		+16.5	Volts
V_{EE}	Not Required for circuit operation.											
Operating Current												
I_{LOGIC}		VI		0.5	1		0.5	1		0.5	1	mA
I_{CC}		VI		7	9		7	9		7	9	mA
I_{EE}	Not required for circuit operation.											
Power Dissipation +15 V, +5 V		VI		110	150		110	150		110	150	mW
Internal Reference Voltage Output Current[4]		VI VI	9.97	10	10.03 2	9.97	10	10.03 2	9.97	10	10.03 2	Volts mA

ELECTRICAL SPECIFICATIONS

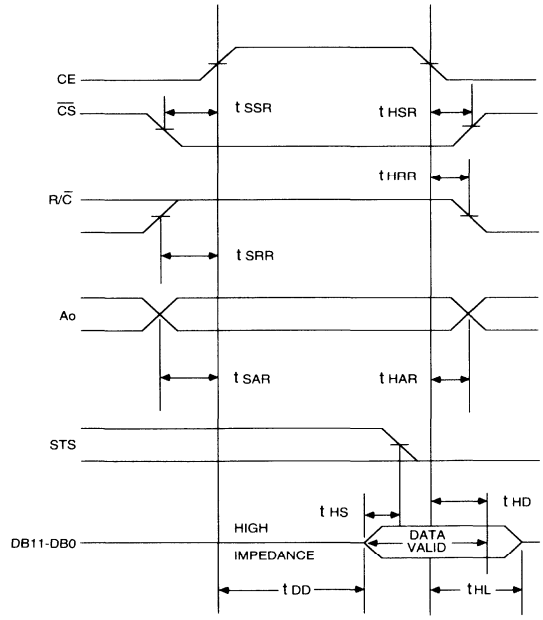
READ MODE TIMING CHARACTERISTICS

T_A = 25 °C, V_{CC} = +15.0 V or +12 V, V_{LOGIC} = +5 V, unless otherwise specified.

PARAMETER	TEST CONDITIONS	TEST LEVEL	SPT774C MIN	SPT774C TYP	SPT774C MAX	SPT774B MIN	SPT774B TYP	SPT774B MAX	SPT774A MIN	SPT774A TYP	SPT774A MAX	UNITS
AC ELECTRICAL CHARACTERISTICS[1]												
t_{DD} Access Time from CE		I			150			150			150	ns
t_{HD} Data Valid After CE Low		I	25			25			25			ns
t_{HL} Output Float Delay		I			150			150			150	ns
t_{SSR} $\overline{CS}$ to CE Setup		I	50	0		50	0		50	0		ns
t_{SRR} R/$\overline{C}$ to CE Setup		I	0	0		0	0		0	0		ns
t_{SAR} Ao to CE Setup		I	50			50			50			ns
t_{HSR} $\overline{CS}$ Valid After CE Low		I	0	0		0	0		0	0		ns
t_{HRR} R/$\overline{C}$ High After CE Low		I	50			50			50			ns
t_{HS} STS Delay After Data Valid		I	90		300	90		300	90		300	ns
t_{HAR} Ao Valid after CE Low		I	50			50			50			ns

Note 1: Time is measured from 50% level of digital transitions. Tested with a 100 pF and 3 kΩ load for high impedance to drive and tested with 10 pF and 3 kΩ load for drive to high impedance.

Figure 2 - Read Mode Timing Diagram



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ELECTRICAL SPECIFICATIONS

STAND-ALONE MODE TIMING CHARACTERISTICS

T_A = 25 °C, V_{CC} = +15.0 V or +12 V, V_{LOGIC} = +5 V, unless otherwise specified.

PARAMETER	TEST CONDITIONS	LEVEL	SPT774C MIN	SPT774C TYP	SPT774C MAX	SPT774B MIN	SPT774B TYP	SPT774B MAX	SPT774A MIN	SPT774A TYP	SPT774A MAX	UNITS
AC ELECTRICAL CHARACTERISTICS												
t_{HRL} Low R/$\overline{C}$ Pulse Width		I	50			50			50			ns
t_{DS} STS Delay from R/$\overline{C}$		I			200			200			200	ns
t_{HDR} Data Valid After R/$\overline{C}$ Low		I	25			25			25			ns
t_{HS} STS Delay After Data Valid		I	90		300	90		300	90		300	ns
t_{HRH} High R/$\overline{C}$ Pulse Width		I	150			150			150			ns
t_{DDR} Data Access Time		I			150			150			150	ns
SAMPLE AND HOLD												
Acquisition Time		IV	1.35	1.45	1.55	1.35	1.45	1.55	1.35	1.45	1.55	µs
Aperture Uncertainty Time		V		1			1			1		ns,RMS

Figure 3 - Low Pulse for R/$\overline{C}$ - Outputs Enabled After Conversion

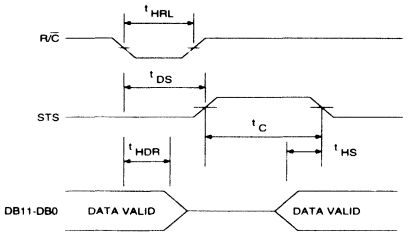
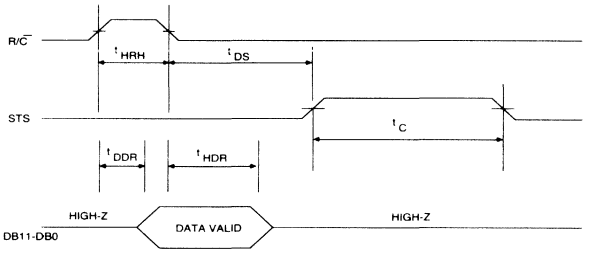


Figure 4 - High Pulse for R/$\overline{C}$ - Outputs Enabled While R/$\overline{C}$ is High, Otherwise High Impedance



TEST LEVEL CODES

All electrical characteristics are subject to the following conditions:

All parameters having min/max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality Assurance inspection. Any blank section in the data column indicates that the specification is not tested at the specified condition.

Unless otherwise noted, all tests are pulsed tests; therefore, $T_J = T_C = T_A$.

TEST LEVEL	TEST PROCEDURE
I	100% production tested at the specified temperature.
II	100% production tested at T_A=25 °C, and sample tested at the specified temperatures.
III	QA sample tested only at the specified temperatures.
IV	Parameter is guaranteed (but not tested) by design and characterization data.
V	Parameter is a typical value for information purposes only.
VI	100% production tested at T_A = 25 °C. Parameter is guaranteed over specified temperature range.

DEFINITION OF SPECIFICATIONS

INTEGRAL LINEARITY ERROR

Linearity error refers to the deviation of each individual code from a line drawn from "zero" through "full scale" with all offset errors nulled out (See Figure 5 and 6). The point used as "zero" occurs 1/2 LSB (1.22 mV for a 10 Volt span) before the first code transition (all zeros to only the LSB "on"). "Full scale" is defined as a level 1 and 1/2 LSB beyond the last code transition (to all ones). The deviation of a code from the true straight line is measured from the middle of each particular code.

The SPT774AC and BC grades are guaranteed for maximum nonlinearity of ±1/2 LSB. For these grades, this means that an analog value which falls exactly in the center of a given code width will result in the correct digital output code. Values nearer the upper or lower transition of the code width may produce the next upper or lower digital output code. The SPT774AM, BM, CC and CM grades are guaranteed to ±1 LSB maximum error. For these grades, an analog value which falls within a given code width will result in either the correct code for the region or either adjacent one. The linearity is not user-adjustable.

DIFFERENTIAL LINEARITY ERROR (NO MISSING CODES)

A specification which guarantees no missing codes requires that every code combination appear in a monotonically increasing sequence as the analog input level is increased. Thus every code must have a finite width. For the SPT774 type BC, AC, BM and AM grades, which guarantee no missing codes to 12-bit resolution, all 4096 codes must be present over the entire operating temperature ranges. The SPT774 CC and CM grades guarantee no missing codes to 11-bit resolution over temperature; this means that all code combinations of the upper 11-bits must be present; in practice, very few of the 12-bit codes are missing.

DIFFERENTIAL NONLINEARITY

Differential nonlinearity is a measure of how much the actual quantization step width varies from the ideal step width of 1 LSB. Figure 6 shows a differential nonlinearity of 2 LSB - the actual step width is 3 LSB. The SPT774's specification gives the worst case differential nonlinearity in the A/D transfer function under specified dynamic operating conditions. Small, localized differential nonlinearities may be insignificant when digitizing full scale signals. However, if a low level input signal happens to fall on the part of the A/D transfer function with the differential nonlinearity error, the effect will be significant.

MISSING CODES

Missing codes represent a special kind of differential nonlinearity. The quantization step width for a missing code is 0 LSB, which results in a differential nonlinearity of -1 LSB. Figure 6 points out two missed codes in the transfer function.

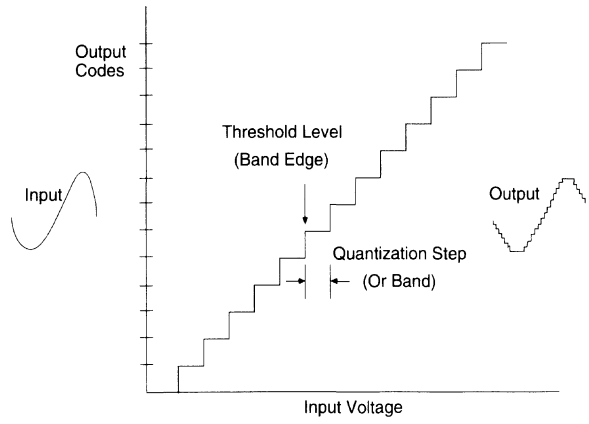
QUANTIZATION UNCERTAINTY

Analog-to-digital converters exhibit an inherent quantization uncertainty of ±1/2 LSB. This uncertainty is a fundamental characteristic of the quantization process and cannot be reduced for a converter of a given resolution.

QUANTIZATION ERROR

Quantization error is the fundamental, irreducible error associated with the perfect quantizing of a continuous (analog) signal into a finite number of digital bits (A/D transfer function). A 12-bit A/D converter can represent an input voltage with a best case uncertainty of 1 part in 2^{12} (1 part in 4096). In real A/Ds under dynamic operating conditions, the quantization bands (bit change step vs input amplitude) for certain codes can be significantly larger (or smaller) than the ideal. The ideal width of each quantization step (or band) is Q=FSR/2^N where FSR=full scale range and N=12. Nonideal quantization bands represent differential non linearity errors (See figures 5, 6 and 7).

Figure 5 - Static Input Conditions



RESOLUTION - ACTUAL vs AVAILABLE

The available resolution of an N-bit converter is 2^N. This means it is theoretically possible to generate 2^N unique output codes.

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Figure 6 - Dynamic Conditions

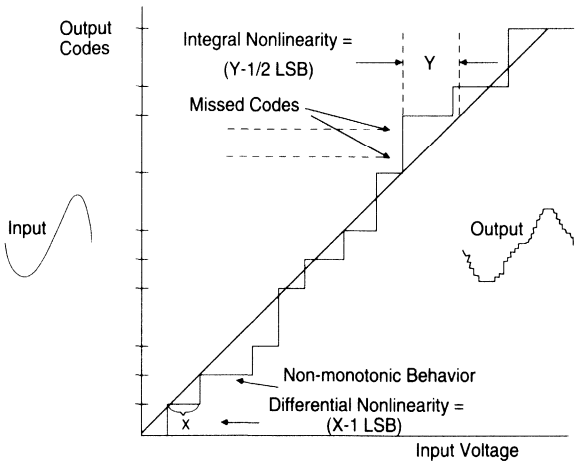
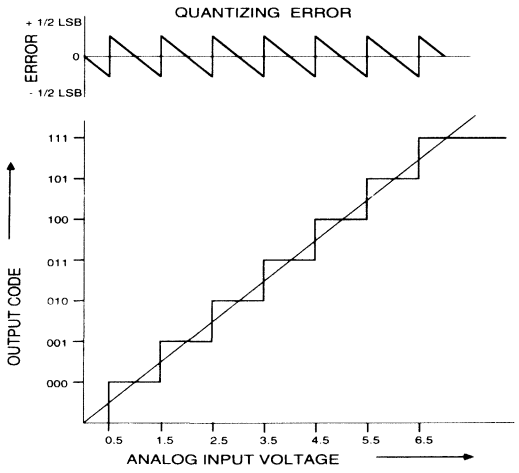


Figure 7 - Quantizing Error



THROUGHPUT

Maximum throughput is the greatest number of conversions per second at which an ADC will deliver its full rate performance. This is equivalent to the inverse of the sum of the multiplex time (if applicable), the S/H settling time and the conversion time.

GAIN

The slope of the transfer curve. Gain is generally user adjustable to compensate for long term drift.

ACQUISITION TIME/APERTURE DELAY TIME

In the SPT774, this is the time delay between the R/$\overline{C}$ falling edge and the actual start of the HOLD mode in a sample and HOLD function.

APERTURE JITTER

A specification indicating how much the aperture delay time varies between samples.

SUCCESSIVE APPROXIMATION ADC

The successive approximation converter uses an architecture with inherently high throughput rates which converts high frequency signals with great accuracy. A sample and hold type circuit can be used on the input to freeze these signals during conversion.

A N-bit successive approximation converter performs a sequence of tests comparing the input voltage to a successively narrower voltage range. The first range is half full scale, the next is quarter full scale, etc., until it reaches the Nth test which narrows it to a range of $1/2^N$ of full scale. The conversion time is fixed by the clock frequency and is thus independent of the input voltage.

UNIPOLAR OFFSET

The first transition should occur at a level 1/2 LSB above analog common. Unipolar offset is defined as the deviation of the actual transition from that point. This offset can be adjusted as discussed on the following pages. The unipolar offset temperature co-efficient specifies the maximum change of the transition point over temperature, with and without external adjustment.

BIPOLAR OFFSET

In the bipolar mode, the major carry transition (0111 1111 1111 to 1000 0000 0000) should occur for an analog value 1/2 LSB below analog common. The bipolar offset error and temperature co-efficient specify the initial deviation and maximum change in the error over temperature.

CONVERSION TIME

The time required to complete a conversion over the specified operating range. Conversion time can be expressed as time/bit for a converter with selectable resolution or as time/conversion when the number of bits is constant. The SPT774 is specified as time/conversion for all 12-bits. Conversion time should not be confused with maximum allowable analog input frequency which is discussed later.

FULL SCALE CALIBRATION ERROR

The last transition (from 1111 1111 1110 to 1111 1111 1111 1111) should occur for an analog value 1 and 1/2 LSB below the nominal full scale (9.9963 Volts for 10.000 Volts full scale). The full scale calibration error is the deviation of the actual level at the last transition from the ideal level. This error, which typically is 0.05 to 0.1% of full scale, can be trimmed out as show in Figure 11 and 12 on page 17. The full scale calibration error over temperature is given with and without the initial error trimmed out. The temperature coefficients for each grade indicate the maximum change in the full scale gain from the initial value using the internal 10 Volt reference.

TEMPERATURE COEFFICIENTS

The temperature coefficients for full scale calibration, unipolar offset, and bipolar offset specify the maximum change from the initial (25 °C) value to the value at Tmin or Tmax.

POWER SUPPLY REJECTION

The standard specifications for the SPT774 assume +5.00 and +15.00 or +12.00 Volt supplies. The only effect of power supply error on the performance of the device will be a small change in the full scale calibration. This will result in a linear change in all lower order codes. The specifications show the maximum change in calibration from the initial value with the supplies at the various limits.

CODE WIDTH

The fundamental unit for A/D converter specifications is the code width. This is defined as the range of analog input values for which a given digital output code will occur. The nominal value of a code width is equivalent to 1 least significant bit (LSB) of the full scale range or 2.44 mV out of 10 Volts for a 12-bit ADC.

LEFT-JUSTIFIED DATA

The data format used in the SPT774 is left-justified. This means that the data represents the analog input as fraction of full scale, ranging from 0 to 4095/4096. This implies a binary point to the left of the MSB.

MONOTONICITY

This characteristic describes an aspect of the code to code progression from minimum to maximum input. A device is said to be monotonic if the output code continuously increases as the input signal increases, and if the output code continuously decreases as the input signal decreases. Figure 6 demonstrates non-monotonic behavior.

CIRCUIT OPERATION

The SPT774 is a complete 12-bit analog-to-digital converter which consists of a single chip version of the industry standard 774. This single chip contains a precision 12-bit capacitor digital-to-analog converter (CDAC) with voltage reference, comparator, successive approximation register (SAR), sample and hold, clock, output buffers and control circuitry to make possible to use the SPT774 with few external components.

When the control section of the SPT774 initiates a conversion command, the clock is enabled and the successive-approximation register is reset to all zeros. Once the conversion cycle begins, it can not be stopped or re-started and data is not available from the output buffers.

The SAR, timed by the clock, sequences through the conversion cycle and returns an end-of-convert flag to the control section of the ADC. The clock is then disabled by the control section, the output status goes low, and the control section is enabled to allow the data to be read by external command.

The internal SPT774 12-bit CDAC is sequenced by the SAR starting from the MSB to the LSB at the beginning of the conversion cycle to provide an output voltage from the CDAC that is equal to the input signal voltage (which is divided by the input voltage divider network). The comparator determines whether the addition of each successively-weighted bit voltage causes the CDAC output voltage summation to greater or less than the input voltage; it the sum is less, the bit is left on; if more, the bit is turned off. After testing all the bits, the SAR contains a 12-bit binary code which accurately represents the input signal to within ±1/2 LSB.

The internal reference provides the voltage reference to the CDAC with excellent stability over temperature and time. The reference is trimmed to 10.00 Volts ±1% and can supply up to 2 mA to an external load in addition to that required to drive the reference input resistor (1 mA) and offset resistor (1 mA) when operating with ±15 V supplies. If the SPT774 is used with ±12 V supplies, or if external current must be supplied over the full temperature range, and external buffer amplifier is recommended. Any external load on the SPT774 reference must remain constant during conversion.

The sample and hold feature is a bonus of the CDAC architecture. Therefore the majority of the S/H specifications are included within the A/D specifications.

Although the sample and hold circuit is not implemented in the classical sense, the sampling nature of the capacitive DAC makes the SPT774 appear to have a built in sample and hold. This sample and hold action substantially increases the signal bandwidth of the SPT774 over that of similar competing devices.

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Note that even though the user may use an external sample and hold for very high frequency inputs, the internal sample and hold still provides a very useful isolation function. Once the internal sample is taken by the CDAC capacitance, the input of the SPT774 is disconnected from the user's sample and hold. This prevents transients occurring during conversion from being inflicted upon the attached sample and hold buffer. All other 774 circuits will cause a transient load current on the sample and hold which will upset the buffer output and may add error to the conversion itself.

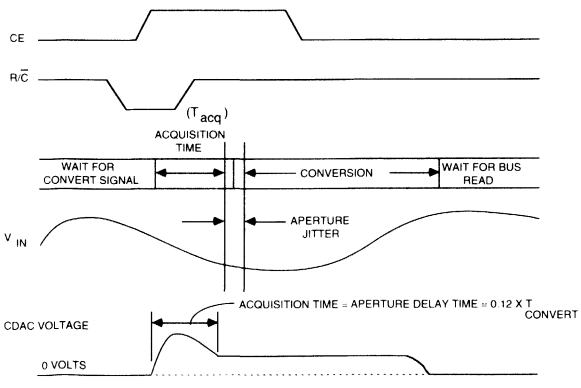
Furthermore, the isolation of the input after the acquisition time in the SPT774 allows the user an opportunity to release the hold on an external sample and hold and start it tracking the next sample. This will increase system throughput with the user's existing components.

SAMPLE AND HOLD FUNCTION

When using an external S/H, the SPT774 acts as any other 774 device because the internal S/H is transparent. The sample/hold function in the SPT774 is inherent to the capacitor DAC structure, and its timing characteristics are determined by the internally generated clock. However, for limited frequency ranges, the internal S/H may eliminate the need for an external S/H. This function will be explained in the next two sections.

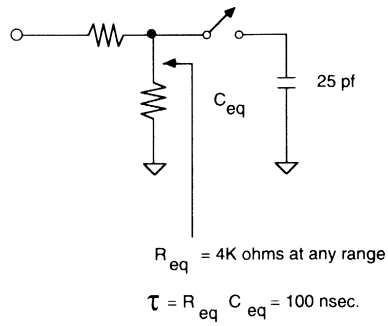
The operation of the S/H function is internal to the SPT774 and is controlled through the normal R/$\overline{C}$ control line (refer to Figure 8). When the R/$\overline{C}$ line makes a negative transition, the SPT774 starts the timing of the sampling and conversion. The first 2 clock cycles are allocated to signal acquisition of the input by the CDAC (this time is defined as T_{acq}). Following these two cycles, the input sample is taken and held. The A/D conversion follows this cycle with the duration controlled by the internal clock cycle.

Figure 8 - Sample and Hold Function



During T_{acq}, the equivalent circuit of the SPT774 input is as shown in Figure 9 (the time constant of the input is independent of which input level is used). This CDAC capacitance must be charged up to the input voltage during T_{acq}. Since the CDAC time constant is 100 nsecs, there is more than enough time for settling the input to 12-bits of accuracy during T_{acq}. The excess time left during T_{acq} allows the user's buffer amp to settle after being switched to the CDAC load.

Figure 9 - Equivalent SPT774 Input Circuit



Note that because the sample is taken relative to the R/$\overline{C}$ transition, Tacq is also the traditional "aperture delay" of this internal sample and hold.

Since T_{acq} is measured in clock cycles, its duration will vary with the internal clock frequency. This results in T_{acq} =1.45 µsec between units and over temperature.

Offset, gain and linearity errors of the S/H circuit, as well as the effects of its droop rate, are included in the overall specs for the SPT774.

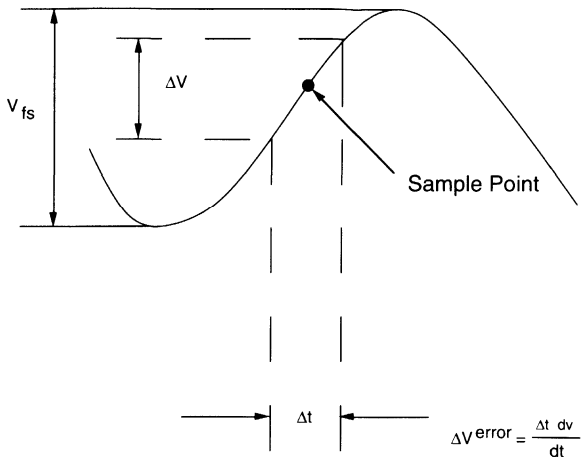
APERTURE UNCERTAINTY

Often the limiting factor in the application of the sample and hold is the uncertainty in the time that the actual sample is taken, i.e., the "aperture jitter" or T_{AJ}. The SPT774 has a nominal aperture jitter of 8 nsecs between samples. With this jitter, it is possible to accurately sample a wide range of input signals.

The aperture jitter causes an amplitude uncertainty for any input where the voltage is changing. The approximate voltage error due to aperture jitter depends on the slew rate of the signal at the sample point (see Figure 10). The magnitude of this change for a sine wave can be calculated:

$Verr \leq V_{fs}/2^{N+1}$ (where Verr is the allowable error voltageand Vfs is the full scale voltage)

Figure 10 - Aperture Uncertainty



From Figure 10:

$Sr=\Delta V/\Delta T=2\ \pi fVp$

Let $\Delta V=Verr=V_{fs}2^{-(N+1)}$, $Vp=Vin/2$ and $\Delta T=t_{AJ}$ (The time during which unwanted voltage change occurs)

The above conditions then yield:

$V_{fs}/2^{N+1} \geq \pi f Vin\ t_{AJ}$ or $f_{max} \leq V_{fs}/(\pi Vin\ t_{AJ})2N+1$

For the SPT774, T_{AJ}=1 nsec, therefore $f_{max} \leq$40 kHz.

For higher frequency signal inputs, an external sample and hold is recommended.

TYPICAL INTERFACE CIRCUIT

The SPT774 is a complete A/D converter that is fully operational when powered up and issued a Start Convert Signal. Only a few external components are necessary as shown in Figure 11 and 12. The two typical interface circuits are for operating the SPT774 in either an unipolar or bipolar input mode. Further information is given in the following sections on these connections, but first a few conditions concerning board layout to achieve the best operation.

For each application of this device, strict attention must be given to power supply decoupling, board layout (to reduce pickup between analog and digital sections), and grounding. Digital timing, calibration and the analog signal source must be considered for correct operation.

To achieve specified accuracy, a double-sided printed circuit board with a copper ground plane on the component side is recommended. Keep analog signal traces away from digital lines. It is best to lay the PC board out such that there is an analog section and a digital section with a single point ground connection between the two through an RF bead located as close to the device as possible. If possible, run analog signals between ground traces and cross digital lines at right angles only.

POWER SUPPLIES

The supply voltages for the SPT774 must be kept as quiet as possible from noise pickup and also regulated from transients or drops. Because the part has 12-bit accuracy, voltage spikes on the supply lines can cause several LSB deviations on the output. Switching power supply noise can be a problem. Careful filtering and shielding should be employed to prevent the noise from being pickup by the converter.

Capacitor bypass pairs are needed from each supply pin to it's respective ground to filter noise and counter the problems caused by the variations in supply current. A 10 µF tantalum and a 0.1 µF ceramic type in parallel between V_{LOGIC} (pin 1) and digital common (pin 15), and V_{CC} (pin 7) and analog common (pin 9) is sufficient. V_{EE} is generated internally so pin 11 may be grounded or connected to a negative supply if the SPT774 is being used to upgrade an already existing design.

GROUNDING CONSIDERATIONS

Any ground path from the analog and digital ground should be as low resistance as possible to accommodate the ground currents present with this device.

The analog ground current is approximately 6 mADC while the digital ground is 3 mADC The analog and digital common pins should be tied together as close to the package as possible to guarantee best performance. The code dependent currents flow through the V_{LOGIC} and V_{CC} terminals and not through the analog and digital common pins.

The SPT774 may be operated by a µP or in the stand-alone mode. The part has four standard input ranges: 0 V to +10 V, 0 V to +20 V, ±5 V and ±10 V The maximum errors that are listed in the specifications for gain and offset may be adjusted externally to zero as explained in the next two sections.

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CALIBRATION AND CONNECTION PROCEDURES

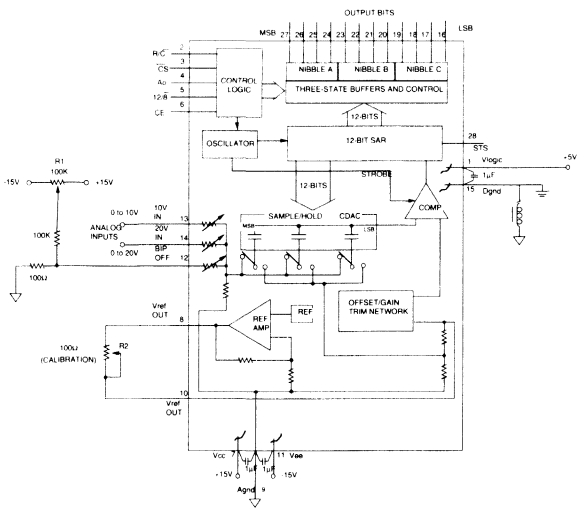
UNIPOLAR

The calibration procedure consists of adjusting the converter's most negative output to its ideal value for offset adjustment, and then adjusting the most positive output to its ideal value for gain adjustment.

Starting with offset adjustment and referring to Figure 11, the midpoint of the first LSB increment should be positioned at the origin to get an output code of all 0s. To do this, an input of +1/2 LSB or +1.22 mV for the 10 V range and +2.44 mV for the 20 V range should be applied to the SPT774. Adjust the offset potentiometer R1 for code transition flickers between 0000 0000 0000 and 0000 0000 0001.

The gain adjustment should be done at positive full scale. The ideal input corresponding to the last code change is applied. This is 1 and 1/2 LSB below the nominal full scale which is +9.9963 V for the 10 V range and +19.9927 V for the 20 V range. Adjust the gain potentiometer R2 for flicker between codes 1111 1111 1110 and 1111 1111 1111. If calibration is not necessary for the intended application, replace R2 with a 50 Ω, 1% metal film resister and remove the network from pin 12. Connect pin 12 to pin 9. Connect the analog input to pin 13 for the 0 V to 10 V range or to pin 14 for the 0 V to 20 V range.

Figure 11 - Unipolar Input Connections



BIPOLAR

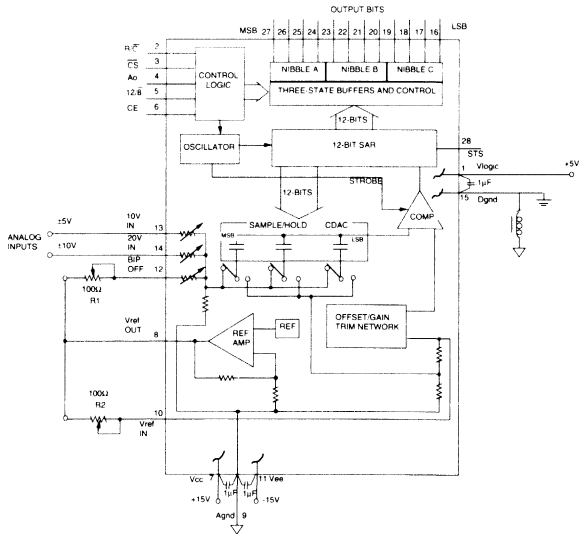
The gain and offset errors listed in the specification may be adjusted to zero using the potentiometers R1 and R2 (See Figure 12). If adjustment is not needed, either or both pots may be replaced by a 50 Ω, 1% metal film resistor.

To calibrate, connect the analog input signal to pin 13 for a ±5 V range or to pin 14 for a ±10 V range. First apply a DC input voltage 1/2 LSB above negative full scale which is -4.9988 V for the ±5 V range or -9.9976 V for the ±10 V range. Adjust the offset potentiometer R1 for flicker between output codes 0000 0000 0000 and 0000 0000 0001. Next, apply a DC input voltage 1 and 1/2 LSB below positive full scale which is +4.9963 V for the ±5 V range or +9.9927 V for the ±10 V range. Adjust the gain potentiometer R2 for flicker between codes 1111 1111 1110 and 1111 1111 1111.

ALTERNATIVE

In some applications, a full scale of 10.24 V (for an LSB of 2.5 mV) or 20.48 V (for an LSB of 5.0 mV) is more convenient. In the Unipolar mode of operation, replace R2 by 200 Ω potentiometer and add 150 Ω in series with pin 13 for 10.24 V input range or 500 Ω in series with pin 14 for 20.48 V input range. In bipolar mode of operation, replace R1 by 500 Ω potentiometer (in addition to the previous changes). The calibration will remain similar to the standard calibration procedure.

Figure 12 - Bipolar Input Connections



CONTROLLING THE SPT774

The SPT774 can be operated by most microprocessor systems due to the control input pins and on-chip logic. It may also be operated in the "stand-alone" mode and enabled by the R/$\overline{C}$ input pin. Full µP control consists of selecting an 8 or 12-bit conversion cycle, initiating the conversion, and reading the output data when ready. The output read has the options of choosing either 12-bits at once or 8 following by 4-bits in a left-justified format. All five control inputs are TTL/CMOS compatible and include 12/$\overline{8}$, $\overline{CS}$, Ao, R/$\overline{C}$ and CE. The use of these inputs in controlling the converter's operations is shown in Table I, and the internal control logic is shown in a simplified schematic in Figure 14.

STAND-ALONE OPERATION

The simplest interface is a control line connected to R/$\overline{C}$. The other controls must be tied to known states as follows: CE and 12/$\overline{8}$ are wired high, Ao and $\overline{CS}$ are wired low. The output controls must be tied to known states as follows: CE and 12/$\overline{8}$ are wired high, Ao and $\overline{CS}$ are wired low. The output data arrives in words of 12-bits each. The limits on R/$\overline{C}$ duty cycle are shown in Figures 3 and 4. It may have a duty cycle within and including the extremes shown in the specifications on the pages. In general, data may be read when R/$\overline{C}$ is high unless STS is also high, indicating a conversion is in progress.

Figure 13 - Interfacing the SPT774 to an 8-bit Data Bus

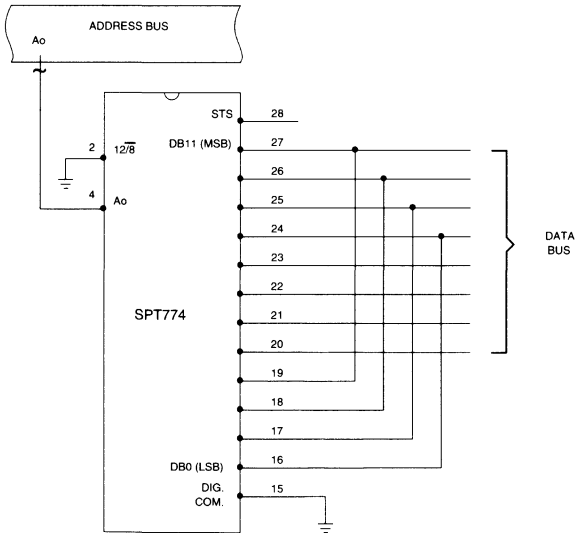


Table I - Truth Table for the SPT774 Control Inputs

CE	$\overline{CS}$	R/$\overline{C}$	12/$\overline{8}$	Ao	Operation
0	X	X	X	X	None
X	1	X	X	X	None
↑	0	0	X	0	Initiate 12 bit conversion
↑	0	0	X	1	Initiate 8 bit conversion
1	↓	0	X	0	Initiate 12 bit conversion
1	↓	0	X	1	Initiate 8 bit conversion
1	0	↓	X	0	Initiate 12 bit conversion
1	0	↓	X	1	Initiate 8 bit conversion
1	0	1	1	X	Enable 12 bit Output
1	0	1	0	0	Enable 8 MSB's Only
1	0	1	0	1	Enable 4 LSB's Plus 4 Trailing Zeroes

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CONVERSION LENGTH

A conversion start transition latches the state of Ao as shown in Figure 13 and Table I. The latched state determines if the conversion stops with 8-bit (Ao high) or continues for 12-bits (Ao low). If all 12-bits are read following an 8-bit conversion, the three LSB's will be a logic "0" and DB3 will be a logic "1". Ao is latched because it is also involved in enabling the output buffers as will be explained later. No other control inputs are latched.

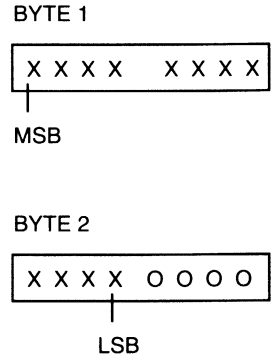
CONVERSION START

A conversion may be initiated by a logic transition on any of the three inputs: CE, $\overline{CS}$, R/$\overline{C}$, as shown in Table I. The last of the three to reach the correct state starts the conversions, so one, two or all three may be dynamically controlled. The nominal delay from each is the same and all three may change state simultaneously. In order to assure that a particular input controls the start of conversion, the other two should be setup at least 50 ns earlier. Refer to the convert mode timing specifications. The Convert Start timing diagram is illustrated in Figure 1.

The output signal STS is the status flag and goes high only when a conversion is in progress. While STS is high, the output buffers remain in a high impedance state so that data can not be read. Also, when STS is high, an additional Start Convert will not reset the converter or reinitiate a conversion. Note, if Ao changes state after a conversion begins, an additional Start Convert command will latch the new start of Ao and possible cause a wrong cycle length for that conversion (8 versus 12-bits).

READING THE OUTPUT DATA

The output data buffers remain in a high impedance state until the following four conditions are met: R/$\overline{C}$ is high, STS is low, CE is high, and $\overline{CS}$ is low. That data lines become active in response to the four conditions and output data according to the conditions of 12/$\overline{8}$ and Ao. The timing diagram for this process is shown in Figure 2. When 12/$\overline{8}$ is high, all 12 data outputs become active simultaneously and the Ao input is ignored. This is for easy interface to a 12 or 16-bit data bus. The 12/$\overline{8}$ input is usually tied high or low, although it is TTL/CMOS compatible. When 12/$\overline{8}$ is low, the output is separated into two 8-bit bytes as shown below:



This configuration makes it easy to connect to an 8-bit data bus as shown in Figure 13. The Ao control can be connected to the least significant bit of the address bus in order to store the output data into two consecutive memory locations. When Ao is pulled low, the 8 MSBs are enabled only. When Ao is high, the 4 MSBs are disabled, bits 4 through 7 are forced to a zero and the four LSBs are enabled. The two byte format is "left justified data" as shown above and can be considered to have a decimal point or binary to the left of byte 1.

Ao may be toggled without damage to the converter at any time. Break-before-make action is guaranteed between the two data bytes. This assures that the outputs which are strapped together in Figure 13 will never be enabled at the same time.

In Figure 2, it can be seen that a read operation usually begins after the conversion is completed and STS is low. If earlier access is needed, the read can begin no later than the addition of time t_{DD} and t_{HS} before STS goes low.

Figure 14 - Control Logic

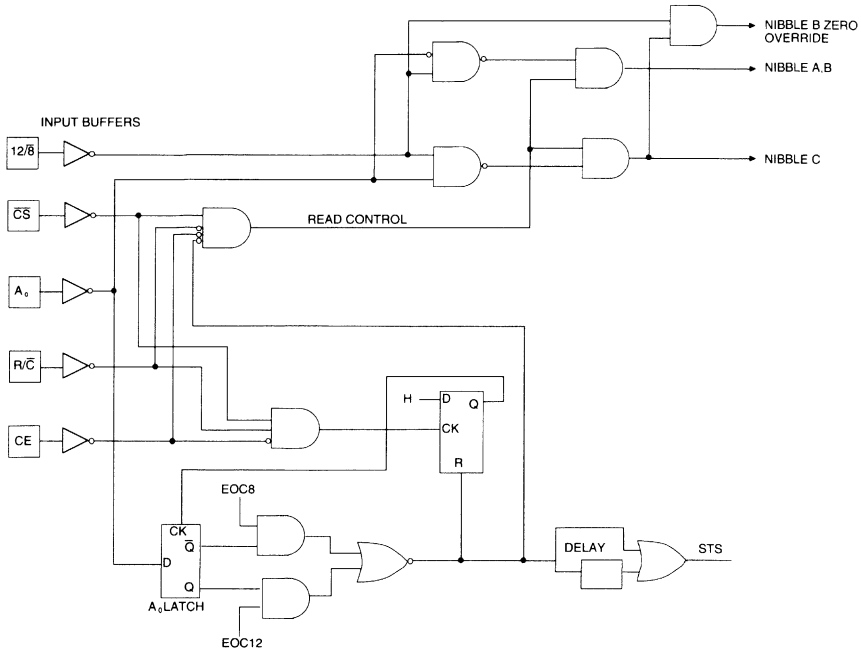
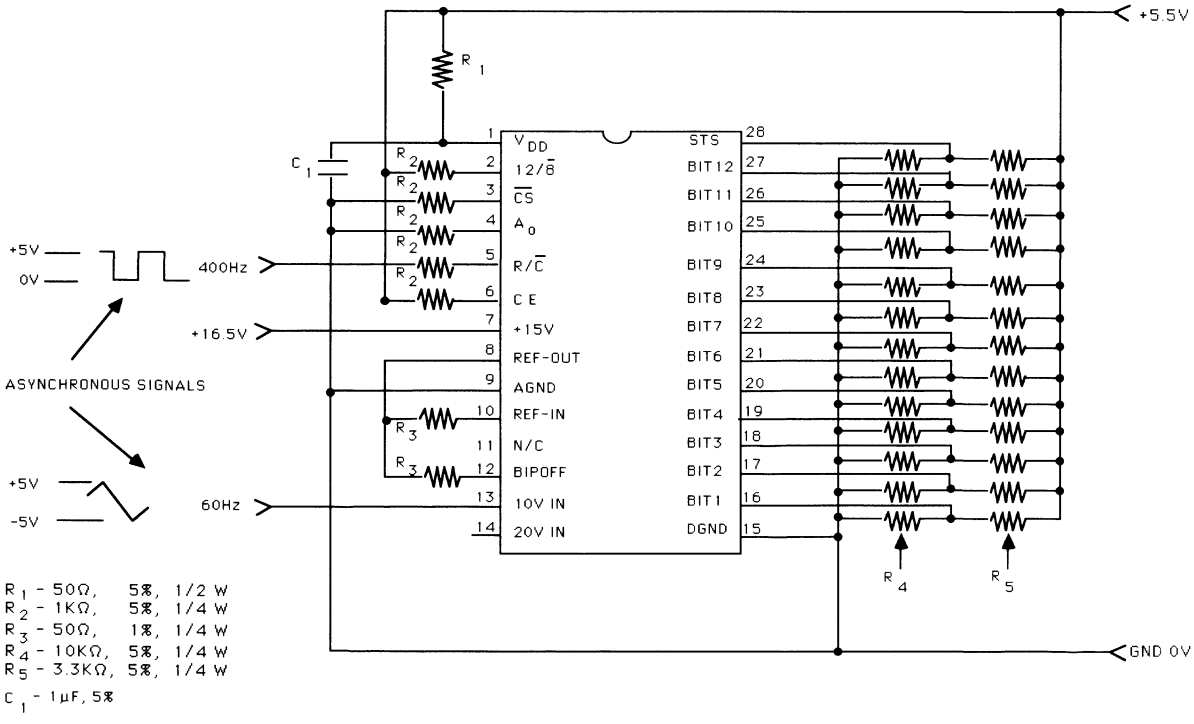


Figure 15 - Burn-In Schematic



R_1 - 50Ω, 5%, 1/2 W
R_2 - 1KΩ, 5%, 1/4 W
R_3 - 50Ω, 1%, 1/4 W
R_4 - 10KΩ, 5%, 1/4 W
R_5 - 3.3KΩ, 5%, 1/4 W
C_1 - 1μF, 5%

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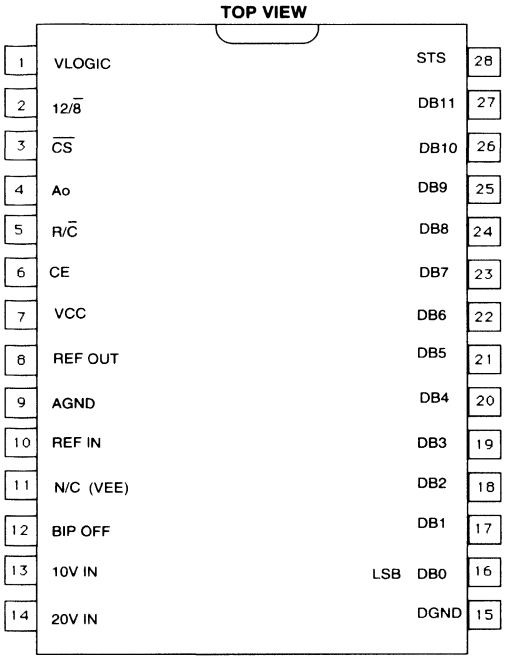
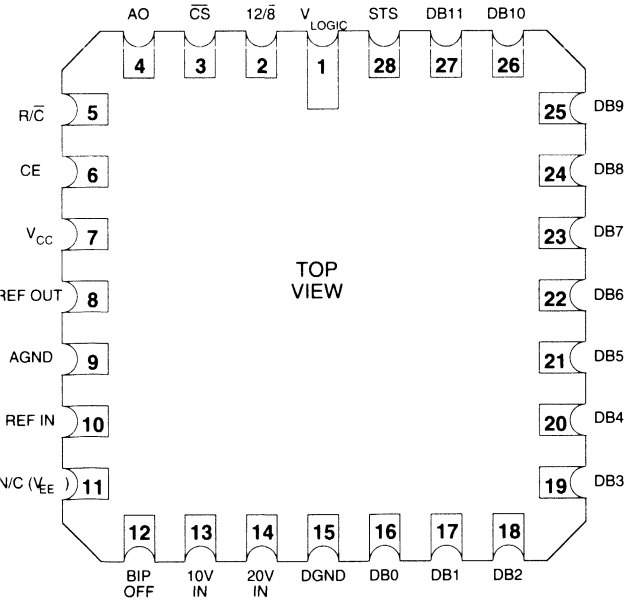
PIN Assignment SPT774



28-LEAD DIP



28-LEAD LCC

PIN Functions SPT774

NAME	FUNCTION
V_{LOGIC}	Logic Supply Voltage, Nominally +5 V
12/$\overline{8}$	Data Mode Selection
$\overline{CS}$	Chip Selection
Ao	Byte Address/Short Cycle
R/$\overline{C}$	Read/Convert
CE	Chip Enable
V_{CC}	Analog Positive Supply Voltage, Nominally +15 V
REF OUT	Reference Output, Nominally +10 V
AGND*	Analog Ground
REF IN	Reference Input
N/C (V_{EE})	This pin is not connected to the device.
BIP OFF	Bipolar Offset
10 V IN	10 Volt Analog Input
20 V IN	20 Volt Analog Input
DGND	Digital Ground
DB0 - DB11	Digital Data Output DB11 - MSB DB0 - LSB
STS	Status

* The lid on the sidebrazed and LCC packages are internally connected to AGND.

LEADERSHIP IN DATA CONVERSION AND SIGNAL PROCESSING

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SIGNAL PROCESSING TECHNOLOGIES

SPT1175

8-BIT, 40 MSPS CMOS A/D CONVERTER

PRELIMINARY INFORMATION

3

FEATURES

- 40 MSPS Maximum Conversion Rate
- Internal Sample-and-Hold Function
- 90 mW Power Dissipation at 20 MSPS
- Internal Voltage Reference
- Single +5.0 V Power Supply
- Three-State TTL-Outputs
- TTL/CMOS Compatible

APPLICATIONS

- Video Digitizing
- Image Scanners
- Personal Computer Video
- Medical Ultrasound
- Multimedia
- Digital Television

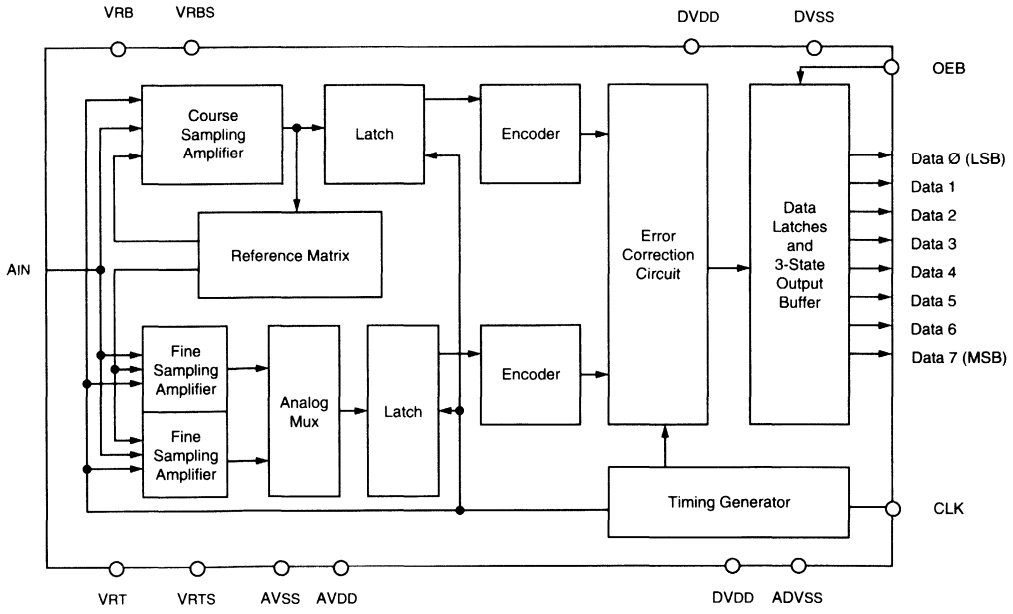
GENERAL DESCRIPTION

The SPT1175 is a CMOS two-step A/D converter capable of digitizing full scale analog input signals into 8-bit digital words at a sample rate of 40 MSPS.

For most applications, no external sample-and-hold or video driving amplifiers are required due to the device's narrow aperture time, wide bandwidth, and low input capacitance.

The SPT1175 operates from a single +5.0 V power supply and has an internal voltage reference which eliminates the need for external reference circuitry. All digital inputs and three-state outputs are TTL-compatible. The SPT1175 is ideal for most video and image processing applications that require low power dissipation and low cost. The SPT1175 is available in 24-lead plastic SOIC, 24-pin plastic DIP and die form.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Beyond which damage may occur)[1] 25 °C

Supply Voltages
V_{DD} ..... -0.5 to +7.0 V

Input Voltages
Analog Input ..... V_{SS} to V_{DD}
Reference Input Voltage ..... V_{SS} to V_{DD}
ESD Susceptibility[2] ..... ±2,000 V

Temperature
Operating Temperature ..... 0 to +70 °C
Junction Temperature ..... 175 °C
Lead Temperature, (soldering 10 seconds) ..... 300 °C
Storage Temperature ..... -55 to +125 °C

Notes: 1. Operation at any Absolute Maximum Rating is not implied. See Electrical Specifications for proper nominal applied conditions in typical applications.
2. 100 pF discharged through a 1.5 kΩ resistor (human body model).

ELECTRICAL SPECIFICATIONS

T_A= +25 °C, AV_{DD}=DV_{DD}=+5.0 V, AV_{SS}=DV_{SS}=0.0 V, V_{RB}=+0.6 V and V_{RT}=+2.6 V, unless otherwise specified.

PARAMETERS	TEST CONDITIONS	TEST LEVEL	MIN	TYP	MAX	UNITS
Resolution			8			Bits
DC Accuracy (+25 °C)						
Integral Nonlinearity		I		±0.8	±1.2	LSB
Differential Nonlinearity		I		±0.6	±1.0	LSB
No Missing Codes		I		Guaranteed		
Analog Input						
Input Voltage Range		I	VRB		VRT	V
Input Bias Current		I			±5.0	µA
Input Resistance		VI	100	200		kΩ
Input Capacitance		V		15		pF
Input Bandwidth		V	12			MHz
Reference Input						
Reference Ladder Resistance		I	200	300	400	Ω
Reference Current		I	5.0	6.7	10.0	mA
Reference Input Voltage	VRB	I	0	0.6	-	V
	VRT	I	-	2.6	2.8	V
Internal Bias	Short VRT and VRTS	I	2.5	2.6	2.7	V
	Short VRB and VRBS	I	0.55	0.60	0.65	V
Offset Voltage Error						
Top		I	-18	-25	-68	mV
Bottom		I	0	10	40	mV
Timing Characteristics						
Maximum Conversion Rate	1 MHz Sine Wave	I	40			MSPS
Overvoltage Recovery Time		V		25		ns
Output Delay (TdisL, TdisH)	(High 'Z')	IV			100	ns
Aperture Jitter Time		V		25		ps-RMS
Output Delay Time (td)	1 TTL +15 pF Load	V		16		ns
Output Enable Time	(TenH, TenL)	IV			100	ns

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ELECTRICAL SPECIFICATIONS

T_A=+25 °C, AV_{DD}=DV_{DD}=+5.0 V, AV_{SS}=DVss=0.0 V, V_{RB}=+0.6 V and V_{RT}=+2.6 V, unless otherwise specified.

PARAMETERS	TEST CONDITIONS	TEST LEVEL	MIN	TYP	MAX	UNITS
Dynamic Performance						
Signal-To-Noise Ratio	fs= 20 MSPS					
$f$in=1.0 MHz		I		45		dB
$f$in=3.58 MHz		I		45		dB
$f$in=10 MHz		I		41		dB
Spurious Free						
Dynamic Range	fs= 20 MSPS					
$f$in=1.0 MHz		V		45		dB
$f$in=3.58 MHz		V		40		dB
$f$in=10 MHz		V		34		dB
Differential Phase	NTSC 20 IRE Mod Ramp	I		0.7		Degrees
Differential Gain	fs= 14.3 MSPS	I		1.0		%
Digital Inputs						
Input Current, Logic High		I			1.0	µA
Input Current, Logic Low		I			1.0	µA
Pulse Width High (CLK)		IV	15			ns
Pulse Width Low (CLK)		IV	15			ns
Voltage, Logic High		I	4.0			V
Voltage, Logic Low		I			1.0	V
Digital Outputs						
Short Circuit Current		I			30	mA
Output Current, High		I	-1.1			mA
Output Current, Low		I	3.5			µA
Output Current, High 'Z'		I			16	µA
Voltage High		I	4.0			V
Voltage Low		I			0.4	V
Power Supply Requirements						
AV_{DD} (Analog Supply Voltage)		IV	+4.75	+5.0	+5.25	V
DV_{DD} (Digital Supply Voltage)		IV	+4.75	+5.0	+5.25	V
Supply Current		I		18	27	mA
Power Dissipation	fs=20 MSPS	I		90	135	mW

TEST LEVEL CODES

All electrical characteristics are subject to the following conditions:

All parameters having min/max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality Assurance inspection. Any blank section in the data column indicates that the specification is not tested at the specified condition.

Unless otherwise noted, all tests are pulsed tests; therefore, $T_J = T_C = T_A$.

TEST LEVEL	TEST PROCEDURE
I	100% production tested at the specified temperature.
II	100% production tested at T_A=25 °C, and sample tested at the specified temperatures.
III	QA sample tested only at the specified temperatures.
IV	Parameter is guaranteed (but not tested) by design and characterization data.
V	Parameter is a typical value for information purposes only.
VI	100% production tested at T_A = 25 °C. Parameter is guaranteed over specified temperature range.

Table 1 - Output Coding

INDEX	ANALOG INPUT (V)	DIGITAL OUTPUT	
0	0.6078125	00000000	
1	0.6078125 ~ 0.6156260	00000001	V_{RB}=0.6 V
2	0.6156250 ~ 0.6234375	00000010	V_{RT}=2.6 V
....	....	....	
123	1.5921875 ~ 1.6000000	01111111	1 LSB=7.8125 mV
124	1.6000000 ~ 1.6078125	10000000	
125	1.6078125 ~ 1.6156250	10000001	
....	....	....	
254	2.5843750 ~2.5921875	11111110	
255	2.5921875 ~	11111111	

Figure 1A: Timing Diagram

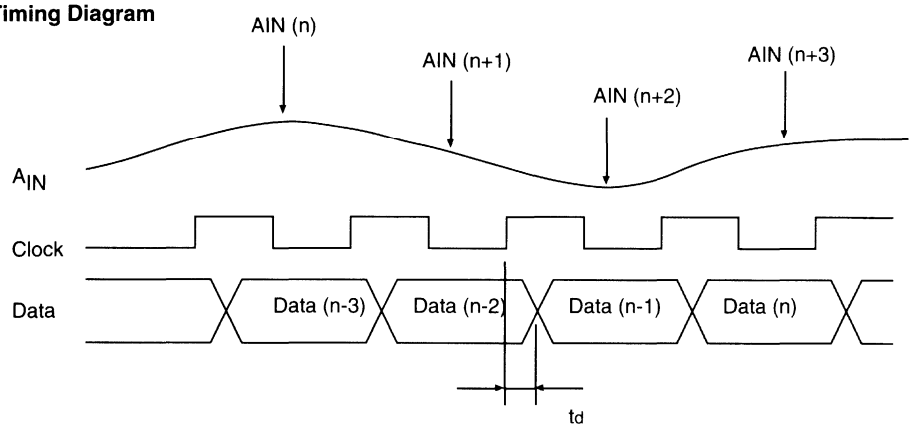
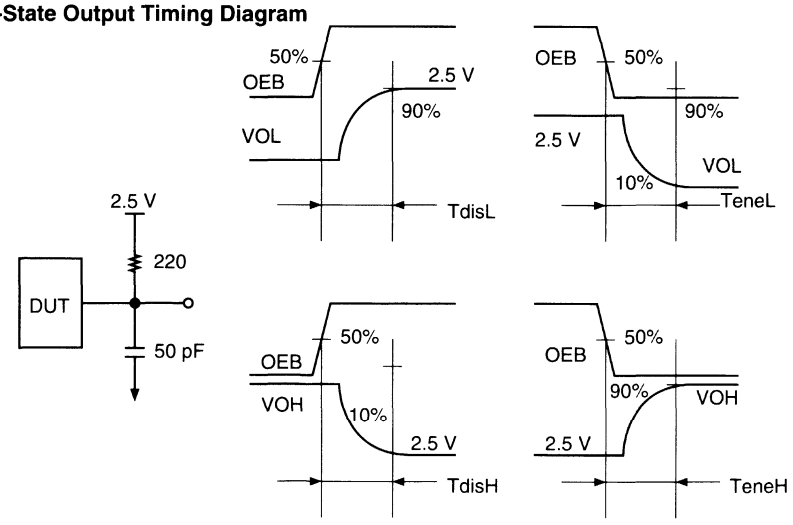


Figure 1B: Tri-State Output Timing Diagram



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TYPICAL INTERFACE CIRCUIT

The SPT1175 is an 8-bit analog-to-digital converter which uses a two-step, ping-pong architecture to perform conversions up to 40 MSPS. Figure 2 shows the typical interface requirements when using the SPT1175 in normal operation. The following sections describe the function and operation of the device.

POWER SUPPLIES AND GROUNDING

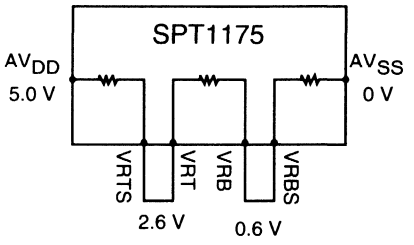
The SPT1175 operates from a single +5 V power supply. To reduce noise effects, separate the analog and digital systems close to the device. Each power supply pin should be bypassed as closely as possible to the device. For optimal performance, both the AGND and DGND should be connected to the system's analog ground plane.

ANALOG INPUT AND VOLTAGE REFERENCE

The SPT1175 input voltage range is VRT<V_{IN}<VRB. Two reference voltages (VRT and VRB) are required for device operation. These voltages may be generated externally or the SPT1175's internal reference may be used.

Inside the SPT1175, reference resistors are placed between AV_{DD} and VRTS and between AV_{SS} and VRBS so that VRTS and VRBS generate the 2.6 V and 0.6 V references respectively. (See figure 3.) In order to utilize the internal self-bias reference voltage, VRTS is to be shorted with VRT and the VRBS pin is to be shorted to the VRB pin. The self-bias internal reference is not as stable over temperature and supply variations as externally generated reference voltages but will perform well in many commercial video applications.

Figure 3 - Reference Circuit Diagram



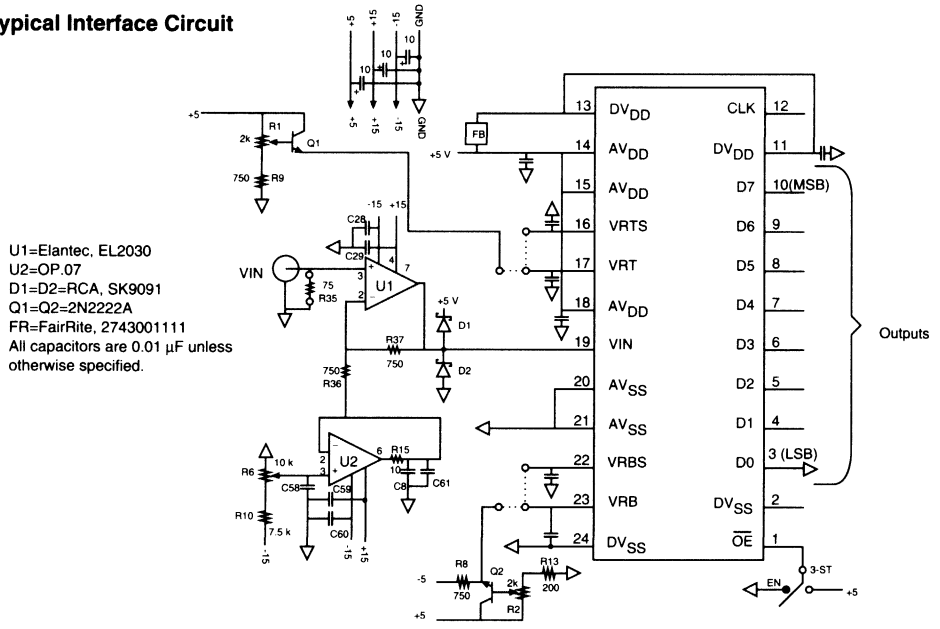
DIGITAL INPUTS AND OUTPUTS

The analog input is sampled and tracked on the first 'H' cycle of the external clock and is held from the falling edge of CLK. The output remains valid (output hold time), and the new data becomes valid (output delay time) after the rising edge of CLK, delayed by 2.5 clock cycles.

EVALUATION BOARD

The EB1175 evaluation board is available to aid designers in demonstrating the full performance of the SPT1175. This board includes a reference circuit, clock driver circuit, output data latches, and an on-board reconstruction DAC. An application note describing the operation of the board is available. Contact the factory for price and delivery.

Figure 2 - Typical Interface Circuit



LEADERSHIP IN DATA CONVERSION AND SIGNAL PROCESSING

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SIGNAL PROCESSING TECHNOLOGIES

SPT7710

8-BIT, 150 MSPS FLASH A/D CONVERTER

PRELIMINARY INFORMATION

3

FEATURES

- Metastable Errors Reduced to 1 LSB
- Low Input Capacitance - 10 pF
- Wide Input Bandwidth - 210 MHz
- 150 MSPS Conversion Rate
- Typical Power Dissipation <2 Watts

APPLICATIONS

- Digital Oscilloscopes
- Transient Capture
- Radar, EW, ECM
- Direct RF Down-conversion
- Medical Electronics: Ultrasound, CAT Instrumentation

GENERAL DESCRIPTION

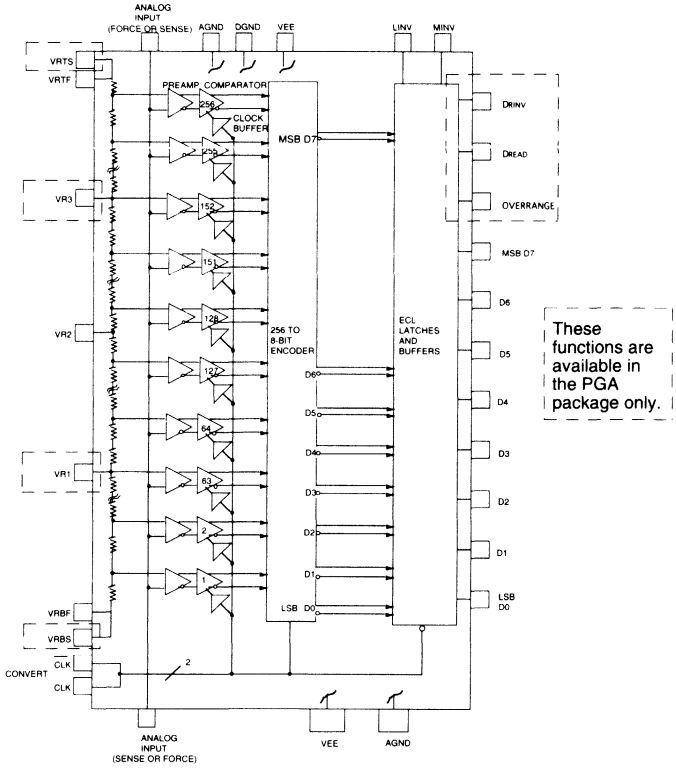
The SPT7710 is a monolithic flash A/D converter capable of digitizing a two volt analog input signal into 8-bit digital words at a 150 MSPS (TYP) update rate.

For most applications, no external sample-and-hold is required for accurate conversion due to the device's narrow aperture time, wide bandwidth, and low input capacitance. A single standard -5.2 volt power supply is required for operation of the SPT7710, with nominal power dissipation of 2 W.

A proprietary decoding scheme reduces metastable errors to the 1 LSB level.

The part is packaged in a 42L ceramic sidebrazed DIP which is pin compatible with the CX20116 and CXA1396D. A 46L PGA package is also available which allows access to additional reference ladder taps, an overrange bit, and a data ready output. The SPT7710 is available in an industrial temperature range. Contact the factory for military temperature range and surface-mount package options.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Beyond which damage may occur)[1] 25 °C

Supply Voltages
- Negative Supply Voltage (V_{EE} TO GND) ..... -7.0 to +0.5 V
- Ground Voltage Differential ..... -0.5 to +0.5 V

Input Voltage
- Analog Input Voltage ..... +0.5 V to V_{EE}
- Reference Input Voltage ..... +0.5 V to V_{EE}
- Digital Input Voltage ..... +0.5 V to V_{EE}
- Reference Current VRTF to VRBF ..... 25 mA

Output
- Digital Output Current ..... 0 to -25 mA

Temperature
- Operating Temperature, ambient ..... -25 to +85 °C
- junction ..... +150 °C
- Lead Temperature, (soldering 10 seconds). ..... +300 °C
- Storage Temperature ..... -65 to +150 °C

Notes: 1. Operation at any Absolute Maximum Rating is not implied. See Electrical Specifications for proper nominal applied conditions in typical applications.

ELECTRICAL SPECIFICATIONS

$T_A=T_{MIN}$ to T_{MAX}, V_{EE}=-5.2 V, R_{Source}=50 Ω, V_{RBF}=-2.00 V, V_{R2}=-1.0 V, V_{RTF}=0.00 V, f_{clk}=125 MHz, Duty Cycle=50%, unless otherwise specified.

PARAMETERS	TEST CONDITIONS	TEST LEVEL	SPT7710A MIN	SPT7710A TYP	SPT7710A MAX	SPT7710B MIN	SPT7710B TYP	SPT7710B MAX	UNITS
DC ELECTRICAL CHARACTERISTICS									
Integral Linearity		II	-0.75		+0.75	-0.95		+0.95	LSB
Differential Linearity (No missing codes guaranteed)		II	-0.75		+0.75	-0.95		+0.95	LSB
Offset Error VRT		II	-30		+30	-30		+30	mV
Offset Error VRB		II	-30		+30	-30		+30	mV
Input Voltage Range		II	-2		0.0	-2		0.0	Volts
Input Capacitance	Over full input range	V		10			10		pF
Input Resistance		V		70			70		kΩ
Input Current		II		250	500		250	500	µA
Clock Synchronous Input Currents		V		40			40		µA
Supply Current	T_A=25 °C	II		400	500		400	500	mA
Power Dissipation	T_A=25 °C	II		2.0	2.6		2.0	2.6	W
Ladder Resistance		II	100	200	300	100	200	300	Ω
Reference Bandwidth		V		10			10		MHz
Digital Output High Voltage	50 Ω to -2 V	II	-1.1	-0.9	-0.7	-1.1	-0.9	-0.7	Volts
Digital Output Low Voltage	50 Ω to -2 V	II	-1.95	-1.8	-1.5	-1.95	-1.8	-1.5	Volts
Digital Input High Voltage (MINV, LINV)		II	-1.1		-0.7	-1.1		-0.7	Volts
Digital Input Low Voltage (MINV, LINV)		II	-2.0		-1.5	-2.0		-1.5	Volts

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ELECTRICAL SPECIFICATIONS

T_A=+25 °C, V_{EE}=-5.2 V, R_{Source}=50 Ω, V_{RBF}=-2.00 V, V_{R2}=-1.0 V, V_{RTF}=0.00 V, f_{clk}=125 MHz, Duty Cycle=50%, unless otherwise specified.

PARAMETERS	TEST CONDITIONS	TEST LEVEL	SPT7710A MIN	SPT7710A TYP	SPT7710A MAX	SPT7710B MIN	SPT7710B TYP	SPT7710B MAX	UNITS
AC ELECTRICAL CHARACTERISTICS									
Maximum Sample Rate		I	125	150		125	150		MSPS
Clock Low Width, TPW0		I	4	3		4	3		ns
Clock High Width, TPW1		I	4	3		4	3		ns
Output Delay (TD)		V		2.0			2.0		ns
Output Delay TEMPCO		V		1			1		ps/°C
Data-to-Data Ready Delay		V		4.5			4.5		ns
Large Signal Bandwidth	V_{IN}=F.S.	V		210			210		MHz
Small Signal Bandwidth	V_{IN}=500 mV P-P	V		335			335		MHz
Aperture Jitter		V		5			5		ps
Acquisition Time		V		1.5			1.5		ns
Input Slew Rate		V		1,000			1,000		V/µs
Total Dynamic Error	F_{IN} = 3.58 MHz F_{IN} = 50 MHz	I I	44 38	48 42		44 38	48 42		dB dB
Signal-to-Noise Ratio	F_{IN} = 3.58 MHz F_{IN} = 50 MHz	I I	46 40	49 45		46 40	49 45		dB dB
Total Harmonic Distortion	F_{IN} = 3.58 MHz F_{IN} = 50 MHz	I I	47 40	48 44		47 40	46 44		dBc dBc

TEST LEVEL CODES

All electrical characteristics are subject to the following conditions:

All parameters having min/max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality Assurance inspection. Any blank section in the data column indicates that the specification is not tested at the specified condition.

Unless otherwise noted, all tests are pulsed tests; therefore, $T_J = T_C = T_A$.

TEST LEVEL	TEST PROCEDURE
I	100% production tested at the specified temperature.
II	100% production tested at T_A=25 °C, and sample tested at the specified temperatures.
III	QA sample tested only at the specified temperatures.
IV	Parameter is guaranteed (but not tested) by design and characterization data.
V	Parameter is a typical value for information purposes only.
VI	100% production tested at T_A = 25 °C. Parameter is guaranteed over specified temperature range.

GENERAL DESCRIPTION

The SPT7710 is a fast monolithic 8-bit parallel flash A/D converter. The nominal conversion rate is 150 MSPS and the analog bandwidth is in excess of 200 MHz. A major advance over previous flash converters is the inclusion of 256 input preamplifiers between the reference ladder and input comparators. (See block diagram.) This not only reduces clock transient kickback to the input and reference ladder due to a low AC beta but also reduces the effect of the dynamic state of the input signal on the latching characteristics of the input comparators. The preamplifiers act as buffers and stabilize the input capacitance so that it remains constant over different input voltages and frequency ranges and therefore makes the part easier to drive than previous flash converters. The SPT7710 incorporates a proprietary decoding scheme that reduces metastable errors (sparkle codes or *flyers*) to a maximum of 1 LSB.

The SPT7710 has true differential analog and digital data paths from the preamplifiers to the output buffers (Current Mode Logic) for reducing potential missing codes while rejecting common mode noise.

Signature errors are also reduced by careful layout of the analog circuitry. Every comparator also has a clock buffer to reduce differential delays and to improve signal-to-noise ratio. The output drive capability of the device can provide full ECL swings into 50 Ω loads.

TYPICAL INTERFACE CIRCUIT

The typical interface circuit is shown in figure 1. The SPT7710 is relatively easy to apply depending on the accuracy needed in the intended application. Wire-wrap may be employed with careful point-to-point ground connections if desired, but to achieve the best operation, a double sided PC board with a ground plane on the component side separated into digital and analog sections will give the best performance. The converter is bonded-out to place the digital pins on the left side of the package and the analog pins on the right side. Additionally, an RF bead connection through a single point from the analog to digital ground planes will reduce ground noise pickup.

The circuit in Figure 2 (PGA Package only) is intended to show the most elaborate method of achieving the least error by correcting for integral linearity, input induced distortion, and power supply/ground noise. This is achieved by the use of external reference ladder tap connections, input buffer and supply decoupling. The function of each pin and external connections to other components is as follows:

Figure 1 - SPT7710 Typical Interface Circuit 1

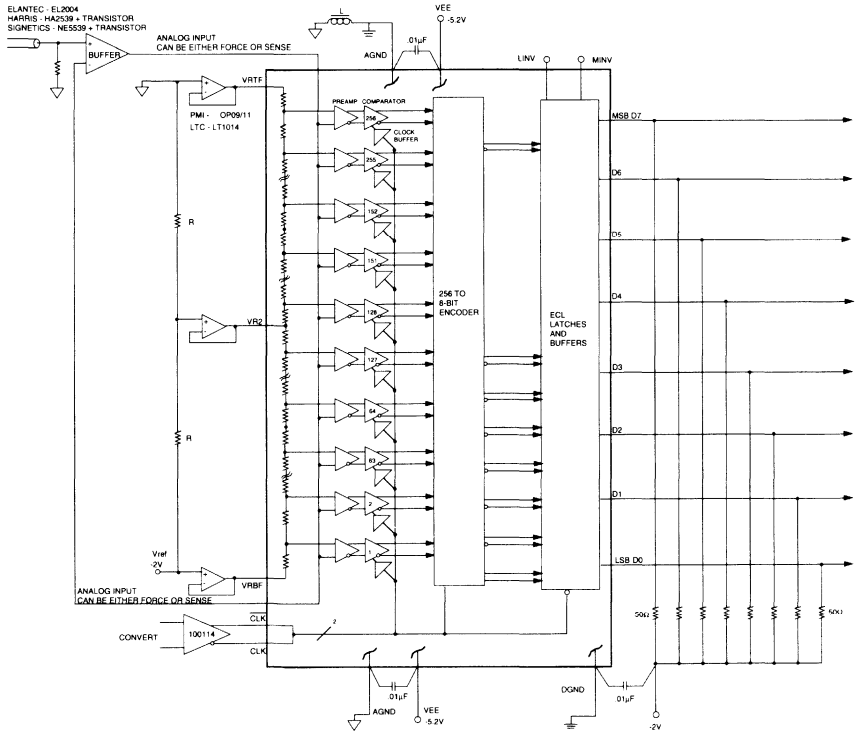

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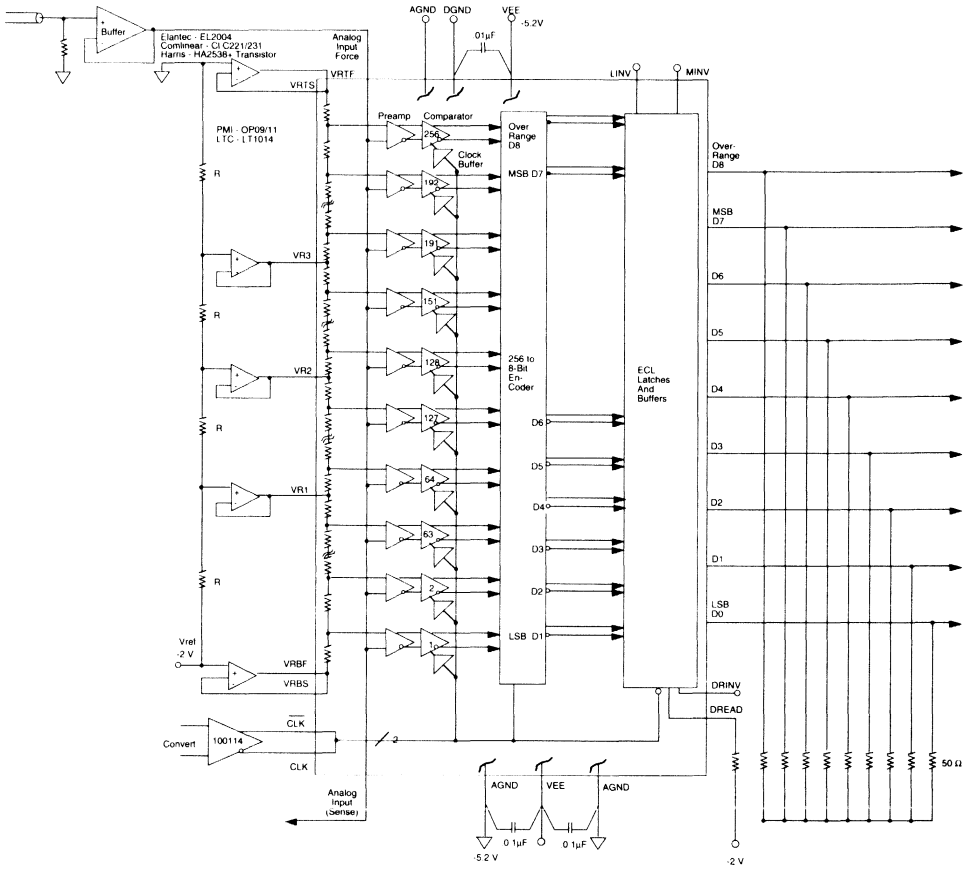
Figure 2 - SPT7710 Typical Interface Circuit 2 (PGA Package Only)



V_{EE}, AGND, DGND

V_{EE} is the supply pin with AGND as ground for the device. The power supply pins should be bypassed as close to the device as possible with at least a .01 µF ceramic capacitor. A 1 µF tantalum can also be used for low frequency suppression. DGND is the ground for the ECL outputs and is to be referenced to the output pulldown voltage and appropriately bypassed as shown in Figure 1.

VIN (ANALOG INPUT)

There are two analog input pins that are tied to the same point internally. Either one may be used as an analog input *sense* and the other for input *force*. This is convenient for testing the source signal to see if there is sufficient drive capability. The pins can also be tied together and driven by the same source. The SPT7710 is superior to similar devices due to a preamplifier stage before the comparators. This makes the device easier to drive because it has constant capacitance and induces less slew rate distortion. If an input buffer is needed, a Harris HA2540 may be used in conjunction with an output transistor buffer for lower frequency applications. For higher frequencies, another option is to use an Elantec EL2004 video buffer or an HA2539 and a 2N5836 transistor. Very high performance can be achieved by using a Comlinear CLC221/231.

CLK, $\overline{CLK}$ (CLOCK INPUTS)

The clock inputs are designed to be driven differentially with ECL levels. The clock may be driven single-ended since $\overline{CLK}$ is internally biased to -1.3 V. (See clock input circuit.) $\overline{CLK}$ may be left open but a .01 µF bypass capacitor from $\overline{CLK}$ to AGND is recommended. NOTE: System performance may be degraded due to increased clock noise or jitter.

MINV, LINV (OUTPUT LOGIC CONTROL)

These are ECL-compatible digital controls for changing the output code from straight binary to two's complement, etc. For more information, see Table I. Both MINV and LINV are in the logic low (0) state when they are left open. The high state can be obtained by tying to AGND through a diode or 3.9 kΩ resistor.

Table I - Output Coding

	MINV	0	0	1	1
	LINV	0	1	0	1
	0V	111...11	100...00	011...11	000...00
	.	111...10	100...01	011...10	000...01
	.	.	.	.	.
	.	.	.	.	.
	.	.	.	.	.
V_{IN}	.	100...00	111...11	000...00	011...11
	.	011...11	000...00	111...11	100...00
	.	.	.	.	.
	.	.	.	.	.
	.	.	.	.	.
	.	000...01	011...10	100...01	111...10
	-2V	000...00	011...11	100...00	111...11

1: V_{IH}, V_{OH} 0: V_{IL}, V_{OL}

D0 TO D7 (DIGITAL OUTPUTS)

The digital outputs can driveECL levels into 50 Ωs when pulled down to -2 V. When pulled down to -5.2 V, the outputs can drive 130 Ω to 1 kΩ loads.

VRBF, VR2, VRTF (REFERENCE INPUTS)

There are two reference inputs and one external reference voltage tap. These are -2 V (VRBF), mid-tap (VR2) and AGND (VRTF). The reference pins and tap can be can be driven by op amps as shown in Figure 1 or VR2 may be bypassed for limited temperature operation. These voltage inputs can be bypassed to AGND for further noise suppression if desired.

VRBF, VRBS, VR1, VR2, VR3, VRTF, VRTS REFERENCE INPUTS *(PGA PACKAGE ONLY)*

These are five external reference voltage taps from -2 V (VRBF) to AGND (VRTF) which can be used to control integral linearity over temperature. The taps can be driven by op amps as shown in figure 2. These voltage level inputs can be bypassed to AGND for further noise suppression if so desired. VRB and VRT have "force" and "sense" pins for monitoring the top and bottom voltage references.

DREAD - DATA READY, DRINV - DATA READY INVERSE *(PGA PACKAGE ONLY)*

The data ready pin is a flag that goes high or low at the output when data is valid or ready to be received. It is essentially a delay line that accounts for the time necessary for information to be clocked through the SPT7710's decoders and latches. This function is useful for interfacing with high speed memory. Using the data ready output to latch the output data ensures minimum setup and hold times. DRINV is a data ready inverse control pin (see Timing Diagram).

D8 - OVERRANGE *(PGA PACKAGE ONLY)*

This is an overrange function. When the SPT7710 is in an overrange condition, D8 goes high and all data outputs go high as well. This makes it possible to include the SPT7710 into higher resolution systems.

N/C

All *Not Connected* pins should be tied to DGND on the left side of the package and to AGND of the right side of the package.

OPERATION

The SPT7710 has 256 preamp/comparator pairs which are each supplied with the voltage from VRTF to VRBF divided equally by the resistive ladder as shown in the block diagram. This voltage is applied to the positive input of each preamplifier/comparator pair. An analog input voltage applied at VIN is connected to the negative inputs of each preamplifier/comparator pair. The comparators are then clocked through each comparator's individual clock buffer. When the CLK pin is in the low state, the master or input stage of the comparators compares the analog input voltage to the respective reference voltage. When the CLK pin changes from low to high, the comparators are latched to the state prior to the clock transition and output logic codes in sequence from the top comparators, closest to VRTF (0 V), down to the point where the magnitude of the input signal changes sign (thermometer code). The output of each comparator is then registered into four 64-to-6 bit decoders when the CLK is changed from high to low. At the output of the decoders is a set of four 7-bit latches which are enabled (*track*) when the clock changes from high to low. From here, the outputs of the latches are coded into 6 LSBs from 4 columns and 4 columns are coded into 2 MSBs. Next are the MINV and LINV controls for output inversions which consist of a set of eight XOR gates. Finally, 8 ECL output latches and buffers are used to drive the external loads. The conversion takes one clock cycle from the input to the data outputs.

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Figure 3 - Timing Diagram

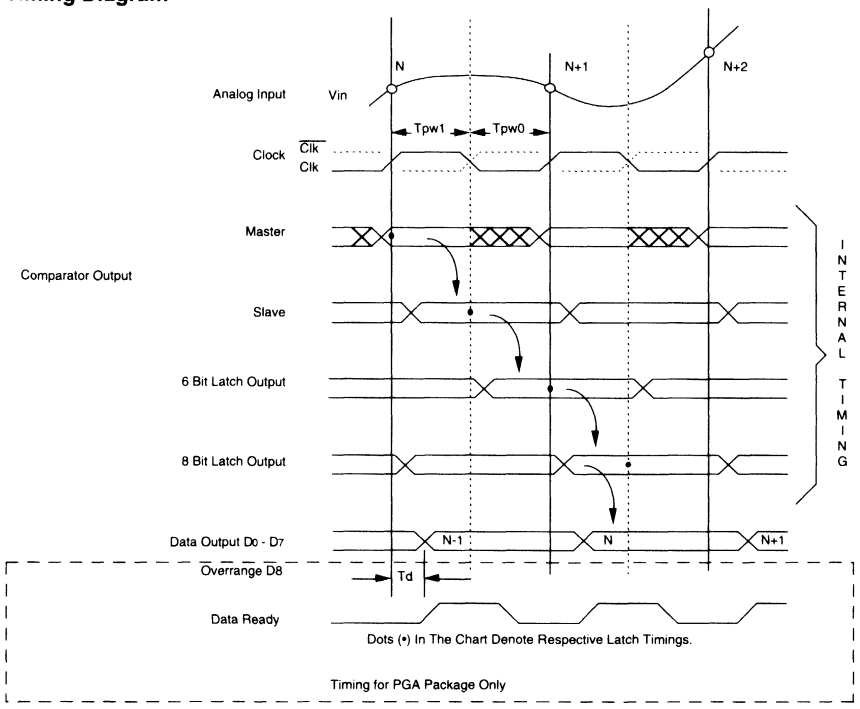
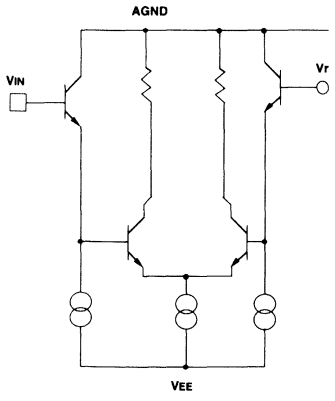
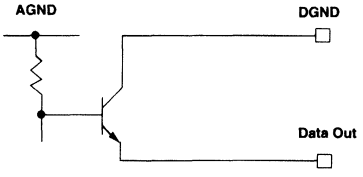


Figure 4 - Subcircuit Schematics

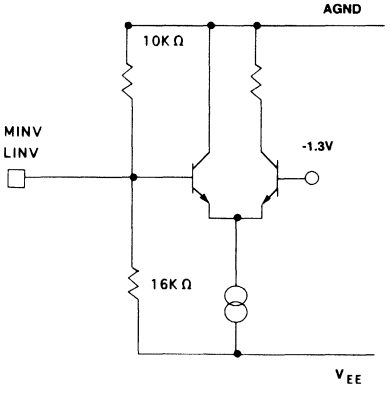
INPUT CIRCUIT



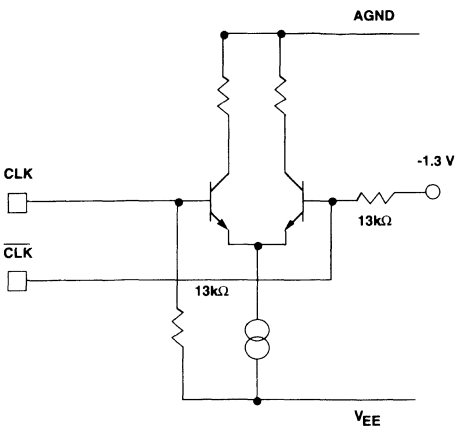
OUTPUT CIRCUIT



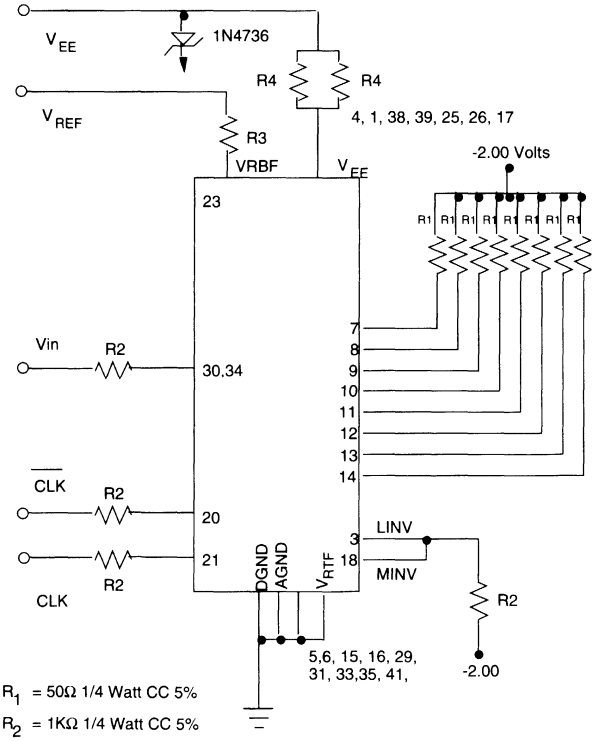
MINV, LINV INPUT CIRCUIT



CLOCK INPUT



BURN-IN CIRCUIT (42L DIP PACKAGE ONLY)



R_1 = 50Ω 1/4 Watt CC 5%
R_2 = 1KΩ 1/4 Watt CC 5%
R_3 = 6.5Ω 1/4 Watt CC 5%
R_4 = 6.5Ω 1/2 Watt CC 5%
V_{REF} = -2.00 Volts
V_{EE} = -6.6 Volts

DEFINITION OF TERMS

A/D CONVERTER ERROR SUMMARY

The transfer function for an A/D converter is very dependent on the slew rate of the signal it is digitizing. The transfer function under dynamic conditions may exhibit numerous errors (Figure 5B) while a static DC input level may appear close to the ideal (Figure 5A). Many dynamic tests as well as the industry standard DC specifications were included for this reason.

TOTAL DYNAMIC ERROR (EFFECTIVE BITS)

Total Dynamic Error (TDE) is the difference between the measured data at the output of an A/D converter in response to a sinewave and an ideal sinewave's data best fitted to the measured data. The data is then plotted as usable (effective) output bits versus frequency. This is the most important specification since it is tested over the entire frequency range of the part and shows true dynamic performance. It also indicates the cumulative effect of many error sources. These errors are quantization error, dynamic differential nonlinearity, missing codes, integral nonlinearity, total harmonic distortion, aperture uncertainty and noise. Not included are DC specifications such as offset and gain errors. The result is calculated from the measured RMS error for the ideal sinewave and the measured actual RMS error as follows:

$$\text{eff bits} = 8 - \log_2 \frac{\text{actual RMS error}}{\text{ideal RMS error}}$$

Furthermore, TDE can be related to effective bits by the following formula:

$$\text{TDE(dB)} = 1.8 + 6.02 \times \text{N(eff bits)}$$

QUANTIZATION ERROR

Quantization error is the fundamental, irreducible error associated with the perfect quantizing of a continuous (analog) signal into a finite number of digital bits (A/D transfer function). An 8-bit A/D converter can represent an input voltage with a best case uncertainty of 1 part in 2^8 (1 part in 256). In real A/Ds under dynamic operating conditions, the quantization bands (bit change step versus input amplitude) for certain codes can be significantly larger (or smaller) than the ideal. The ideal width of each quantization step (or band) is Q = FSR/2^N where FSR = full scale range and N = 8. Nonideal quantization bands represent differential nonlinearity errors. See Figures 5A and 5B.

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DIFFERENTIAL NONLINEARITY

Differential nonlinearity is a measurement of how much the actual quantization step width varies from the ideal step width of 1 LSB. Figure 5B shows a differential nonlinearity of 2 LSB; the actual step width is 3 LSB. The SPT7710's specification gives the worst case differential nonlinearity in the A/D transfer function under specified dynamic operating conditions. Small, localized differential nonlinearities may be insignificant when digitizing full scale signals. However, if a low level input signal happens to fall on that part of the A/D transfer function with the differential nonlinearity error, the effect will be significant.

MISSING CODES

Missing codes represent a special kind of differential nonlinearity. The quantization step width for a missing code is 0 LSB which results in a differential nonlinearity of -1 LSB. Figure 5B illustrates two missed codes in the transfer function.

Figure 5A - Static Input Conditions

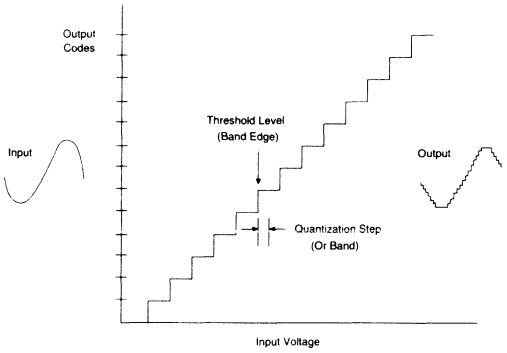
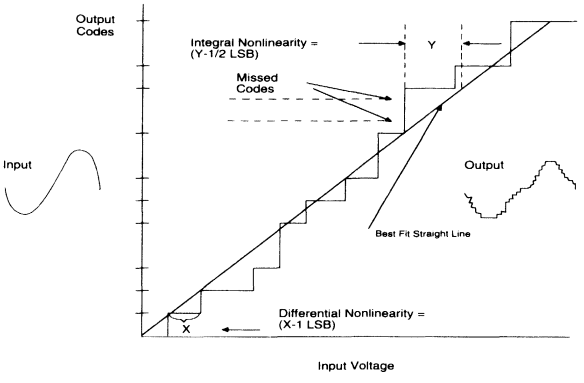


Figure 5B - Dynamic Conditions



INTEGRAL NONLINEARITY

Integral nonlinearity is the maximum deviation of the A/D transfer function from a best fit straight line (Figure 6A). Integral nonlinearity does not include any gain or offset errors. Integral nonlinearity in an A/D is generally more detrimental when digitizing full scale signals than low level signals which may fall on a part of the transfer function which is relatively linear. Figure 5B shows an integral nonlinearity error of 2 LSBs. The SPT7710's integral nonlinearity can be improved by using the external reference ladder tap as shown in Figure 1. The resulting effect on the linearity is shown in Figure 6B.

Figure 6A - Linearity Curve with no TAP adjustment

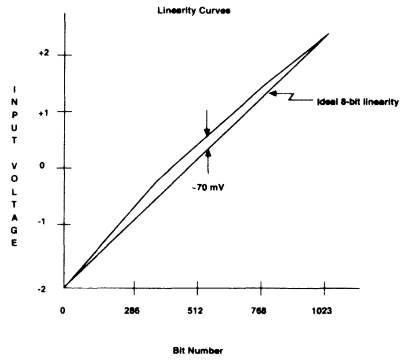
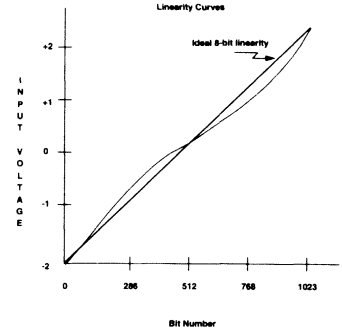


Figure 6B - Linearity Curve with TAP Forced to within .05 mV of Ideal



APERTURE UNCERTAINTY

Aperture uncertainty is the time jitter in the sample point and is caused by short term stability errors in the timebase generating the sample (encode) command to the A/D converter. The approximate voltage error due to aperture uncertainty depends on the slew rate of the signal at the sample point. See Figure 7A.

As in any sampled data system, the aperture width affects the accuracy of the system. The aperture time can be considered an amplitude uncertainty for any input where the voltage is changing. The magnitude of this change for a sinewave can be calculated for time or voltage by the equation:

$$dV/V = 2\pi ft_a$$

By calculating the aperture time for a given system accuracy and comparing it to the aperture time specification of the flash converter, the need for a track-and-hold can be determined. Figure 7B shows the required aperture time for 8-bit resolution high speed converters using sinusoidal waveforms.

An example using an 8-bit flash converter follows. If the signal that is to be measured is known to contain no sinusoidal frequencies above 10 MHz, then it can be determined the A/D converter must have an aperture time of less than 70 ps to ensure less than 8 bits of error due to aperture alone. (See Figure 7B.) Most data sheets do not state aperture time so a sample-and-hold is usually used.

Aperture time and delay are very difficult to measure. However, these values are needed to make intelligent design decisions. SPT supplies these values based on computer design simulations and verified by characterization of samples.

Figure 7A - Aperture Uncertainty

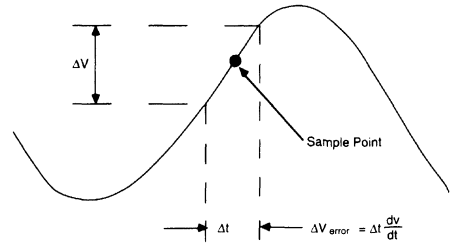
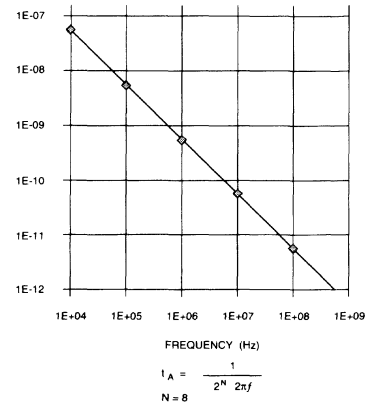


Figure 7B - Aperture Time - Sinewaves



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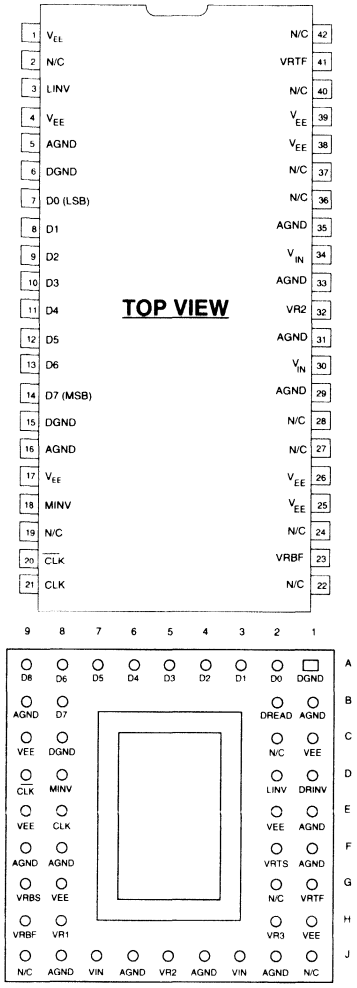
PIN ASSIGNMENT SPT7710



PIN FUNCTIONS SPT7710

LINV	D0 through D6 Output Inversion Control Pin
VEE	Negative Analog Supply Nominally -5.2 V
DGND	Digital Ground
D0	Digital Data Output (LSB)
D1-D6	Digital Data Output
D7	Digital Data Output (MSB)
MINV	D7 Output Inversion Control Pin
$\overline{CLK}$	Inverse ECL Clock Input Pin
CLK	ECL Clock Input Pin
AGND	Analog Ground
VIN	Analog Input; Can be Connected to the Input Signal or Used as a Sense
VR2	Reference Voltage Tap 2 (1.0 V TYP)
VRTF	Reference Voltage Top
VRBF	Reference Voltage Bottom

(The following pin functions are for PGA package only)

DRINV	Data Ready Inverse
DREAD	Data Ready Output
Overrange	Overrange Output D8
VR1	Reference Voltage Tap 1 (-1.5 V TYP)
VR3	Reference Voltage Tap 3 (-0.5 V TYP)
VRTS	Reference Voltage Top, Sense
VRBS	Reference Voltage Bottom, Sense

LEADERSHIP IN DATA CONVERSION AND SIGNAL PROCESSING

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SIGNAL PROCESSING TECHNOLOGIES

SPT7725

8-BIT, 250 MSPS FLASH A/D CONVERTER

PRELIMINARY INFORMATION

3

FEATURES

- Metastable Errors Reduced to 1 LSB
- Low Input Capacitance - 10 pF
- Wide Input Bandwidth - 210 MHz
- 250 MSPS Conversion Rate
- Typical Power Dissipation <2 Watts

APPLICATIONS

- Digital Oscilloscopes
- Transient Capture
- Radar, EW, ECM
- Direct RF Down-Conversion
- Medical Electronics: Ultrasound, CAT Instrumentation

GENERAL DESCRIPTION

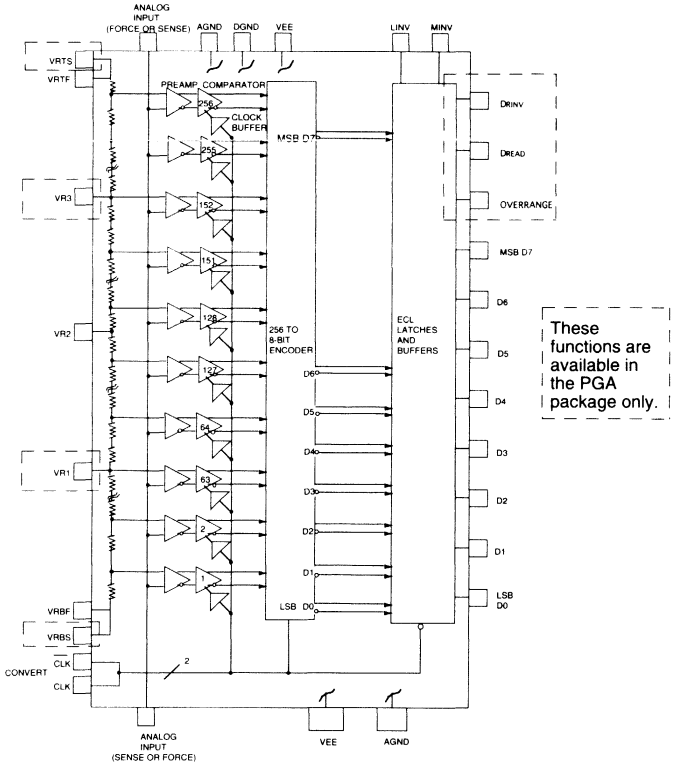
The SPT7725 is a monolithic flash A/D converter capable of digitizing a two volt analog input signal into 8-bit digital words at a 250 MSPS (TYP) update rate.

For most applications, no external sample-and-hold is required for accurate conversion due to the device's narrow aperture time, wide bandwidth, and low input capacitance. A single standard -5.2 volt power supply is required for operation of the SPT7725, with nominal power dissipation of 2 W.

A proprietary decoding scheme reduces metastable errors to the 1 LSB level.

The part is packaged in a 42L ceramic sidebrazed DIP which is pin compatible with the SPT7710. A 46L PGA package is also available which allows access to additional reference ladder taps, an overrange bit, and a data ready output. The SPT7725 is available in an industrial temperature range. Contact the factory for military temperature range and surface-mount package options.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Beyond which damage may occur)[1] 25 °C

Supply Voltages
Negative Supply Voltage (V_{EE} TO GND) ..... -7.0 to +0.5 V
Ground Voltage Differential ..... -0.5 to +0.5 V

Input Voltage
Analog Input Voltage ..... +0.5 V to V_{EE}
Reference Input Voltage ..... +0.5 V to V_{EE}
Digital Input Voltage ..... +0.5 V to V_{EE}
Reference Current VRTF to VRBF ..... 25 mA

Output
Digital Output Current ..... 0 to -25 mA

Temperature
Operating Temperature, ambient ..... -25 to +85 °C
junction ..... +150 °C
Lead Temperature, (soldering 10 seconds). ..... +300 °C
Storage Temperature ..... -65 to +150 °C

Notes: 1. Operation at any Absolute Maximum Rating is not implied. See Electrical Specifications for proper nominal applied conditions in typical applications.

ELECTRICAL SPECIFICATIONS

$T_A=T_{MIN}$ to T_{MAX}, V_{EE}=-5.2 V, R_{Source}=50 Ω, V_{RBF}=-2.00 V, V_{R2}=-1.0 V, V_{RTF}=0.00 V, f_{clk}=250 MHz, Duty Cycle=50%, unless otherwise specified.

PARAMETERS	TEST CONDITIONS	TEST LEVEL	SPT7725A			SPT7725B			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
DC ELECTRICAL CHARACTERISTICS									
Integral Linearity		II	-0.75		+0.75	-0.95		+0.95	LSB
Differential Linearity (No missing codes guaranteed)		II	-0.75		+0.75	-0.95		+0.95	LSB
Offset Error VRT		II	-30		+30	-30		+30	mV
Offset Error VRB		II	-30		+30	-30		+30	mV
Input Voltage Range		II	-2		0.0	-2		0.0	Volts
Input Capacitance	Over full input range	V		10			10		pF
Input Resistance		V		70			70		kΩ
Input Current		II		250	500		250	500	µA
Clock Synchronous Input Currents		V		40			40		µA
Supply Current	T_A=25 °C	II		400	500		400	500	mA
Power Dissipation	T_A=25 °C	II		2.0	2.6		2.0	2.6	W
Ladder Resistance		II	100	200	300	100	200	300	Ω
Reference Bandwidth		V		10			10		MHz
Digital Output High Voltage	50 Ω to -2 V	II	-1.1	-0.9	-0.7	-1.1	-0.9	-0.7	Volts
Digital Output Low Voltage	50 Ω to -2 V	II	-1.95	-1.8	-1.5	-1.95	-1.8	-1.5	Volts
Digital Input High Voltage (MINV, LINV)		II	-1.1		-0.7	-1.1		-0.7	Volts
Digital Input Low Voltage (MINV, LINV)		II	-2.0		-1.5	-2.0		-1.5	Volts

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ELECTRICAL SPECIFICATIONS

T_A=+25 °C, V_{EE}=-5.2 V, R_{Source}=50 Ω, V_{RBF}=-2.00 V, V_{R2}=-1.0 V, V_{RTF}=0.00 V, f_{clk}=250 MHz, Duty Cycle=50%, unless otherwise specified.

PARAMETERS	TEST CONDITIONS	TEST LEVEL	SPT7725A MIN	SPT7725A TYP	SPT7725A MAX	SPT7725B MIN	SPT7725B TYP	SPT7725B MAX	UNITS
AC ELECTRICAL CHARACTERISTICS									
Maximum Sample Rate		I	250			250			MSPS
Clock Low Width, TPW0		I	2	1.8		2	1.8		ns
Clock High Width, TPW1		I	2	1.8		2	1.8		ns
Output Delay (TD)		V		2.0			2.0		ns
Output Delay TEMPCO		V		1			1		ps/°C
Data-to-Data Ready Delay		V		2.0			2.0		ns
Large Signal Bandwidth	V_{IN}=F.S.	V		210			210		MHz
Small Signal Bandwidth	V_{IN}=500 mV P-P	V		335			335		MHz
Aperture Jitter		V		5			5		ps
Acquisition Time		V		1.5			1.5		ns
Input Slew Rate		V		1,000			1,000		V/µs
Total Dynamic Error	F_{IN} = 3.58 MHz	I	44	48		44	48		dB
	F_{IN} = 100 MHz	I	TBD	35		TBD	33		dB
Signal-to-Noise Ratio	F_{IN} = 3.58 MHz	I	46	49		46	49		dB
	F_{IN} = 100 MHz	I	TBD	44		TBD	42		dB
Total Harmonic Distortion	F_{IN} = 3.58 MHz	I	47	52		47	52		dBc
	F_{IN} = 100 MHz	I	TBD	35		TBD	33		dBc

TEST LEVEL CODES

All electrical characteristics are subject to the following conditions:

All parameters having min/max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality Assurance inspection. Any blank section in the data column indicates that the specification is not tested at the specified condition.

Unless otherwise noted, all tests are pulsed tests; therefore, $T_J = T_C = T_A$.

TEST LEVEL	TEST PROCEDURE
I	100% production tested at the specified temperature.
II	100% production tested at T_A=25 °C, and sample tested at the specified temperatures.
III	QA sample tested only at the specified temperatures.
IV	Parameter is guaranteed (but not tested) by design and characterization data.
V	Parameter is a typical value for information purposes only.
VI	100% production tested at T_A = 25 °C. Parameter is guaranteed over specified temperature range.

GENERAL DESCRIPTION

The SPT7725 is a fast monolithic 8-bit parallel flash A/D converter. The nominal conversion rate is 250 MSPS and the analog bandwidth is in excess of 200 MHz. A major advance over previous flash converters is the inclusion of 256 input preamplifiers between the reference ladder and input comparators. (See block diagram.) This not only reduces clock transient kickback to the input and reference ladder due to a low AC beta but also reduces the effect of the dynamic state of the input signal on the latching characteristics of the input comparators. The preamplifiers act as buffers and stabilize the input capacitance so that it remains constant over different input voltages and frequency ranges and therefore makes the part easier to drive than previous flash converters. The SPT7725 incorporates a proprietary decoding scheme that reduces metastable errors (sparkle codes or *flyers*) to a maximum of 1 LSB.

The SPT7725 has true differential analog and digital data paths from the preamplifiers to the output buffers (Current Mode Logic) for reducing potential missing codes while rejecting common mode noise.

Signature errors are also reduced by careful layout of the analog circuitry. Every comparator also has a clock buffer to reduce differential delays and to improve signal-to-noise ratio. The output drive capability of the device can provide full ECL swings into 50 Ω loads.

TYPICAL INTERFACE CIRCUIT

The typical interface circuit is shown in figure 1. The SPT7725 is relatively easy to apply depending on the accuracy needed in the intended application. Wire-wrap may be employed with careful point-to-point ground connections if desired, but to achieve the best operation, a double sided PC board with a ground plane on the component side separated into digital and analog sections will give the best performance. The converter is bonded-out to place the digital pins on the left side of the package and the analog pins on the right side. Additionally, an RF bead connection through a single point from the analog to digital ground planes will reduce ground noise pickup.

The circuit in Figure 2 (PGA package only) is intended to show the most elaborate method of achieving the least error by correcting for integral linearity, input induced distortion, and power supply/ground noise. This is achieved by the use of external reference ladder tap connections, input buffer and supply decoupling. The function of each pin and external connections to other components is as follows:

Figure 1 - SPT7725 Typical Interface Circuit 1

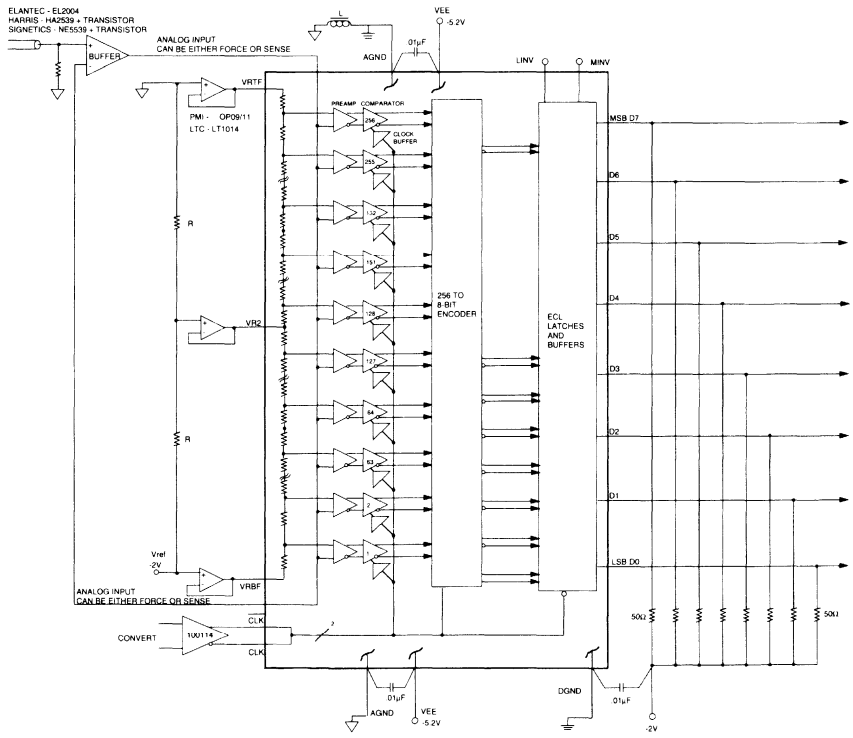

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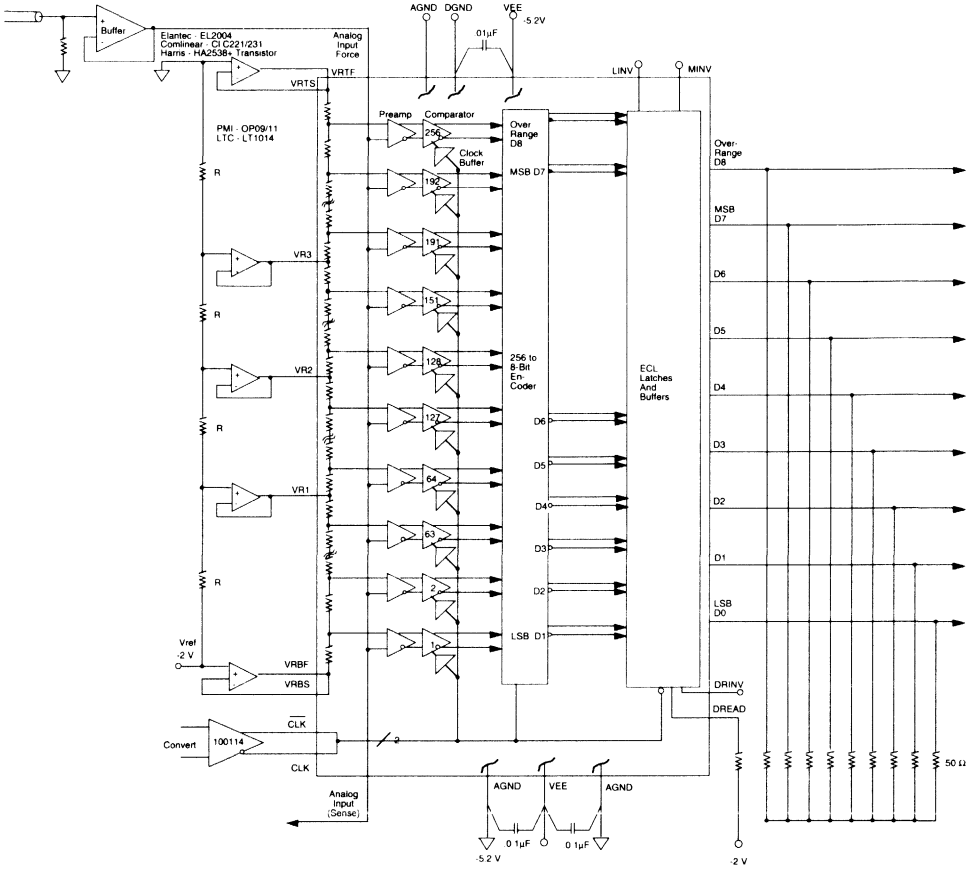
Figure 2 - SPT7725 Typical Interface Circuit 2 (PGA Package Only)



V_{EE}, AGND, DGND

V_{EE} is the supply pin with AGND as ground for the device. The power supply pins should be bypassed as close to the device as possible with at least a .01 µF ceramic capacitor. A 1 µF tantalum can also be used for low frequency suppression. DGND is the ground for the ECL outputs and is to be referenced to the output pulldown voltage and appropriately bypassed as shown in Figure 1.

VIN (ANALOG INPUT)

There are two analog input pins that are tied to the same point internally. Either one may be used as an analog input *sense* and the other for input *force*. This is convenient for testing the source signal to see if there is sufficient drive capability. The pins can also be tied together and driven by the same source. The SPT7725 is superior to similar devices due to a preamplifier stage before the comparators. This makes the device easier to drive because it has constant capacitance and induces less slew rate distortion. If an input buffer is needed, a Harris HA2540 may be used in conjunction with an output transistor buffer for lower frequency applications. For higher frequencies, another option is to use an Elantec EL2004 video buffer or an HA2539 and a 2N5836 transistor. Very high performance can be achieved by using a Comlinear CLC221/231.

CLK, $\overline{CLK}$ (CLOCK INPUTS)

The clock inputs are designed to be driven differentially with ECL levels. The clock may be driven single-ended since $\overline{CLK}$ is internally biased to -1.3 V. (See clock input circuit.) $\overline{CLK}$ may be left open but a .01 µF bypass capacitor from $\overline{CLK}$ to AGND is recommended. NOTE: System performance may be degraded due to increased clock noise or jitter.

MINV, LINV (OUTPUT LOGIC CONTROL)

These are ECL-compatible digital controls for changing the output code from straight binary to two's complement, etc. For more information, see Table I. Both MINV and LINV are in the logic low (0) state when they are left open. The high state can be obtained by tying to AGND through a diode or 3.9 kΩ resistor.

Table I - Output Coding

MINV LINV	0 0	0 1	1 0	1 1
0V	111...11	100...00	011...11	000...00
.	111...10	100...01	011...10	000...01
.	.	.	.	.
.	.	.	.	.
.	.	.	.	.
V_{IN} .	100...00	111...11	000...00	011...11
.	011...11	000...00	111...11	100...00
.	.	.	.	.
.	.	.	.	.
.	.	.	.	.
.	000...01	011...10	100...01	111...10
-2V	000...00	011...11	100...00	111...11

1: V_{IH}, V_{OH} 0: V_{IL}, V_{OL}

D0 TO D7 (DIGITAL OUTPUTS)

The digital outputs can drive ECL levels into 50 Ωs when pulled down to -2 V. When pulled down to -5.2 V, the outputs can drive 130 Ω to 1 kΩ loads.

VRBF, VR2, VRTF (REFERENCE INPUTS)

There are two reference inputs and one external reference voltage tap. These are -2 V (VRBF), mid-tap (VR2) and AGND (VRTF). The reference pins and tap can be can be driven by op amps as shown in Figure 1 or VR2 may be bypassed for limited temperature operation. These voltage inputs can be bypassed to AGND for further noise suppression if desired.

VRBF, VRBS, VR1, VR2, VR3, VRTF, VRTS REFERENCE INPUTS *(PGA PACKAGE ONLY)*

These are five external reference voltage taps from -2V (VRBF) to AGND (VRTF) which can be used to control integral linearity over temperature. The taps can be driven by op amps as shown in Figure 2. These voltage level inputs can be bypassed to AGND for further noise suppression if so desired. VRB and VRT have "force" and "sense" pins for monitoring the top and bottom voltage references.

DREAD - DATA READY, DRINV - DATA READY INVERSE *(PGA PACKAGE ONLY)*

The data ready pin is a flag that goes high or low at the output when data is valid or ready to be received. It is essentially a delay line that accounts for the time necessary for information to be clocked through the SPT7725's decoders and latches. This function is useful for interfacing with high speed memory. Using the data ready output to latch the output data ensures minimum setup and hold times. DRINV is a data ready inverse control pin (see Timing Diagram).

D8 - OVERRANGE *(PGA PACKAGE ONLY)*

This is an overrange function. When the SPT7725 is in an overrange condition, D8 goes high and all data outputs go high as well. This makes it possible to include the SPT7725 into higher resolution systems.

N/C

All *Not Connected* pins should be tied to DGND on the left side of the package and to AGND of the right side of the package.

OPERATION

The SPT7725 has 256 preamp/comparator pairs which are each supplied with the voltage from VRTF to VRBF divided equally by the resistive ladder as shown in the block diagram. This voltage is applied to the positive input of each preamplifier/comparator pair. An analog input voltage applied at VIN is connected to the negative inputs of each preamplifier/comparator pair. The comparators are then clocked through each comparator's individual clock buffer. When the CLK pin is in the low state, the master or input stage of the comparators compares the analog input voltage to the respective reference voltage. When the CLK pin changes from low to high, the comparators are latched to the state prior to the clock transition and output logic codes in sequence from the top comparators, closest to VRTF (0 V), down to the point where the magnitude of the input signal changes sign (thermometer code). The output of each comparator is then registered into four 64-to-6 bit decoders when the CLK is changed from high to low. At the output of the decoders is a set of four 7-bit latches which are enabled (*track*) when the clock changes from high to low. From here, the outputs of the latches are coded into 6 LSBs from 4 columns and 4 columns are coded into 2 MSBs. Next are the MINV and LINV controls for output inversions which consist of a set of eight XOR gates. Finally, 8 ECL output latches and buffers are used to drive the external loads. The conversion takes one clock cycle from the input to the data outputs.

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Figure 3 - Timing Diagram

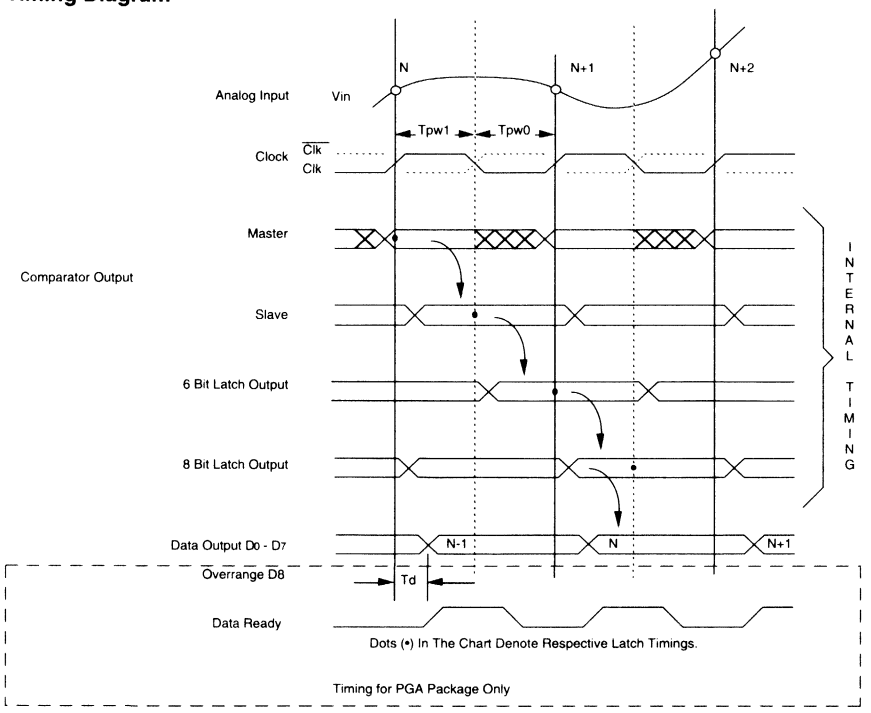
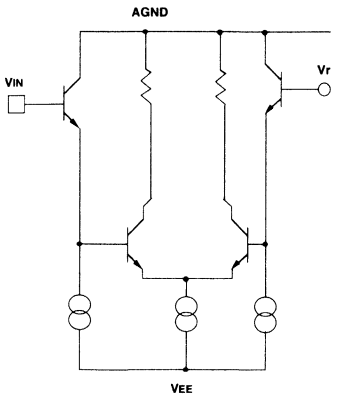
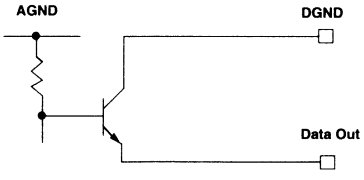


Figure 4 - Subcircuit Schematics

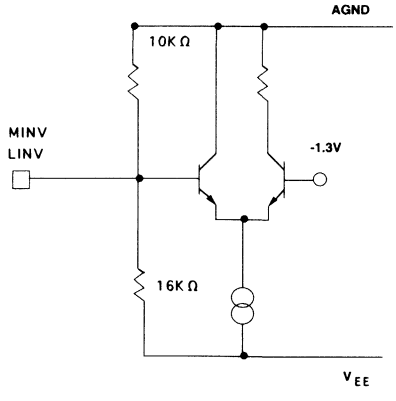
INPUT CIRCUIT



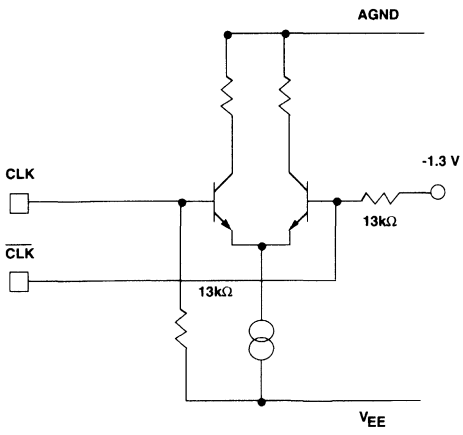
OUTPUT CIRCUIT



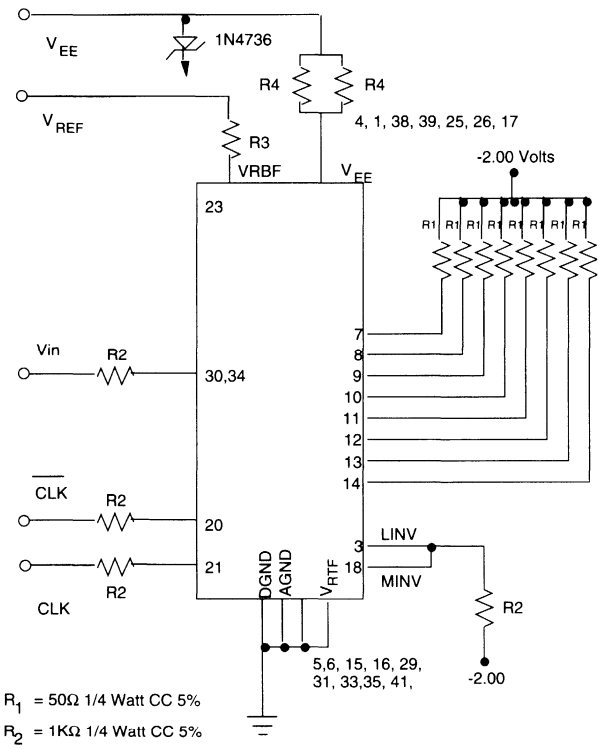
MINV, LINV INPUT CIRCUIT



CLOCK INPUT



BURN-IN CIRCUIT (42L DIP PACKAGE ONLY)



R_1 = 50Ω 1/4 Watt CC 5%
R_2 = 1KΩ 1/4 Watt CC 5%
R_3 = 6.5Ω 1/4 Watt CC 5%
R_4 = 6.5Ω 1/2 Watt CC 5%
V_{REF} = -2.00 Volts
V_{EE} = -6.6 Volts

DEFINITION OF TERMS

A/D CONVERTER ERROR SUMMARY

The transfer function for an A/D converter is very dependent on the slew rate of the signal it is digitizing. The transfer function under dynamic conditions may exhibit numerous errors (Figure 5B) while a static DC input level may appear close to the ideal (Figure 5A). Many dynamic tests as well as the industry standard DC specifications were included for this reason.

TOTAL DYNAMIC ERROR (EFFECTIVE BITS)

Total Dynamic Error (TDE) is the difference between the measured data at the output of an A/D converter in response to a sinewave and an ideal sinewave's data best fitted to the measured data. The data is then plotted as usable (effective) output bits versus frequency. This is the most important specification since it is tested over the entire frequency range of the part and shows true dynamic performance. It also indicates the cumulative effect of many error sources. These errors are quantization error, dynamic differential nonlinearity, missing codes, integral nonlinearity, total harmonic distortion, aperture uncertainty and noise. Not included are DC specifications such as offset and gain errors. The result is calculated from the measured RMS error for the ideal sinewave and the measured actual RMS error as follows:

$$\text{eff bits} = 8 - \log_2 \frac{\text{actual RMS error}}{\text{ideal RMS error}}$$

Furthermore, TDE can be related to effective bits by the following formula:

$$\text{TDE(dB)} = 1.8 + 6.02 \text{ X N(eff bits)}$$

QUANTIZATION ERROR

Quantization error is the fundamental, irreducible error associated with the perfect quantizing of a continuous (analog) signal into a finite number of digital bits (A/D transfer function). An 8-bit A/D converter can represent an input voltage with a best case uncertainty of 1 part in 2^8 (1 part in 256). In real A/Ds under dynamic operating conditions, the quantization bands (bit change step versus input amplitude) for certain codes can be significantly larger (or smaller) than the ideal. The ideal width of each quantization step (or band) is Q = FSR/2^N where FSR = full scale range and N = 8. Nonideal quantization bands represent differential nonlinearity errors. See Figures 5A and 5B.

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DIFFERENTIAL NONLINEARITY

Differential nonlinearity is a measurement of how much the actual quantization step width varies from the ideal step width of 1 LSB. Figure 5B shows a differential nonlinearity of 2 LSB; the actual step width is 3 LSB. The SPT7725's specification gives the worst case differential nonlinearity in the A/D transfer function under specified dynamic operating conditions. Small, localized differential nonlinearities may be insignificant when digitizing full scale signals. However, if a low level input signal happens to fall on that part of the A/D transfer function with the differential nonlinearity error, the effect will be significant.

MISSING CODES

Missing codes represent a special kind of differential nonlinearity. The quantization step width for a missing code is 0 LSB which results in a differential nonlinearity of -1 LSB. Figure 5B illustrates two missed codes in the transfer function.

Figure 5A - Static Input Conditions

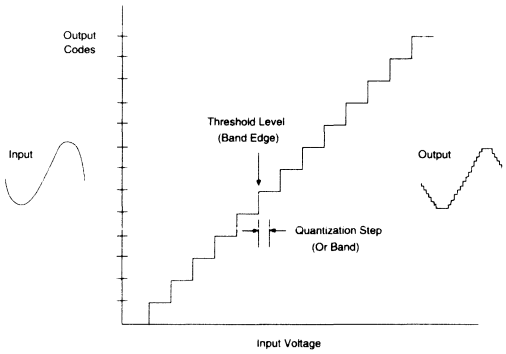
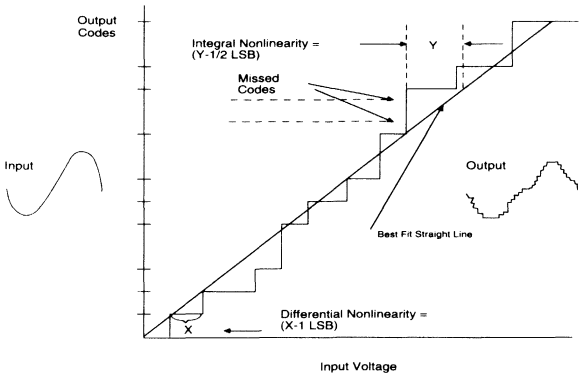


Figure 5B - Dynamic Conditions



INTEGRAL NONLINEARITY

Integral nonlinearity is the maximum deviation of the A/D transfer function from a best fit straight line (Figure 6A). Integral nonlinearity does not include any gain or offset errors. Integral nonlinearity in an A/D is generally more detrimental when digitizing full scale signals than low level signals which may fall on a part of the transfer function which is relatively linear. Figure 5B shows an integral nonlinearity error of 2 LSBs. The SPT7725's integral nonlinearity can be improved by using the external reference ladder tap as shown in Figure 1. The resulting effect on the linearity is shown in Figure 6B.

Figure 6A - Linearity Curve with no TAP adjustment

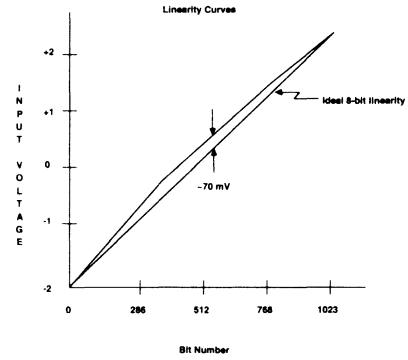
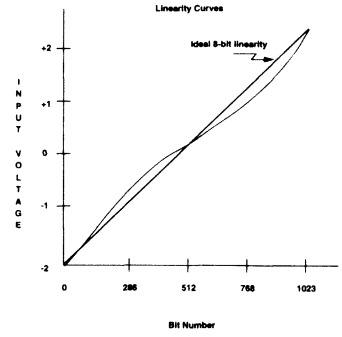


Figure 6B - Linearity Curve with TAP Forced to within .05 mV of Ideal



APERTURE UNCERTAINTY

Aperture uncertainty is the time jitter in the sample point and is caused by short term stability errors in the timebase generating the sample (encode) command to the A/D converter. The approximate voltage error due to aperture uncertainty depends on the slew rate of the signal at the sample point. See Figure 7A.

As in any sampled data system, the aperture width affects the accuracy of the system. The aperture time can be considered an amplitude uncertainty for any input where the voltage is changing. The magnitude of this change for a sinewave can be calculated for time or voltage by the equation:

$$dV/V = 2\pi ft_a$$

By calculating the aperture time for a given system accuracy and comparing it to the aperture time specification of the flash converter, the need for a track-and-hold can be determined. Figure 7B shows the required aperture time for 8-bit resolution high speed converters using sinusoidal waveforms.

An example using an 8-bit flash converter follows. If the signal that is to be measured is known to contain no sinusoidal frequencies above 10 MHz, then it can be determined the A/D converter must have an aperture time of less than 70 ps to ensure less than 8 bits of error due to aperture alone. (See Figure 7B.) Most data sheets do not state aperture time so a sample-and-hold is usually used.

Aperture time and delay are very difficult to measure. However, these values are needed to make intelligent design decisions. SPT supplies these values based on computer design simulations and verified by characterization of samples.

Figure 7A - Aperture Uncertainty

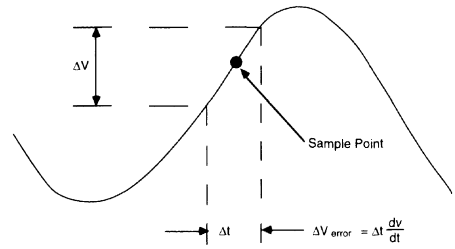
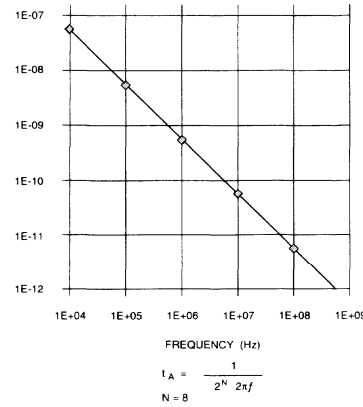


Figure 7B - Aperture Time - Sinewaves



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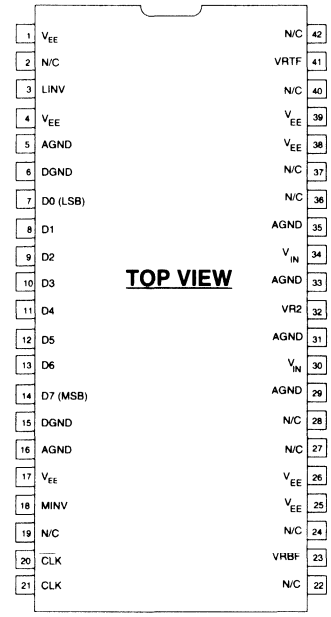
PIN ASSIGNMENT SPT7725



PIN FUNCTIONS SPT7725

LINV	D0 through D6 Output Inversion Control Pin
VEE	Negative Analog Supply Nominally -5.2 V
DGND	Digital Ground
D0	Digital Data Output (LSB)
D1-D6	Digital Data Output
D7	Digital Data Output (MSB)
MINV	D7 Output Inversion Control Pin
$\overline{CLK}$	Inverse ECL Clock Input Pin
CLK	ECL Clock Input Pin
AGND	Analog Ground
VIN	Analog Input; Can be Connected to the Input Signal or Used as a Sense
VR2	Reference Voltage Tap 2 (1.0 V TYP)
VRTF	Reference Voltage Top
VRBF	Reference Voltage Bottom

(The following pin functions are for PGA package only)

DRINV	Data Ready Inverse
DREAD	Data Ready Output
Overrange	Overrange Output D8
VR1	Reference Voltage Tap 1 (-1.5 V TYP)
VR3	Reference Voltage Tap 3 (-0.5 V TYP)
VRTS	Reference Voltage Top, Sense
VRBS	Reference Voltage Bottom, Sense

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SIGNAL PROCESSING TECHNOLOGIES

SPT7750

8-BIT, 500 MSPS FLASH A/D CONVERTER

PRELIMINARY INFORMATION

3

FEATURES

- 1:2 Demuxed ECL Compatible Outputs
- Wide Input Bandwidth - 900 MHz
- Low Input Capacitance - 15 pF
- Metastable Errors Reduced to 1 LSB
- Monolithic for Low Cost
- Gray Code Output

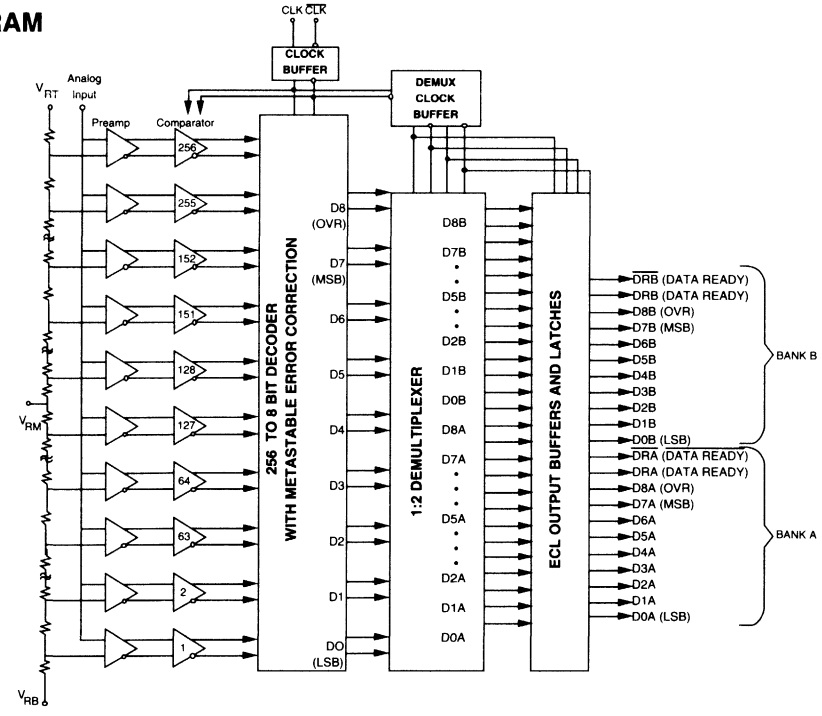
APPLICATIONS

- Digital Oscilloscopes
- Transient Capture
- Radar, EW, ECM
- Direct RF Down-conversion

GENERAL DESCRIPTION

The SPT7750 is a full parallel (flash) analog-to-digital converter capable of digitizing full scale (0 to -2 V) inputs into eight-bit digital words at an update rate of 500 MSPS. The ECL-compatible outputs are demultiplexed into two separate output banks, each with differential data ready outputs to ease the task of data capture. The SPT7750's wide input bandwidth and low capacitance eliminate the need for external track-and-hold amplifiers for most applications. A proprietary decoding scheme reduces metastable errors to the 1 LSB level. The SPT7750 operates from a single -5.2 V supply, with a nominal power dissipation of 4.5 W.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Beyond which damage may occur)[1] 25 °C

Supply Voltages
- Negative Supply Voltage (V_{EE} TO GND) ..... -7.0 to +0.5 V
- Ground Voltage Differential ..... -0.5 to +0.5 V

Input Voltage
- Analog Input Voltage ..... +0.5 V to V_{EE}
- Reference Input Voltage ..... +0.5 V to V_{EE}
- Digital Input Voltage ..... +0.5 V to V_{EE}
- Reference Current VRT to VRB ..... 35 mA

Output
- Digital Output Current ..... 0 to -25 mA

Temperature
- Operating Temperature, ambient ..... -25 to +85 °C
- case ..... +125 °C
- junction ..... +150 °C
- Lead Temperature, (soldering 10 seconds). ..... +300 °C
- Storage Temperature ..... -65 to +150 °C

Notes: 1. Operation at any Absolute Maximum Rating is not implied. See Electrical Specifications for proper nominal applied conditions in typical applications.

ELECTRICAL SPECIFICATIONS

T = T_{MIN} to T_{MAX}, V_{EE}=-5.2 V, V_{RB}=-2.00 V, VRM=-1.0 V, VRT=0.00 V, f_{clk}=500 MHz, Duty Cycle=50%, unless otherwise specified.

PARAMETERS	TEST CONDITIONS	TEST LEVEL	SPT7750A MIN	SPT7750A TYP	SPT7750A MAX	SPT7750B MIN	SPT7750B TYP	SPT7750B MAX	UNITS
DC ELECTRICAL CHARACTERISTICS									
Integral Linearity		II	-0.75		+0.75	-1.5		+1.5	LSB
Differential Linearity (No missing codes guaranteed)		II	-0.75		+0.75	-0.95		+1.5	LSB
Offset Error VRT		II	-30		+30	-30		+30	mV
Offset Error VRB		II	-30		+30	-30		+30	mV
Input Voltage Range		II	-2		0.0	-2		0.0	Volts
Input Capacitance	Over full input range	V		15			15		pF
Input Resistance		V		70			70		kΩ
Input Current		II		750			750		µA
Clock Synchronous Input Currents		V		2			2		µA
Supply Current		II		870			870		mA
Power Dissipation		II		4.5			4.5		W
Ladder Resistance		II		80			80		Ω
Reference Bandwidth		V		30			30		MHz
Digital Output High Voltage		II	-1.1	-0.9		-1.1	-0.9		Volts
Digital Output Low Voltage		II		-1.8	-1.5		-1.8	-1.5	Volts
Digital Input High Voltage (CLK, NCLK)		II	-1.1		-0.7	-1.1		-0.7	Volts
Input Low Voltage (CLK, NCLK)		II	-2.0		-1.5	-2.0		-1.5	Volts

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ELECTRICAL SPECIFICATIONS

T =25 °C, V_{EE}=-5.2 V, V_{RB}=-2.00 V, VRM=-1.0 V, VRT=0.00 V, f_{clk}=500 MHz, Duty Cycle=50%, unless otherwise specified.

PARAMETERS	TEST CONDITIONS	TEST LEVEL	SPT7750A MIN	SPT7750A TYP	SPT7750A MAX	SPT7750B MIN	SPT7750B TYP	SPT7750B MAX	UNITS
AC ELECTRICAL CHARACTERISTICS									
Maximum Sample Rate		I	500	700		500	700		MSPS
Clock Low Width, TPW0		I	0.7	1		0.7	1		ns
Clock High Width, TPW1		I	0.7	1		0.7	1		ns
DATA to DATA READY Delay		IV		1.8			1.8		ns
Clock to Data Delay		IV		1			1		ns
Small Signal Bandwidth		V		900			900		MHz
Aperture Jitter		V		2			2		ps
Acquisition Time		V		250			250		ps
Input Slew Rate		V		5			5		V/ns
Total Dynamic Error	F_{IN} = 50 MHz F_{IN} = 250 MHz	I		-44 -38			-44 -38		dB dB
Signal to Noise Ratio	F_{IN} = 50 MHz F_{IN} = 250 MHz	I		45 40			45 40		dB dB
Total Harmonic Distortion	F_{IN} = 50 MHz F_{IN} = 250 MHz	I		48 41			48 41		dBc dBc

TEST LEVEL CODES

All electrical characteristics are subject to the following conditions:

All parameters having min/max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality Assurance inspection. Any blank section in the data column indicates that the specification is not tested at the specified condition.

Unless otherwise noted, all tests are pulsed tests; therefore, $T_J = T_C = T_A$.

TEST LEVEL	TEST PROCEDURE
I	100% production tested at the specified temperature.
II	100% production tested at T_A=25 °C, and sample tested at the specified temperatures.
III	QA sample tested only at the specified temperatures.
IV	Parameter is guaranteed (but not tested) by design and characterization data.
V	Parameter is a typical value for information purposes only.
VI	100% production tested at T_A = 25 °C. Parameter is guaranteed over specified temperature range.

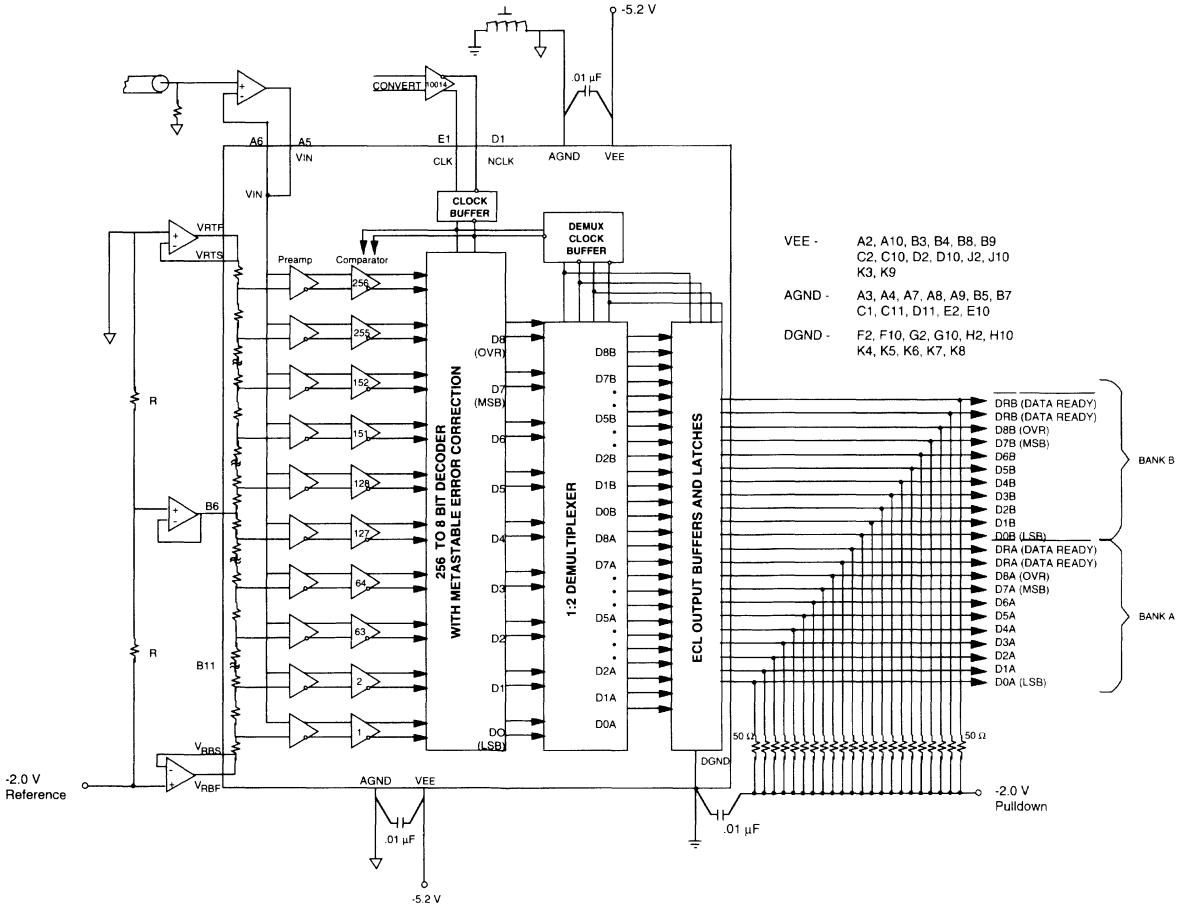
GENERAL DESCRIPTION

The SPT7750 is the fastest monolithic 8-bit parallel flash A/D converter available today. The nominal conversion rate is 500 MSPS and the analog bandwidth is in excess of 900 MHz. A major advance over previous flash converters is the inclusion of 256 input preamplifiers between the reference ladder and input comparators (see block diagram). This not only reduces clock transient kickback to the input and reference ladder due to a low AC beta but also reduces the effect of the dynamic state of the input signal on the latching characteristics of the input comparators. The preamplifiers act as buffers and stabilize the input capacitance so that it remains constant over different input voltage and frequency ranges and therefore makes the part easier to drive than previous flash converters. The preamplifiers also add a gain of two to the input signal so that each comparator has a wider overdrive or threshold range to "trip" into or out of the active state. This gain reduces metastable states that can cause errors at the output.

The SPT7750 has true differential analog and digital data paths from the preamplifiers to the output buffers (Current Mode Logic) for reducing potential missing codes while rejecting common mode noise.

Signature errors are also reduced by careful layout of the analog circuitry. The output drive capability of the device can provide full ECL swings into 50 Ω loads.

Figure 1 - SPT7750 Typical Interface Circuit



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TYPICAL INTERFACE CIRCUIT

The SPT7750 is relatively easy to apply depending on the accuracy needed in the intended application. Wire-wrap may be employed with careful point-to-point ground connections if desired, but to achieve the best operation a double sided PC board with a ground plane on the component side separated into digital and analog sections will give the best performance. An RF bead connection through a single point from the analog to digital ground planes will reduce ground noise pickup.

The circuit in figure 1 is intended to show the most elaborate method of achieving the least error by correcting for integral linearity, input induced distortion and power supply/ground noise. This is achieved by the use of external reference ladder tap connections, input buffer and supply decoupling. The function of each pin and external connections to other components are as follows:

V_{EE}, AGND, DGND

V_{EE} is the supply pin with AGND as ground for the device. The power supply pins should be bypassed as close to the device as possible with at least a .01 µF ceramic capacitor. A 1 µF tantalum can also be used for low frequency suppression. DGND is the ground for the ECL outputs and is to be referenced to the output pulldown voltage and appropriately bypassed as shown in figure 5.

VIN (ANALOG INPUT)

There are two analog input pins that are tied to the same point internally. Either one may be used as an analog input "sense" and the other for input "force". This is convenient for testing the source signal to see if there is sufficient drive capability. The pins can also be tied together and driven by the same source. The SPT7750 is superior to similar devices due to a preamplifier stage before the comparators. This makes the device easier to drive because it has constant capacitance and induces less slew rate distortion.

CLK, $\overline{CLK}$ (CLOCK INPUTS)

The clock inputs are designed to be driven differentially with ECL levels. The duty cycle of the clock should be kept at 50% to avoid causing larger second harmonics. If this is not important to the intended application, then duty cycles other than 50% may be used.

D0 TO D8, DR, $\overline{DR}$ (A AND B)

The digital outputs can drive 50 Ω to ECL levels when pulled down to -2 V. When pulled down to -5.2 V, the outputs can drive 130 Ω to 1 kΩ loads. All digital outputs are grey code with the coding as shown in table 1.

VRBF, VRBS, VRTF, VRTS, VRM (REFERENCE INPUTS)

There are two reference inputs and one external reference voltage tap. These are -2 V (VRB force and sense), mid-tap (VRM) and AGND (VRT force and sense). The reference pins and tap can be driven by op amps as shown in figure 1 or VRM may be bypassed for limited temperature operation. These voltage inputs can be bypassed to AGND for further noise suppression if so desired.

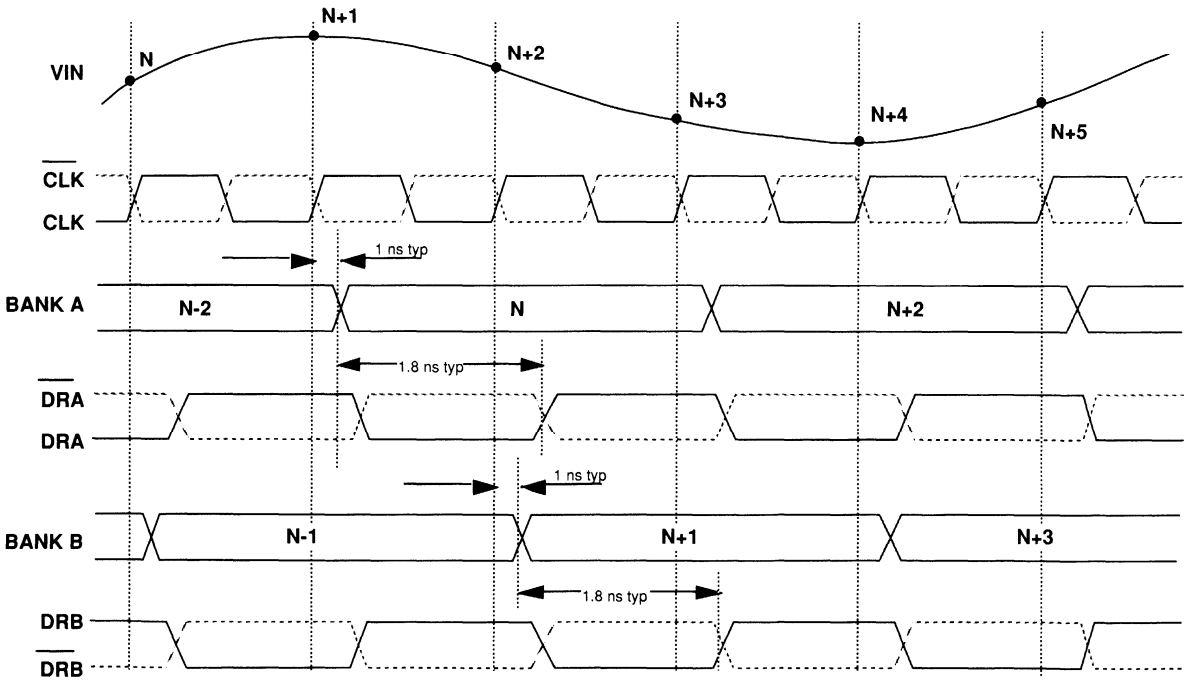
Table I - Output Coding

V_{IN}	D8	D7.....DO
0 V	1	10000000
•	0	10000000
•	0	10000001
•	0	10000011
•	0	10000010
•		⋮
•	0	11111011
•	0	11111010
•	0	11111110
•	0	11111111
•	0	11111101
•	0	11111100
•	0	11110100
•		
•		⋮
•		
•	0	00000110
•	0	00000010
•	0	00000011
•	0	00000001
-2 V	0	00000000

OPERATION

The SPT7750 has 256 preamp/comparator pairs which are each supplied with the voltage from VRT to VRB divided equally by the resistive ladder as shown in the block diagram. This voltage is applied to the positive input of each preamplifier/comparator pair. An analog input voltage applied at VIN is connected to the negative inputs of each preamplifier/comparator pair. The comparators are then clocked through each one's individual clock buffer. When the CLK pin is in the low state, the master or input stage of the comparators compare the analog input voltage to the respective reference voltage. When the CLK pin changes from low to high the comparators are latched to the state prior to the clock transition and output logic codes in sequence from the top comparators, closest to VRT (0 V), down to the point where the magnitude of the input signal changes sign (thermometer code). The output of each comparator is then registered into four 64-to-6 bit decoders when the CLK is changed from high to low. At the output of the decoders is a set of four 7-bit latches which are enabled ("track") when the clock changes from high to low. From here, the output of the latches are coded into 6 LSBs from 4 columns and 4 columns are coded into 2 MSBs. Finally, 8 ECL output latches and buffers are used to drive the external loads. The conversion takes one clock cycle from the input to the data outputs.

TIMING DIAGRAM*



*** Typical Timing at 500 MSPS**

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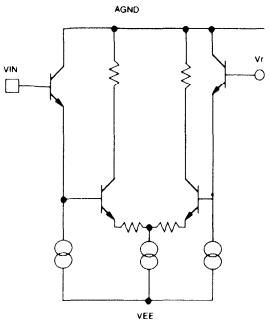
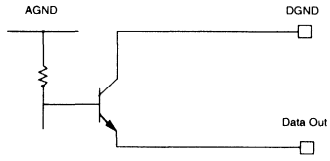
SUBCIRCUIT SCHEMATICS

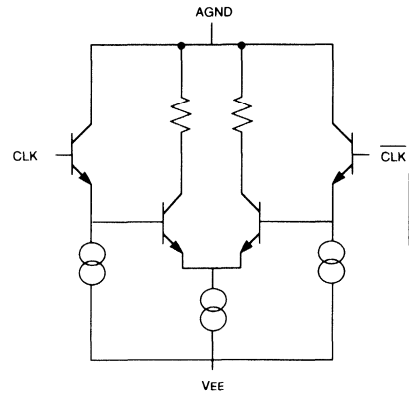
INPUT CIRCUIT



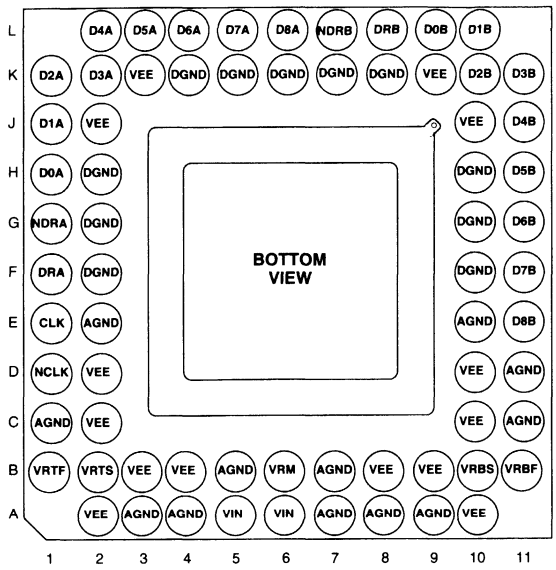
OUTPUT CIRCUIT



CLOCK INPUT



PIN ASSIGNMENT SPT7750



PIN FUNCTIONS SPT7750

NAME	FUNCTION
V_{EE}	Negative Supply Nominally -5.2 V
AGND	Analog Ground
VRTF	Reference Voltage Force Top, Nominally 0 V
VRTS	Reference Voltage Sense Top
VRM	Reference Voltage Middle, Nominally -1 V
VRBF	Reference Voltage Force Bottom, Nominally -2 V
VRBS	Reference Voltage Sense Bottom
VIN	Analog Input Voltage, Can Be Either Voltage or Sense
DGND	Digital Ground
D0~D7A	Data Output Bank A
D0~D7B	Data Output Bank B
DRA	Data Ready Bank A
NDRA	Not Data Ready Bank A
DRB	Data Ready Bank B
NDRB	Not Data Ready Bank B
D8A	Overrange Output Bank A
D8B	Overrange Output Bank B
CLK	Clock Input
NCLK	$\overline{\text{Clock Input}}$

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SIGNAL PROCESSING TECHNOLOGIES

SPT7810

10-BIT, 20 MSPS, ECL OUTPUT A/D CONVERTER

FEATURES

- Monolithic 20 MSPS Converter
- On-Chip Track/Hold
- Bipolar ±2.0 V Analog Input
- 60 dB SNR @ 1 MHz Input
- Low Power (1.3 W Typical)
- 5 pF input Capacitance
- ECL Outputs

APPLICATIONS

- Medical Imaging
- Professional Video
- Radar Receivers
- Instrumentation
- Electronic Warfare
- Digital Communications

GENERAL DESCRIPTION

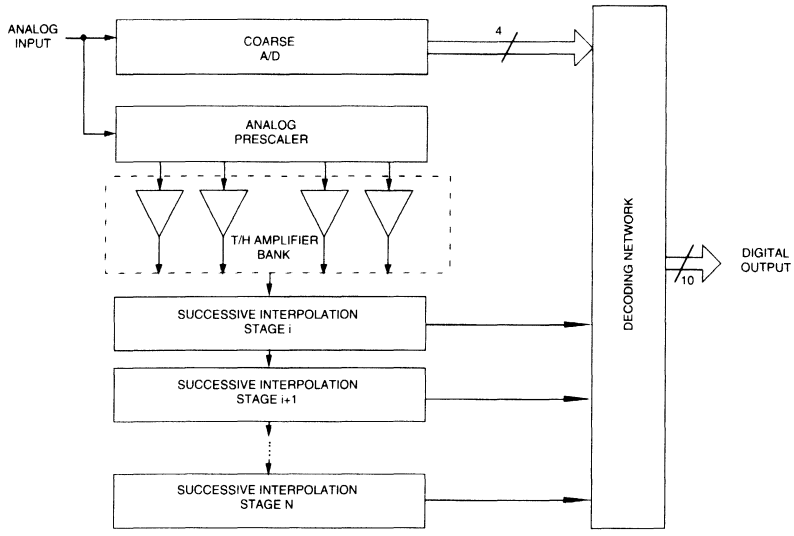
The SPT7810 A/D converter is a 10-bit monolithic converter capable of word rates of a minimum of 20 MSPS. On board track/hold function assures excellent dynamic performance without the need for external components. Drive requirement problems are minimized with an input capacitance of only 5 pF.

Inputs and outputs are ECL to provide a higher level of noise immunity in high speed system applications. An overrange output signal is provided to indicate overflow conditions.

Output data format is straight binary. Power dissipation is very low at only 1.3 watts with power supply voltages of +5.0 and -5.2 volts. The SPT7810 also provides a wide input voltage swing of ±2.0 volts.

The SPT7810 is available in a small 28-lead ceramic sidebrazed DIP, PDIP, and die form. Commercial and industrial temperature ranges are currently offered. Contact the factory for availability of military temperature range and /883 processed units.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Beyond which damage may occur)[1] 25 °C

Supply Voltages

V_{CC} ..... +6 V
V_{EE} ..... -6 V

Input Voltages

Analog Input ..... $V_{FB} \leq V_{IN} \leq V_{FT}$
V_{FT}, V_{FB} ..... +3.0 V, -3.0 V
Reference Ladder Current ..... 12 mA

Output

Digital Outputs ..... +30 to -30 mA

Temperature

Operating Temperature ..... -25 to +85 °C
Junction Temperature [(1)] ..... 175 °C
Lead Temperature, (soldering 10 seconds) ..... 300 °C
Storage Temperature ..... -65 to +150 °C

Note: 1. Operation at any Absolute Maximum Rating is not implied. See Electrical Specifications for proper nominal applied conditions in typical applications.

ELECTRICAL SPECIFICATIONS

$T_A=T_{min}$ - T_{max}, V_{CC}=+5.0 V, V_{EE}=-5.2 V, V_{IN}=±2.0 V, V_{SB}=-2.0 V, V_{ST}=+2.0 V, f_{clock}=20 MHz, 50% clock duty cycle, unless otherwise specified.

PARAMETERS	TEST CONDITIONS	TEST LEVEL	SPT7810A MIN	SPT7810A TYP	SPT7810A MAX	SPT7810B MIN	SPT7810B TYP	SPT7810B MAX	UNITS
Resolution			10			10			Bits
DC Accuracy (+25 °C)	+/- Full Scale								
Integral Nonlinearity	250 kHz Sample Rate	I		±1.0			±1.5		LSB
Differential Nonlinearity		I		±0.5			±0.75		LSB
No Missing Codes				Guaranteed			Guaranteed		
Analog Input									
Input Voltage Range		VI		±2.0			±2.0		V
Input Bias Current	V_{IN}=0 V	VI		30	60		30	60	µA
Input Resistance		VI	100	300		100	300		kΩ
Input Capacitance		V		5			5		pF
Input Bandwidth	3 dB Small Signal	V		120			120		MHz
+FS Error		V		±2.0			±2.0		LSB
-FS Error		V		±2.0			±2.0		LSB
Reference Input									
Reference Ladder Resistance		VI	500	800		500	800		Ω
Reference Ladder Tempco		V		0.8			0.8		Ω/°C
Timing Characteristics									
Maximum Conversion Rate		VI	20			20			MHz
Overvoltage Recovery Time		V		20			20		ns
Pipeline Delay (Latency)		VI			1			1	Clock Cycle
Output Delay	T_A=+25 °C	V		14	18		14	18	ns
Aperture Delay Time	T_A=+25 °C	V		1			1		ns
Aperture Jitter Time	T_A=+25 °C	V		5			5		ps-RMS
Dynamic Performance									
Effective Number of Bits									
fin=1 MHz				9.2			8.7		Bits
fin=3.58 MHz				8.8			8.3		Bits
fin=10.3 MHz				7.5			7.0		Bits

[1] Typical thermal impedances: 28L sidebrazed DIP. θ_{ja} = 50 °C/W, 28L plastic DIP θ_{ja} = 50 °C/W.

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ELECTRICAL SPECIFICATIONS

$T_A=T_{min}$ - T_{max}, V_{CC}=+5.0 V, V_{EE}=-5.2 V, V_{IN}=±2.0 V, V_{SB}=-2.0 V, V_{ST}=+2.0 V, f_{clock}=20 MHz, 50% clock duty cycle, unless otherwise specified.

PARAMETERS	TEST CONDITIONS	TEST LEVEL	SPT7810A MIN	SPT7810A TYP	SPT7810A MAX	SPT7810B MIN	SPT7810B TYP	SPT7810B MAX	UNITS
Dynamic Performance									
Signal-To-Noise Ratio (without Harmonics)									
fin=1 MHz	+25 °C	I	57	60		54	57		dB
	$T_A=T_{min}$ - T_{max}	IV	55	58		52	55		dB
fin=3.58 MHz	+25 °C	I	56	58		53	55		dB
	$T_A=T_{min}$ - T_{max}	IV	54	56		51	53		dB
fin=10.3 MHz	+25 °C	I	50	53		47	49		dB
	$T_A=T_{min}$ - T_{max}	IV	47	50		44	46		dB
Harmonic Distortion[2]									
fin=1 MHz	+25 °C	I	57	60		54	57		dB
	$T_A=T_{min}$ - T_{max}	IV	54	57		51	54		dB
fin=3.58 MHz	+25 °C	I	56	58		53	55		dB
	$T_A=T_{min}$ - T_{max}	IV	53	55		50	52		dB
fin=10.3 MHz	+25 °C	I	46	48		43	45		dB
	$T_A=T_{min}$ - T_{max}	IV	45	47		42	44		dB
Signal-to-Noise and Distortion									
fin=1 MHz	+25 °C	I	55	57		52	54		dB
	$T_A=T_{min}$ - T_{max}	IV	52			49			dB
fin=3.58 MHz	+25 °C	I	54	55		51	52		dB
	$T_A=T_{min}$ - T_{max}	IV	51			48			dB
fin=10.3 MHz	+25 °C	I	44	47		41	44		dB
	$T_A=T_{min}$ - T_{max}	IV	43			40			dB
Spurious Free Dynamic Range	+25 °C, fin = 1 MHz	V		67			67		dB
Differential Phase	+25 °C, fin=3.58 & 4.35 MHz	V		0.2			0.2		Degree
Differential Gain	+25 °C, fin=3.58 & 4.35 MHz	V		0.5			0.7		%
Digital Inputs									
Logic "1" Voltage		V	-1.1			-1.1			V
Logic "0" Voltage		V			-1.5			-1.5	V
Maximum Input Current Low		VI	-500	±200	+750	-500	±200	+750	µA
Maximum Input Current High		VI	-500	±300	+750	-500	+300	+750	µA
Pulse Width Low (CLK)		IV	20			20			ns
Pulse Width High (CLK)		IV	20		300	20		300	ns
Digital Outputs									
Logic "1" Voltage	50 Ω to -2 V	VI	-1.1	-0.8		-1.1	-0.8		V
Logic "0" Voltage	50 Ω to -2 V	VI		-1.8	-1.5		-1.8	-1.5	V
Power Supply Requirements									
Voltages V_{CC}		IV	+4.75	-5.0	+5.25	+4.75	+5.0	+5.25	V
$-V_{EE}$		IV	-4.95	-5.2	-5.45	-4.95	-5.2	-5.45	V
Currents I_{CC}		II		140	170		140	190	mA
$-I_{EE}$		II		115	140		115	160	mA
Power Dissipation	Outputs Open	II		1.3	1.6		1.3	1.8	W
Power Supply Rejection Ratio	(5 V ±0.25 V, -5.2 V ±2.0 V)	V		1.0			1.0		LSB

[2] 64 distortion BINS from 4096 pt FFT.

Figure 1A: Timing Diagram

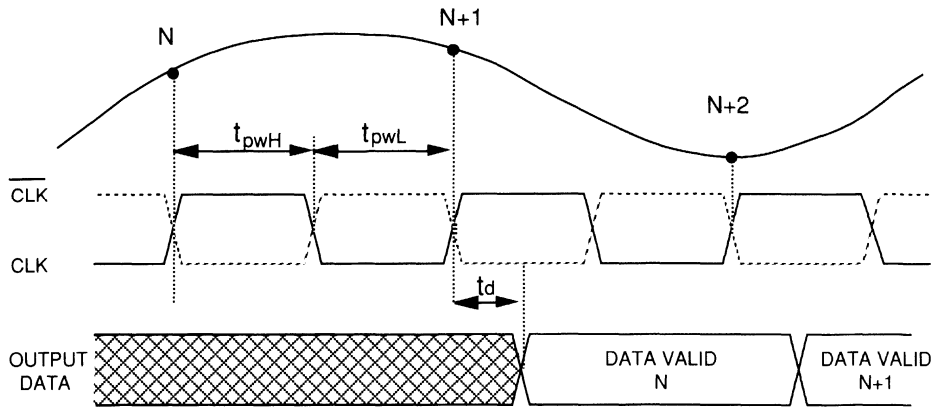

Figure 1B: Single Event Clock

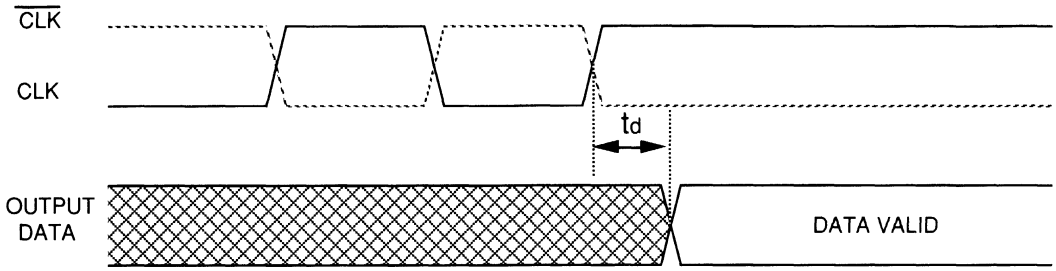

Table 1 - Timing Parameters

PARAMETERS	DESCRIPTION	MIN	TYP	MAX	UNITS
t_d	CLK to Data Valid Prop Delay	-	14	18	ns
t_{pwH}	CLK High Pulse Width	20	-	300	ns
t_{pwL}	CLK Low Pulse Width	20	-	-	ns

TEST LEVEL CODES

All electrical characteristics are subject to the following conditions:

All parameters having min/max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality Assurance inspection. Any blank section in the data column indicates that the specification is not tested at the specified condition.

Unless otherwise noted, all tests are pulsed tests; therefore, $T_J = T_C = T_A$.

TEST LEVEL	TEST PROCEDURE
I	100% production tested at the specified temperature.
II	100% production tested at T_A=25 °C, and sample tested at the specified temperatures.
III	QA sample tested only at the specified temperatures.
IV	Parameter is guaranteed (but not tested) by design and characterization data.
V	Parameter is a typical value for information purposes only.
VI	100% production tested at T_A = 25 °C. Parameter is guaranteed over specified temperature range.

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SPECIFICATION DEFINITIONS

APERTURE DELAY

Aperture delay represents the point in time, relative to the rising edge of the CLOCK input, that the analog input is sampled.

APERTURE JITTER

The variations in aperture delay for successive samples.

DIFFERENTIAL GAIN (DG)

A signal consisting of a sine wave superimposed on various DC levels is applied to the input. Differential gain is the maximum variation in the sampled sine wave amplitudes at these DC levels.

DIFFERENTIAL PHASE (DP)

A signal consisting of a sine wave superimposed on various DC levels that is applied to the input. Differential phase is the variation in the sampled sine wave phases at these DC levels.

EFFECTIVE NUMBER OF BITS (ENOB)

SINAD = 6.02N + 1.76, where N is equal to the effective number of bits.

$$N = \frac{SINAD - 1.76}{6.02}$$

+/- FULL-SCALE ERROR (GAIN ERROR)

Difference between measured full scale response [(+Fs) - (-Fs)] and the theoretical response (+4 V -2 LSBs) where the +FS (full scale) input voltage is defined as the output transition between 1-10 and 1-11 and the -FS input voltage is defined as the output transition between 0-00 and 0-01.

INPUT BANDWIDTH

Small signal (50 mV) bandwidth (3 dB) of analog input stage.

DIFFERENTIAL NONLINEARITY (DNL)

Error in the width of each code from its theoretical value. (Theoretical = $V_{FS}/2^N$)

INTEGRAL NONLINEARITY (INL)

Linearity error refers to the deviation of each individual code (normalized) from a straight line drawn from -Fs through +Fs. The deviation is measured from the edge of each particular code to the true straight line.

OUTPUT DELAY

Time between the clock's triggering edge and output data valid.

OVERVOLTAGE RECOVERY TIME

The time required for the ADC to recover to full accuracy after an analog input signal 125% of full scale is reduced to 50% of the full-scale value.

SIGNAL-TO-NOISE RATIO (SNR)

The ratio of the fundamental sinusoid power to the total noise power. Harmonics are excluded.

SIGNAL-TO-NOISE AND DISTORTION (SINAD)

The ratio of the fundamental sinusoid power to the total noise and distortion power.

TOTAL HARMONIC DISTORTION (THD)

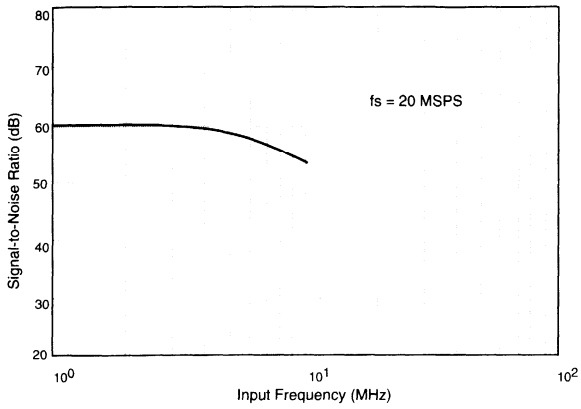
The ratio of the total power of the first 64 harmonics to the power of the measured sinusoidal signal.

SPURIOUS FREE DYNAMIC RANGE (SFDR)

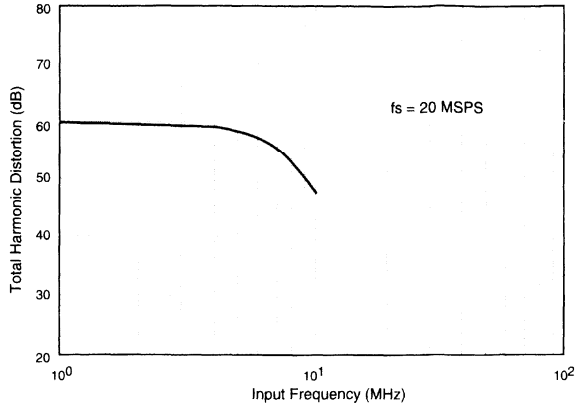
The ratio of the fundamental sinusoidal amplitude to the single largest harmonic or spurious signal.

PERFORMANCE CHARACTERISTICS

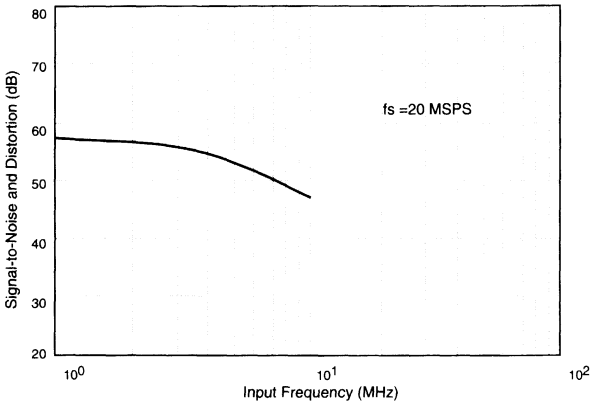
SNR vs Input Frequency



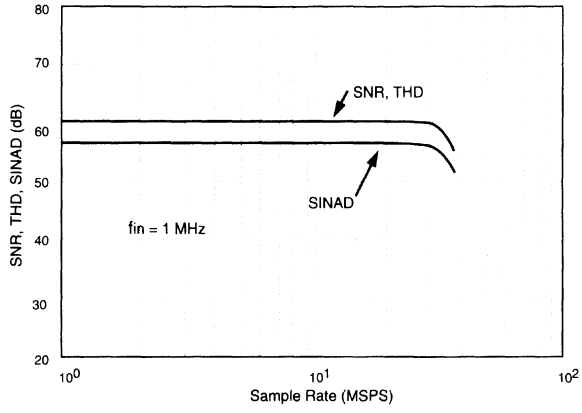
THD vs Input Frequency



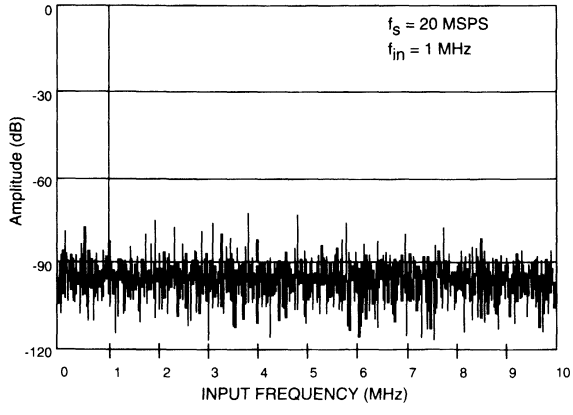
SINAD vs Input Frequency



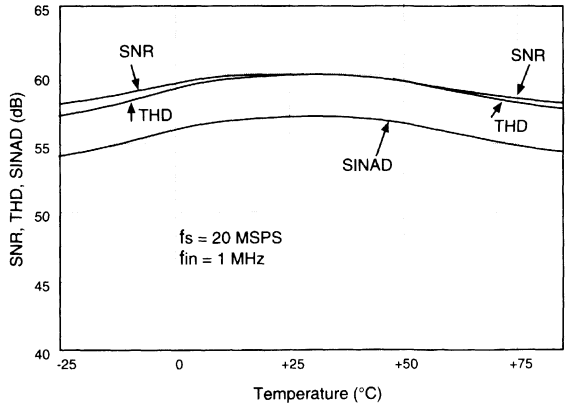
SNR, THD, SINAD vs Sample Rate



Spectral Response



SNR, THD, SINAD vs Temperature



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TYPICAL INTERFACE CIRCUIT

The SPT7810 requires few external components to achieve the stated operation and performance. Figure 2 shows the typical interface requirements when using the SPT7810 in normal circuit operation.

The following section provides a description of the pin functions and outlines critical performance criteria to consider for achieving the optimal device performance.

POWER SUPPLIES AND GROUNDING

The SPT7810 requires the use of two supply voltages, V_{EE} and V_{CC}. Both supplies should be treated as analog supply sources. This means the V_{EE} and V_{CC} ground returns of the device should both be connected to the analog ground plane. All other -5.2 V requirements of the external digital logic circuit should be connected to the digital ground plane. Each power supply pin should be bypassed as closely as possible to the device with .01 µF and 10 µF capacitors as shown in Figure 2.

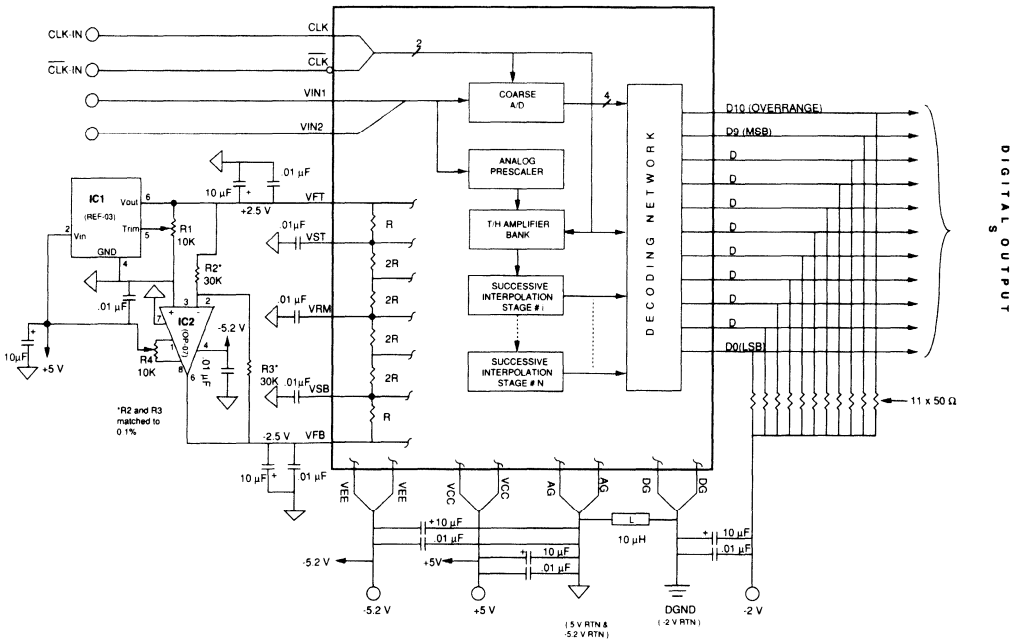
The two grounds available on the SPT7810 are AGND and DGND. DGND is used only for ECL outputs and is to be referenced to the output pulldown voltage. These grounds are not tied together internal to the device. The use of ground planes is recommended to achieve the best performance of the SPT7810. The AGND and the DGND ground planes should be separated from each other and only connected together at the device through an inductance. Doing this will minimize the ground noise pickup.

VOLTAGE REFERENCE

The SPT7810 requires the use of two voltage references: V_{FT} and V_{FB}. V_{FT} is the force for the top of the voltage reference ladder (+2.5 V typ), V_{FB} (-2.5 V typ) is the force for the bottom of the voltage reference ladder. Both voltages are applied across an internal reference ladder resistance of 800 ohms. In addition, there are 3 reference ladder taps (V_{ST},V_{RM} and V_{SB}). V_{ST} is the sense for the top of the reference ladder (+2.0 V), V_{RM} is the midpoint of the ladder (0.0 V typ) and V_{SB} is the sense for the bottom of the reference ladder (-2.0 V). The voltages seen at V_{ST} and V_{SB} are the true full scale input voltages of the device when V_{FT} and V_{FB} are driven to the recommended voltages (+2.5 V and -2.5 V typical respectively). These points should be used to monitor the actual full scale input voltage of the device and should not be driven to the expected ideal values as is commonly done with standard flash converters. When not being used, a decoupling capacitor of .01 uF connected to AGND from each tap is recommended to minimize high frequency noise injection.

An example of a reference driver circuit recommended is shown in figure 2. IC1 is REF-03, the +2.5 V reference with a tolerance of 0.6% or +/- 0.015 V. The potentiometer R1 is 10k

Figure 2 - Typical Interface Circuit



ohms and supports a minimum adjustable range of up to 150 mV. IC2 is recommended to be an OP-07 or equivalent device. R2 and R3 must be matched to within 0.1% with good TC tracking to maintain a 0.3 LSB matching between V_{FT} and V_{FB}. If 0.1% matching is not met, then potentiometer R4 can be used to adjust the V_{FB} voltage to the desired level. R1 and R4 should be adjusted such that V_{ST} and V_{SB} are exactly +2.0 V and -2.0V respectively.

The analog input range will scale proportionally with respect to the reference voltage if a different input range is required. The maximum scaling factor for device operation is ± 10% of the recommended reference voltages of V_{FT} and V_{FB}. However, because the device is laser trimmed to optimize performance with ± 2.5 V references, the accuracy of the device will degrade if operated beyond a ± 2% range.

The following errors are defined:
+FS error = top of ladder offset voltage = Δ(+FS -V_{ST}+1 LSB)
-FS error = bottom of ladder offset voltage = Δ(-FS -V_{SB}-1 LSB)
where the +FS (full scale) input voltage is defined as the output transition between 1-10 and 1-11 and the -FS input voltage is defined as the output transition between 0-00 and 0-01.

ANALOG INPUT

V_{IN1} and V_{IN2} are the analog inputs. Both inputs are tied to the same point internally. Either one may be used as an analog input "sense" and the other for an input "force." The inputs can also be tied together and driven from the same source. The full scale input range will be 80% of the reference voltage or ±2 volts with V_{FB}=-2.5 V and V_{FT}=+2.5 V.

The drive requirements for the analog inputs are minimal when compared to conventional Flash converters due the SPT7810's extremely low input capacitance of only 5 pF and very high input resistance of 300 kΩ. For example, for an input signal of ± 2 V p-p with an input frequency of 10 MHz, the peak output current required for the driving circuit is only 628 μA.

CLOCK INPUT

The clock inputs (CLK, $\overline{CLK}$) are designed to be driven differentially with ECL levels. The clock may be driven single ended since $\overline{CLK}$ is internally biased to -1.3 V. $\overline{CLK}$ may be left open, but a .01 μF bypass capacitor to AGND is recommended. As with all high speed circuits, proper terminations are required to avoid signal reflections and possible ringing that can cause the device to trigger at an unwanted time.

The CLK pulse width (tpwH) must be kept between 10 ns and 300 ns to ensure proper operation of the internal track-and-hold amplifier. (See timing diagram.) When operating the SPT7810 at sampling rates above 3 MSPS, it is recommended that the clock input duty cycle be kept at 50% to optimize performance. The analog input signal is latched on the rising edge of the CLK.

DIGITAL OUTPUTS

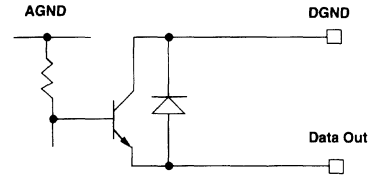
The format of the output data (D0-D9) is straight binary. These outputs are ECL with the output circuit shown in Figure 4. The outputs are latched on the rising edge of CLK with a propagation delay of 4 ns. There is a one clock cycle latency between CLK and the valid output data (see timing diagram). These digital outputs can drive 50 ohms to ECL levels when pulled down to -2 V. The total specified power dissipation of the device does not include the power used by these loads. The additional power used by these loads can vary between 10 and 300 mW typically (including the overrange load) depending on the output codes. If lower power levels are desired, the output loads can be reduced, but careful consideration to the capacitive loads in relation to the operating frequency must be considered.

Table 2 - Output Data Information

ANALOG INPUT	OVERRANGE D1O	OUTPUT CODE D9-DO
>+2.0 V + 1/2 LSB	1	11 1111 1111
+2.0 V -1 LSB	O	11 1111 111Ø
0.0 V	O	ØØ ØØØØ ØØØØ
-2.0 V +1 LSB	O	OO OOOO OOOØ
<2.0 V	O	OO OOOO OOOO

(Ø indicates the flickering bit between logic 0 and 1).

Figure 3 - Output Circuit



OVERRANGE OUTPUT

The OVERRANGE OUTPUT (D10) is an indication that the analog input signal has exceeded the positive full scale input voltage by 1 LSB. When this condition occurs, D10 will switch to logic 1. All other data outputs (D0 to D9) will remain at logic 1 as long as D10 remains at logic 1. This feature makes it possible to include the SPT7810 into higher resolution systems.

EVALUATION BOARD

The EB7810 Evaluation Board is available to aid designers in demonstrating the full performance of the SPT7810. This board includes a reference circuit, clock driver circuit, output data latches and an on-board reconstruction of the digital data. An application note describing the operation of this board as well as information on the testing of the SPT7810 is also available. Contact the factory for price and availability.

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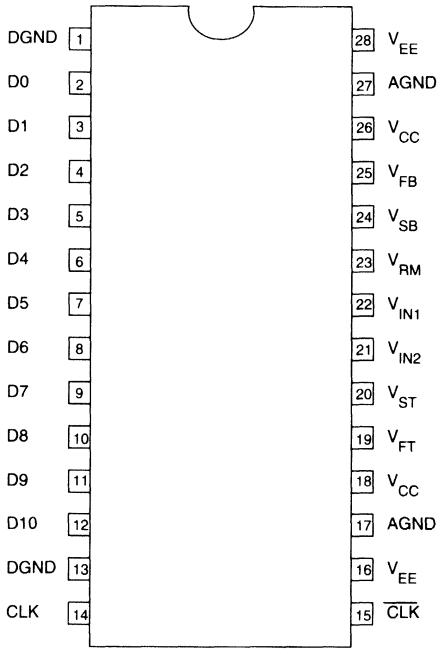
PIN ASSIGNMENT



PIN FUNCTIONS

NAME	FUNCTION
DGND	Digital Ground
D0-D9	ECL Outputs (D0=LSB)
D10	ECL Output Overrange
CLK	Clock Input
$\overline{CLK}$	Inverted Clock Input
V_{EE}	-5.2 V Supply
AGND	Analog Ground
V_{CC}	+5.0 V supply
V_{IN1}, V_{IN2}	Inputs (tied together at the die)
V_{FT}	Force for Top of Reference Ladder
V_{ST}	Sense for Top of Reference Ladder
V_{FB}	Force for Bottom of Reference Ladder
V_{SB}	Sense for Bottom of Reference Ladder
V_{RM}	Middle of Reference Ladder

LEADERSHIP IN DATA CONVERSION AND SIGNAL PROCESSING

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SPT
SIGNAL PROCESSING TECHNOLOGIES

SPT7814

10-BIT, 40 MSPS, ECL OUTPUT A/D CONVERTER

3

FEATURES

- Monolithic 40 MSPS Converter
- On-Chip Track/Hold
- Bipolar ±2.0 V Analog Input
- 57 dB SNR @ 3.58 MHz Input
- 50 dB SNR @ 10.3 MHz Input
- Low Power (1.3 W Typical)
- 5 pF input Capacitance
- ECL Outputs

APPLICATIONS

- Medical Imaging
- Professional Video
- Radar Receivers
- Instrumentation
- Electronic Warfare
- Digital Communications

GENERAL DESCRIPTION

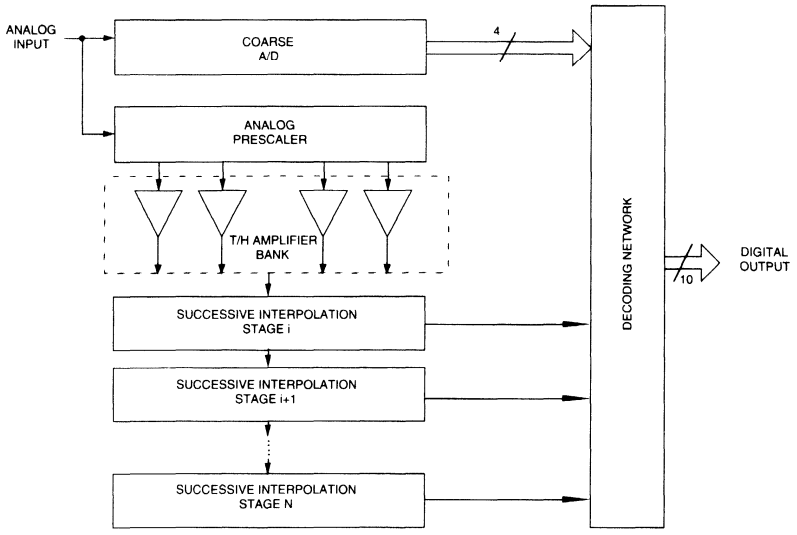
The SPT7814 A/D converter is a 10-bit monolithic converter capable of word rates of a minimum of 40 MSPS. On board track/hold function assures excellent dynamic performance without the need for external components. Drive requirement problems are minimized with an input capacitance of only 5 pF.

Inputs and outputs are ECL to provide a higher level of noise immunity in high speed system applications. An overrange output signal is provided to indicate overflow conditions.

Output data format is straight binary. Power dissipation is very low at only 1.3 watts with power supply voltages of +5.0 and -5.2 volts. The SPT7814 also provides a wide input voltage swing of ±2.0 volts.

The SPT7814 is available in a small 28-lead ceramic sidebrazed DIP, PDIP, and die form. Commercial and industrial temperature ranges are currently offered. Contact the factory for availability of military temperature ranges and /833 processed units.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Beyond which damage may occur)[1] 25 °C

Supply Voltages
- V_{CC} ..... +6 V
- V_{EE} ..... -6 V

Input Voltages
- Analog Input ..... $V_{FB} \leq V_{IN} \leq V_{FT}$
- V_{FT}, V_{FB} ..... +3.0 V, -3.0 V
- Reference Ladder Current ..... 12 mA

Output
- Digital Outputs ..... +30 to -30 mA

Temperature
- Operating Temperature ..... -25 to +85 °C
- Junction Temperature (1) ..... 175 °C
- Lead Temperature, (soldering 10 seconds) ..... 300 °C
- Storage Temperature ..... -65 to +150 °C

Note: 1. Operation at any Absolute Maximum Rating is not implied. See Electrical Specifications for proper nominal applied conditions in typical applications.

ELECTRICAL SPECIFICATIONS

$T_A=T_{min}$ - T_{max}, V_{CC}=+5.0 V, V_{EE}=-5.2 V, V_{IN}=±2.0 V, V_{SB}=-2.0 V, V_{ST}=+2.0 V, f_{clock}=40 MHz, 50% clock duty cycle, unless otherwise specified.

PARAMETERS	TEST CONDITIONS	TEST LEVEL	SPT7814A MIN	SPT7814A TYP	SPT7814A MAX	SPT7814B MIN	SPT7814B TYP	SPT7814B MAX	UNITS
Resolution			10			10			Bits
DC Accuracy (+25 °C)	+/- Full Scale								
Integral Nonlinearity	250 kHz Sample Rate	I		±1.0			±1.5		LSB
Differential Nonlinearity		I		±0.5			±0.75		LSB
No Missing Codes				Guaranteed			Guaranteed		
Analog Input									
Input Voltage Range		VI		±2.0			±2.0		V
Input Bias Current	V_{IN}=0 V	VI		30	60		30	60	µA
Input Resistance		VI	100	300		100	300		kΩ
Input Capacitance		V		5			5		pF
Input Bandwidth	3 dB Small Signal	V		120			120		MHz
+FS Error		V		±2.0			±2.0		LSB
-FS Error		V		±2.0			±2.0		LSB
Reference Input									
Reference Ladder Resistance		VI	500	800		500	800		Ω
Reference Ladder Tempco		V		0.8			0.8		Ω/°C
Timing Characteristics									
Maximum Conversion Rate		VI	40			40			MHz
Overvoltage Recovery Time		V		20			20		ns
Pipeline Delay (Latency)		VI			1			1	Clock Cycle
Output Delay	T_A=+25 °C	V		14	18		14	18	ns
Aperture Delay Time	T_A=+25 °C	V		1			1		ns
Aperture Jitter Time	T_A=+25 °C	V		5			5		ps-RMS
Dynamic Performance									
Effective Number of Bits									
fin=1 MHz				8.7			8.2		Bits
fin=3.58 MHz				8.7			8.2		Bits
fin=10.3 MHz				7.3			6.9		Bits

[1] Typical thermal impedances: 28L sidebrazed DIP. θ_{ja} = 50 °C/W, 28L plastic DIP θ_{ja} = 50 °C/W.

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ELECTRICAL SPECIFICATIONS

$T_A=T_{min}$ - T_{max}, V_{CC}=+5.0 V, V_{EE}=-5.2 V, V_{IN}=±2.0 V, V_{SB}=-2.0 V, V_{ST}=+2.0 V, f_{clock}=40 MHz, 50% clock duty cycle, unless otherwise specified.

PARAMETERS	TEST CONDITIONS	TEST LEVEL	SPT7814A MIN	SPT7814A TYP	SPT7814A MAX	SPT7814B MIN	SPT7814B TYP	SPT7814B MAX	UNITS
Dynamic Performance									
Signal-To-Noise Ratio (without Harmonics)									
fin=1 MHz	+25 °C	I	55	57		52	54		dB
	$T_A=T_{min}$ - T_{max}	IV	53	55		50	52		dB
fin=3.58 MHz	+25 °C	I	55	57		52	54		dB
	$T_A=T_{min}$ - T_{max}	IV	53	55		50	52		dB
fin=10.3 MHz	+25 °C	I	48	50		46	48		dB
	$T_A=T_{min}$ - T_{max}	IV	45	47		43	45		dB
Harmonic Distortion[2]									
fin=1 MHz	+25 °C	I	54	56		52	54		dB
	$T_A=T_{min}$ - T_{max}	IV	51	53		49	51		dB
fin=3.58 MHz	+25 °C	I	54	56		52	54		dB
	$T_A=T_{min}$ - T_{max}	IV	51	53		49	51		dB
fin=10.3 MHz	+25 °C	I	46	48		43	45		dB
	$T_A=T_{min}$ - T_{max}	IV	45	47		41	43		dB
Signal-to-Noise and Distortion									
fin=1 MHz	+25 °C	I	52	54		49	51		dB
	$T_A=T_{min}$ - T_{max}	IV	49			46			dB
fin=3.58 MHz	+25 °C	I	52	54		49	51		dB
	$T_A=T_{min}$ - T_{max}	IV	49			46			dB
fin=10.3 MHz	+25 °C	I	44	46		41	43		dB
	$T_A=T_{min}$ - T_{max}	IV	43			40			dB
Spurious Free Dynamic Range	+25 °C, fin=1 MHz	V		67			67		dB
Differential Phase	+25 °C, fin=3.58 & 4.35 MHz	V		0.2			0.2		Degree
Differential Gain	+25 °C, fin=3.58 & 4.35 MHz	V		0.5			0.7		%
Digital Inputs									
Logic "1" Voltage		V	-1.1			-1.1			V
Logic "0" Voltage		V			-1.5			-1.5	V
Maximum Input Current Low		VI	-500	±200	+750	-500	±200	+750	µA
Maximum Input Current High		VI	-500	±300	+750	-500	+300	+750	µA
Pulse Width Low (CLK)		IV	10			10			ns
Pulse Width High (CLK)		IV	10		300	10		300	ns
Digital Outputs									
Logic "1" Voltage	50 Ω to -2 V	VI	-1.1	-0.8		-1.1	-0.8		V
Logic "0" Voltage	50 Ω to -2 V	VI		-1.8	-1.5		-1.8	-1.5	V
Power Supply Requirements									
Voltages V_{CC}		IV	+4.75	-5.0	+5.25	+4.75	+5.0	+5.25	V
$-V_{EE}$		IV	-4.95	-5.2	-5.45	-4.95	-5.2	-5.45	V
Currents I_{CC}		II		140	170		140	190	mA
$-I_{EE}$		II		115	140		115	160	mA
Power Dissipation	Outputs Open	II		1.3	1.6		1.3	1.8	W
Power Supply Rejection Ratio	(5 V ±0.25 V, -5.2 V ±2.0 V)	V		1.0			1.0	LSB	

[2] 64 distortion BINS from 4096 pt FFT.

Figure 1A: Timing Diagram

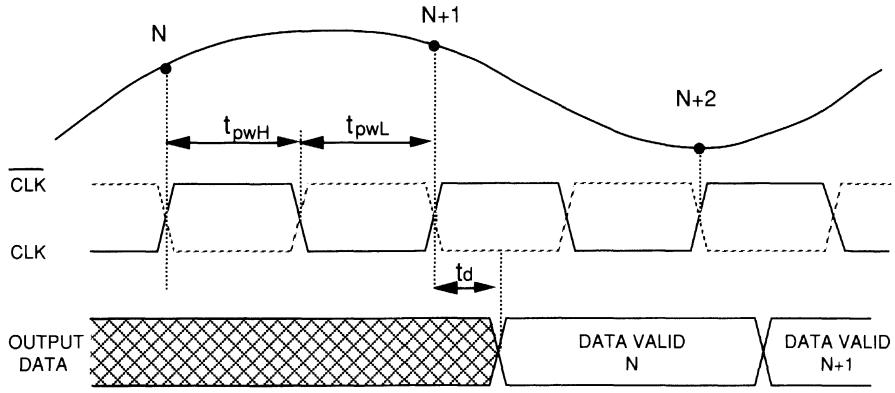

Figure 1B: Single Event Clock

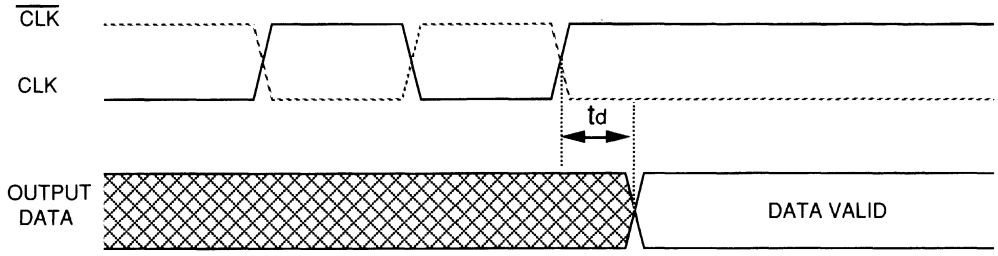

Table 1 - Timing Parameters

PARAMETERS	DESCRIPTION	MIN	TYP	MAX	UNITS
t_d	CLK to Data Valid Prop Delay	-	14	18	ns
t_{pwH}	CLK High Pulse Width	10	-	300	ns
t_{pwL}	CLK Low Pulse Width	10	-	-	ns

TEST LEVEL CODES

All electrical characteristics are subject to the following conditions:

All parameters having min/max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality Assurance inspection. Any blank section in the data column indicates that the specification is not tested at the specified condition.

Unless otherwise noted, all tests are pulsed tests; therefore, $T_J = T_C = T_A$.

TEST LEVEL	TEST PROCEDURE
I	100% production tested at the specified temperature.
II	100% production tested at T_A=25 °C, and sample tested at the specified temperatures.
III	QA sample tested only at the specified temperatures.
IV	Parameter is guaranteed (but not tested) by design and characterization data.
V	Parameter is a typical value for information purposes only.
VI	100% production tested at T_A = 25 °C. Parameter is guaranteed over specified temperature range.

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SPECIFICATION DEFINITIONS

APERTURE DELAY

Aperture delay represents the point in time, relative to the rising edge of the CLOCK input, that the analog input is sampled.

APERTURE JITTER

The variations in aperture delay for successive samples.

DIFFERENTIAL GAIN (DG)

A signal consisting of a sine wave superimposed on various DC levels is applied to the input. Differential gain is the maximum variation in the sampled sine wave amplitudes at these DC levels.

DIFFERENTIAL PHASE (DP)

A signal consisting of a sine wave superimposed on various DC levels that is applied to the input. Differential phase is the variation in the sampled sine wave phases at these DC levels.

EFFECTIVE NUMBER OF BITS (ENOB)

SINAD = 6.02N + 1.76, where N is equal to the effective number of bits.

$$N = \frac{SINAD - 1.76}{6.02}$$

+/- FULL-SCALE ERROR (GAIN ERROR)

Difference between measured full scale response [(+Fs) - (-Fs)] and the theoretical response (+4 V -2 LSBs) where the +FS (full scale) input voltage is defined as the output transition between 1-10 and 1-11 and the -FS input voltage is defined as the output transition between 0-00 and 0-01.

INPUT BANDWIDTH

Small signal (50 mV) bandwidth (3 dB) of analog input stage.

DIFFERENTIAL NONLINEARITY (DNL)

Error in the width of each code from its theoretical value. (Theoretical = $V_{FS}/2^N$)

INTEGRAL NONLINEARITY (INL)

Linearity error refers to the deviation of each individual code (normalized) from a straight line drawn from -Fs through +Fs. The deviation is measured from the edge of each particular code to the true straight line.

OUTPUT DELAY

Time between the clock's triggering edge and output data valid.

OVERVOLTAGE RECOVERY TIME

The time required for the ADC to recover to full accuracy after an analog input signal 125% of full scale is reduced to 50% of the full-scale value.

SIGNAL-TO-NOISE RATIO (SNR)

The ratio of the fundamental sinusoid power to the total noise power. Harmonics are excluded.

SIGNAL-TO-NOISE AND DISTORTION (SINAD)

The ratio of the fundamental sinusoid power to the total noise and distortion power.

TOTAL HARMONIC DISTORTION (THD)

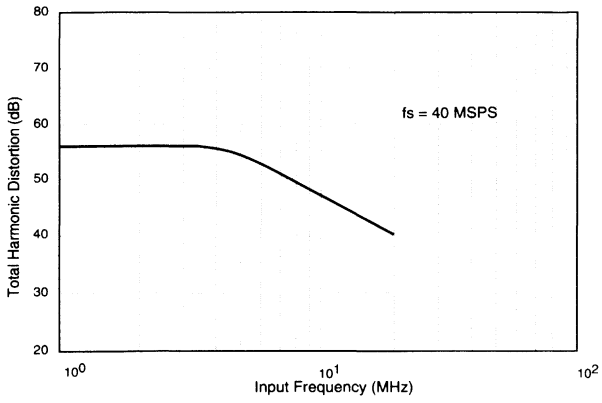
The ratio of the total power of the first 64 harmonics to the power of the measured sinusoidal signal.

SPURIOUS FREE DYNAMIC RANGE (SFDR)

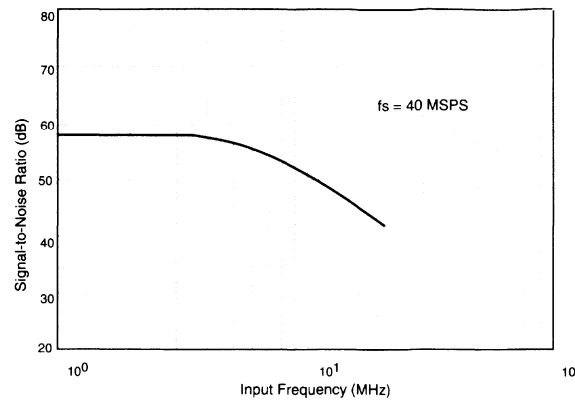
The ratio of the fundamental sinusoidal amplitude to the single largest harmonic or spurious signal.

PERFORMANCE CHARACTERISTICS

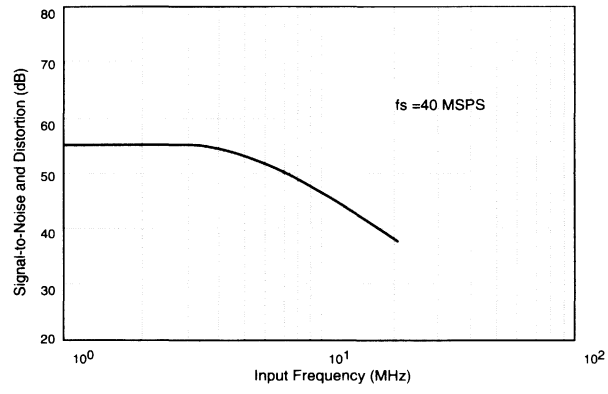
THD vs Input Frequency



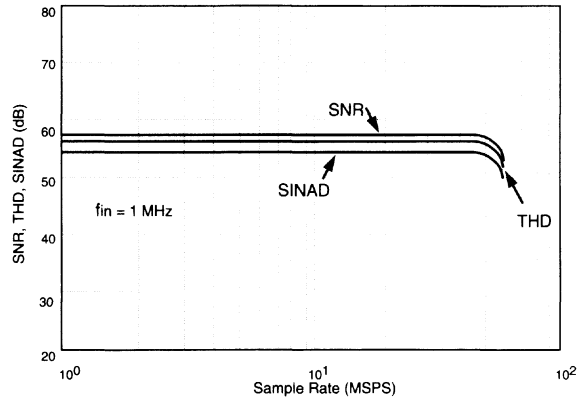
SNR vs Input Frequency



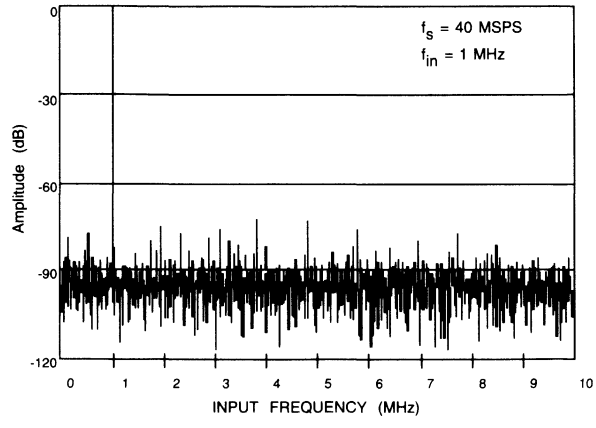
SINAD vs Input Frequency



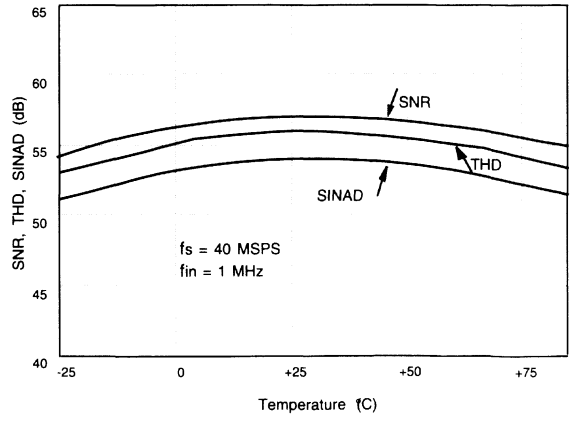
SNR, THD, SINAD vs Sample Rate



Spectral Response



SNR, THD, SINAD vs Temperature



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TYPICAL INTERFACE CIRCUIT

The SPT7814 requires few external components to achieve the stated operation and performance. Figure 2 shows the typical interface requirements when using the SPT7814 in normal circuit operation.

The following section provides a description of the pin functions and outlines critical performance criteria to consider for achieving the optimal device performance.

POWER SUPPLIES AND GROUNDING

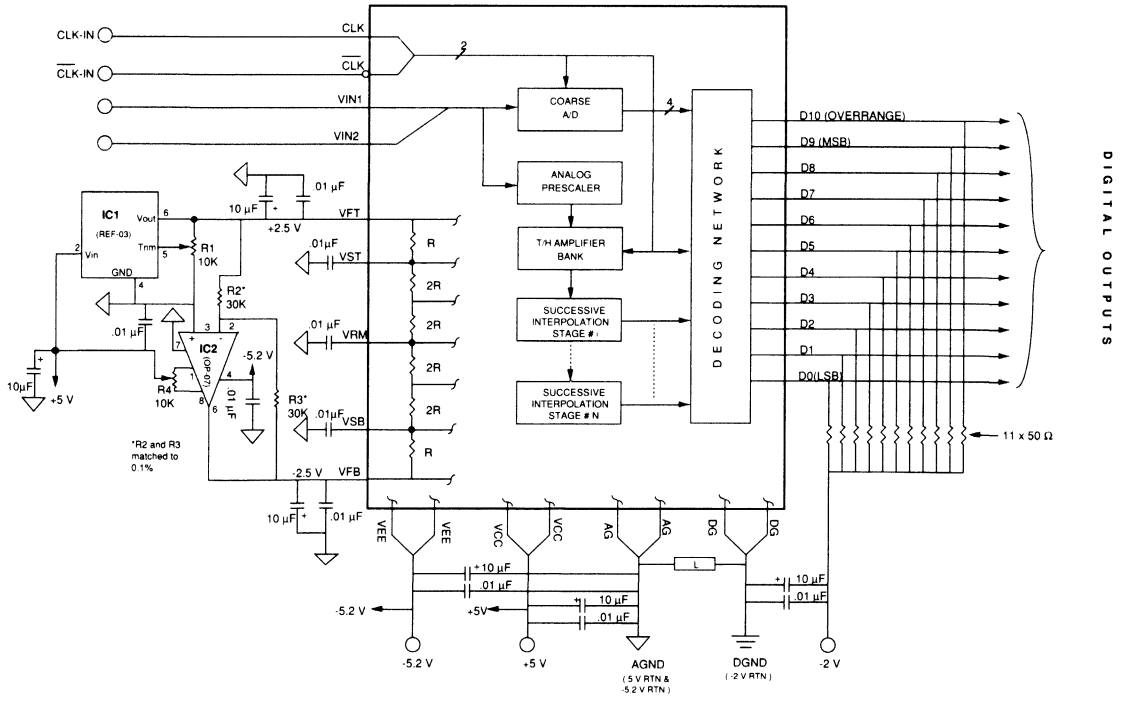
The SPT7814 requires the use of two supply voltages, V_{EE} and V_{CC}. Both supplies should be treated as analog supply sources. This means the V_{EE} and V_{CC} ground returns of the device should both be connected to the analog ground plane. All other -5.2 V requirements of the external digital logic circuit should be connected to the digital ground plane. Each power supply pin should be bypassed as closely as possible to the device with .01 µF and 10 µF capacitors as shown in Figure 2.

The two grounds available on the SPT7814 are AGND and DGND. DGND is used only for ECL outputs and is to be referenced to the output pulldown voltage. These grounds are not tied together internal to the device. The use of ground planes is recommended to achieve the best performance of the SPT7814. The AGND and the DGND ground planes should be separated from each other and only connected together at the device through an inductance. Doing this will minimize the ground noise pickup.

VOLTAGE REFERENCE

The SPT7814 requires the use of two voltage references: V_{FT} and V_{FB}. V_{FT} is the force for the top of the voltage reference ladder (+2.5 V typ), V_{FB} (-2.5 V typ) is the force for the bottom of the voltage reference ladder. Both voltages are applied across an internal reference ladder resistance of 800 ohms. In addition, there are 3 reference ladder taps (V_{ST},V_{RM} and V_{SB}). V_{ST} is the sense for the top of the reference ladder (+2.0 V), V_{RM} is the midpoint of the ladder (0.0 V typ) and V_{SB} is the sense for the bottom of the reference ladder (-2.0 V). The voltages seen at V_{ST} and V_{SB} are the true full scale input voltages of the device when V_{FT} and V_{FB} are driven to the recommended voltages (+2.5 V and -2.5 V typical respectively). These points should be used to monitor the actual full scale input voltage of the device and should not be driven to the expected ideal values as is commonly done with standard flash converters. When not being used, a decoupling capacitor of .01 uF connected to AGND from each tap is recommended to minimize high frequency noise injection.

Figure 2 - Typical Interface Circuit



An example of a reference driver circuit recommended is shown in figure 2. IC1 is REF-03, the +2.5 V reference with a tolerance of 0.6% or +/- 0.015 V. The potentiometer R1 is 10k ohms and supports a minimum adjustable range of up to 150 mV. IC2 is recommended to be an OP-07 or equivalent device. R2 and R3 must be matched to within 0.1% with good TC tracking to maintain a 0.3 LSB matching between V_{FT} and V_{FB}. If 0.1% matching is not met, then potentiometer R4 can be used to adjust the V_{FB} voltage to the desired level. R1 and R4 should be adjusted such that V_{ST} and V_{SB} are exactly +2.0 V and -2.0V respectively.

The analog input range will scale proportionally with respect to the reference voltage if a different input range is required. The maximum scaling factor for device operation is ± 10% of the recommended reference voltages of V_{FT} and V_{FB}. However, because the device is laser trimmed to optimize performance with ± 2.5 V references, the accuracy of the device will degrade if operated beyond a ± 2% range.

The following errors are defined:
+FS error = top of ladder offset voltage = Δ(+FS -V_{ST}+1 LSB)
-FS error = bottom of ladder offset voltage = Δ(-FS -V_{SB}-1 LSB)
where the +FS (full scale) input voltage is defined as the output transition between 1-10 and 1-11 and the -FS input voltage is defined as the output transition between 0-00 and 0-01.

ANALOG INPUT

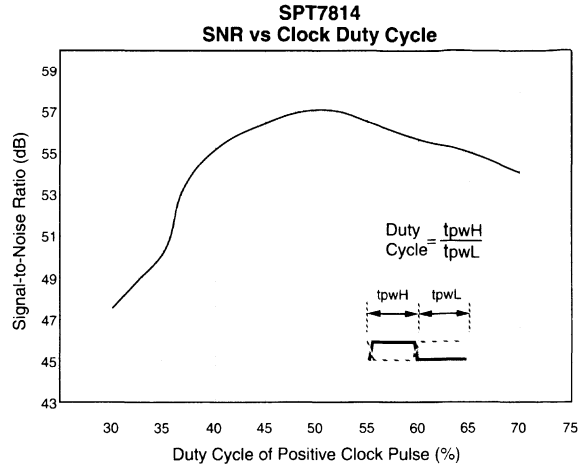
V_{IN1} and V_{IN2} are the analog inputs. Both inputs are tied to the same point internally. Either one may be used as an analog input "sense" and the other for an input "force." The inputs can also be tied together and driven from the same source. The full scale input range will be 80% of the reference voltage or ±2 volts with V_{FB}=-2.5 V and V_{FT}=+2.5 V.

The drive requirements for the analog inputs are minimal when compared to conventional Flash converters due the SPT7814's extremely low input capacitance of only 5 pF and very high input resistance of 300 kΩ. For example, for an input signal of ± 2 V p-p with an input frequency of 10 MHz, the peak output current required for the driving circuit is only 628 μA.

CLOCK INPUT

The clock inputs (CLK, $\overline{CLK}$) are designed to be driven differentially with ECL levels. The clock may be driven single ended since $\overline{CLK}$ is internally biased to -1.3 V. $\overline{CLK}$ may be left open, but a .01 μF bypass capacitor to AGND is recommended. As with all high speed circuits, proper terminations are required to avoid signal reflections and possible ringing that can cause the device to trigger at an unwanted time.

The CLK pulse width (tpwH) must be kept between 10 ns and 300 ns to ensure proper operation of the internal track-and-hold amplifier. (See timing diagram.) When operating the SPT7814 at sampling rates above 3 MSPS, it is recommended that the clock input duty cycle be kept at 50% to optimize performance. (See graph.) The analog input signal is latched on the rising edge of the CLK.



DIGITAL OUTPUTS

The format of the output data (D0-D9) is straight binary. These outputs are ECL with the output circuit shown in Figure 4. The outputs are latched on the rising edge of CLK with a propagation delay of 4 ns. There is a one clock cycle latency between CLK and the valid output data (see timing diagram). These digital outputs can drive 50 ohms to ECL levels when pulled down to -2 V. The total specified power dissipation of the device does not include the power used by these loads. The additional power used by these loads can vary between 10 and 300 mW typically (including the overrange load) depending on the output codes. If lower power levels are desired, the output loads can be reduced, but careful consideration to the capacitive loads in relation to the operating frequency must be considered.

Table 2 - Output Data Information

ANALOG INPUT	OVERRANGE D1O	OUTPUT CODE D9-DO
>+2.0 V + 1/2 LSB	1	11 1111 1111
+2.0 V -1 LSB	O	11 1111 111Ø
0.0 V	O	ØØ ØØØØ ØØØØ
-2.0 V +1 LSB	O	OO OOOO OOOØ
<2.0 V	O	OO OOOO OOOO

(Ø indicates the flickering bit between logic 0 and 1).

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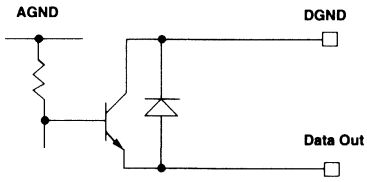
Figure 3 - Output Circuit



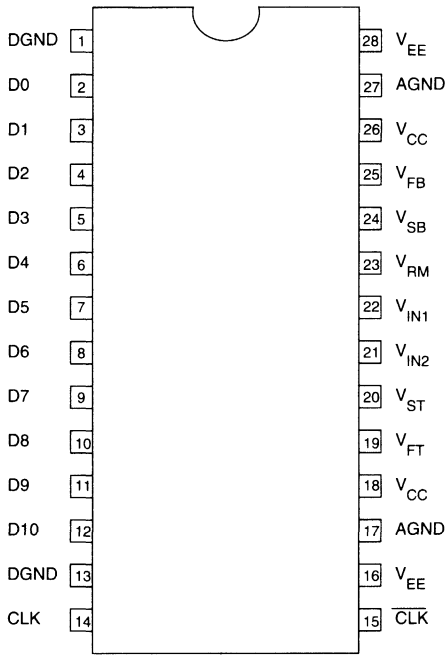
OVERRANGE OUTPUT

The OVERRANGE OUTPUT (D10) is an indication that the analog input signal has exceeded the positive full scale input voltage by 1 LSB. When this condition occurs, D10 will switch to logic 1. All other data outputs (D0 to D9) will remain at logic 1 as long as D10 remains at logic 1. This feature makes it possible to include the SPT7814 into higher resolution systems.

EVALUATION BOARD

The EB7814 Evaluation Board is available to aid designers in demonstrating the full performance of the SPT7814. This board includes a reference circuit, clock driver circuit, output data latches and an on-board reconstruction of the digital data. An application note describing the operation of this board as well as information on the testing of the SPT7814 is also available. Contact the factory for price and availability.

PIN ASSIGNMENT



PIN FUNCTIONS

NAME	FUNCTION
DGND	Digital Ground
D0-D9	ECL Outputs (D0=LSB)
D10	ECL Output Overrange
CLK	Clock Input
$\overline{CLK}$	Inverted Clock Input
V_{EE}	-5.2 V Supply
AGND	Analog Ground
V_{CC}	+5.0 V supply
V_{IN1}, V_{IN2}	Inputs (tied together at the die)
V_{FT}	Force for Top of Reference Ladder
V_{ST}	Sense for Top of Reference Ladder
V_{FB}	Force for Bottom of Reference Ladder
V_{SB}	Sense for Bottom of Reference Ladder
V_{RM}	Middle of Reference Ladder

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LEADERSHIP IN DATA CONVERSION AND SIGNAL PROCESSING

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SIGNAL PROCESSING TECHNOLOGIES

SPT7820

10-BIT, 20 MSPS, TTL OUTPUT, A/D CONVERTER

FEATURES

- Monolithic 20 MSPS Converter
- On-Chip Track/Hold
- Bipolar ±2.0 V Analog Input
- 60 dB SNR @ 1 MHz Input
- Low Power (1.0 W Typical)
- 5 pF Input Capacitance
- TTL Outputs

APPLICATIONS

- Medical Imaging
- Professional Video
- Radar Receivers
- Instrumentation
- Electronic Warfare
- Digital Communications

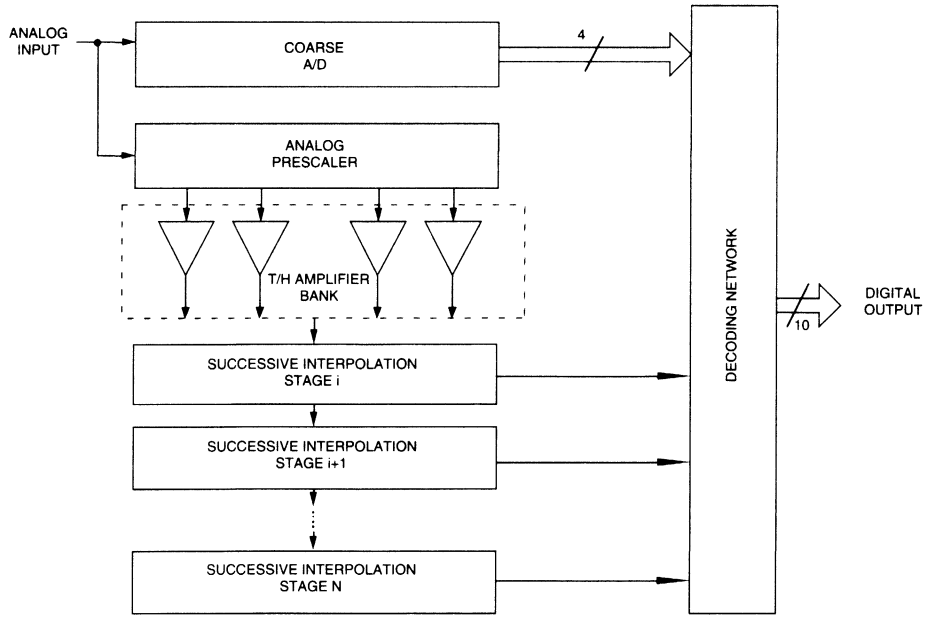
GENERAL DESCRIPTION

The SPT7820 A/D converter is a 10-bit monolithic converter capable of word rates of a mimimum of 20 MSPS. On board track/hold function assures excellent dynamic performance without the need for external components. Drive requirement problems are minimized with an input capacitance of only 5 pF.

Inputs and outputs are TTL compatible to interface with TTL logic systems. An overrange output signal is provided to indicate overflow conditions. Output data format is straight binary. Power dissipation is very low at only 1.0 watt with power supply voltages of +5.0 and -5.2 volts. The SPT7820 also provides a wide input voltage swing of ±2.0 volts.

The SPT7820 is available in a small 28-lead ceramic sidebrazed DIP, PDIP, LCC, SOIC, and die form. Commercial, industrial and military temperature ranges are currently offered. Contact the factory for availability of /883 processed units.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Beyond which damage may occur)[1] 25 °C

Supply Voltages

V_{CC} ..... +6 V
V_{EE} ..... -6 V

Input Voltages

Analog Input ..... $V_{FB} \leq V_{IN} \leq V_{FT}$
V_{FT}, V_{FB} ..... +3.0 V, -3.0 V
Reference Ladder Current ..... 12 mA
CLK Input ..... V_{CC}

Output

Digital Outputs ..... +30 to -30 mA

Temperature

Operating Temperature ..... -55 to +125 °C
Junction Temperature[1] ..... 175 °C
Lead Temperature, (soldering 10 seconds) ..... 300 °C
Storage Temperature ..... -65 to +150 °C

Note: 1. Operation at any Absolute Maximum Rating is not implied. See Electrical Specifications for proper nominal applied conditions in typical applications.

ELECTRICAL SPECIFICATIONS

$T_A=T_{min}$ - T_{max}, V_{CC}=+5.0 V, V_{EE}=-5.2 V, DV_{CC}=+5.0 V, V_{IN}=±2.0 V, V_{SB}=-2.0 V, V_{ST}=+2.0 V, f_{clock}=20 MHz, 50% clock duty cycle, unless otherwise specified.

PARAMETERS	TEST CONDITIONS	TEST LEVEL	SPT7820A MIN	SPT7820A TYP	SPT7820A MAX	SPT7820B MIN	SPT7820B TYP	SPT7820B MAX	UNITS
Resolution			10			10			Bits
DC Accuracy (+25 °C)	+/- Full Scale								
Integral Nonlinearity	250 kHz Sample Rate	I		±1.0			±1.5		LSB
Differential Nonlinearity		I		±0.5			±0.75		LSB
No Missing Codes				Guaranteed			Guaranteed		
Analog Input									
Input Voltage Range		VI		±2.0			±2.0		V
Input Bias Current	V_{IN}=0 V	VI		30	60		30	60	µA
Input Bias Current	T_A=-55 to +125 °C	VI			75			75	µA
Input Resistance		VI	100	300		100	300		kΩ
Input Resistance	-55 to +125 °C	VI	75	300		75	300		kΩ
Input Capacitance		V		5			5		pF
Input Bandwidth	3 dB Small Signal	V		120			120		MHz
+FS Error		V		±2.0			±2.0		LSB
-FS Error		V		±2.0			±2.0		LSB
Reference Input									
Reference Ladder Resistance		VI	500	800		500	800		Ω
Reference Ladder Tempco		V		0.8			0.8		Ω/°C
Timing Characteristics									
Maximum Conversion Rate		VI	20			20			MHz
Overvoltage Recovery Time		V		20			20		ns
Pipeline Delay (Latency)		VI			1			1	Clock Cycle
Output Delay	T_A=+25 °C	V		14	18		14	18	ns
Aperture Delay Time	T_A=+25 °C	V		1			1		ns
Aperture Jitter Time	T_A=+25 °C	V		5			5		ps-RMS
Acquisition Time	T_A=+25 °C	V		20			20		ns
Dynamic Performance									
Effective Number of Bits									
fin=1 MHz				9.2			8.7		Bits
fin=3.58 MHz				8.8			8.3		Bits
fin=10.3 MHz				7.5			7.0		Bits

[1] Typical thermal impedances (unsoldered, in free air): 28L sidebrazed DIP. θ_{ja} = 50 °C/W, 28L LCC θ_{ja} = 99 °C/W, 28L plastic DIP θ_{ja} = 50°C/W, SOIC θ_{ja} = 100 °C/W.

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ELECTRICAL SPECIFICATIONS

$T_A=T_{min}$ - T_{max}, V_{CC}=+5.0 V, V_{EE}=-5.2 V, DV_{CC}=+5.0 V, V_{IN}=±2.0 V, V_{SB}=-2.0 V, V_{ST}=+2.0 V, f_{clock}=20 MHz, 50% clock duty cycle, unless otherwise specified.

PARAMETERS	TEST CONDITIONS	TEST LEVEL	SPT7820A MIN	SPT7820A TYP	SPT7820A MAX	SPT7820B MIN	SPT7820B TYP	SPT7820B MAX	UNITS
Dynamic Performance									
Signal-To-Noise Ratio (without Harmonics)									
fin=1 MHz	+25 °C	I	57	60		54	57		dB
	(0-70, -25 to +85 °C)	IV	55	58		52	55		dB
	-55 to +125 °C	I	52	55		49	52		dB
fin=3.58 MHz	+25 °C	I	56	58		53	55		dB
	(0-70, -25 to +85 °C)	IV	54	56		51	53		dB
	-55 to +125 °C	I	52	54		49	51		dB
fin=10.3 MHz	+25 °C	I	50	53		47	49		dB
	(0-70, -25 to +85 °C)	IV	47	50		44	46		dB
	-55 to +125 °C	I	43	46		40	42		dB
Harmonic Distortion[2]									
fin=1 MHz	+25 °C	I	57	60		54	57		dB
	(0-70, -25 to +85 °C)	IV	54	57		51	54		dB
	-55 to +125 °C	I	50	53		47	50		dB
fin=3.58 MHz	+25 °C	I	56	58		53	55		dB
	(0-70, -25 to +85 °C)	IV	53	55		50	52		dB
	-55 to +125 °C	I	50	52		47	49		dB
fin=10.3 MHz	+25 °C	I	46	48		43	45		dB
	(0-70, -25 to +85 °C)	IV	45	47		42	44		dB
	-55 to +125 °C	I	45	47		42	44		dB
Signal-to-Noise and Distortion									
fin=1 MHz	+25 °C	I	55	57		52	54		dB
	(0-70, -25 to +85 °C)	IV	52			49			dB
	-55 to +125 °C	I	48			45			dB
fin=3.58 MHz	+25 °C	I	54	55		51	52		dB
	(0-70, -25 to +85 °C)	IV	51			48			dB
	-55 to +125 °C	I	48			45			dB
fin=10.3 MHz	+25 °C	I	44	47		41	44		dB
	(0-70, -25 to +85 °C)	IV	43			40			dB
	-55 to +125 °C	I	41			38			dB
Spurious Free Dynamic Range	+25 °C, fin = 1 MHz	V		67			67		dB
Differential Phase	+25 °C, fin = 3.58 & 4.35 MHz	V		0.2			0.2		Degree
Differential Gain	+25 °C, fin = 3.58 & 4.35 MHz	V		0.5			0.7		%
Digital Inputs									
Logic "1" Voltage		V	2.4		4.5	2.4		4.5	V
Logic "0" Voltage		V			0.8			0.8	V
Maximum Input Current Low		IV	0	+5	+20	0	+5	+20	µA
Maximum Input Current High		IV	0	+5	+20	0	+5	+20	µA
Pulse Width Low (CLK)		IV	20			20			ns
Pulse Width High (CLK)		IV	20		300	20		300	ns
Digital Outputs									
Logic "1" Voltage		IV	2.4			2.4			V
Logic "0" Voltage		IV			0.6			0.6	V
Power Supply Requirements									
Voltages V_{CC}		IV	4.75		5.25	4.75		5.25	V
DV_{CC}		IV	4.75	5.0	5.25	4.75	5.0	5.25	V
$-V_{EE}$		IV	-4.95	-5.2	-5.45	-4.95	-5.2	-5.45	V
Currents I_{CC}		IV		118	145		118	145	mA
DI_{CC}		IV		40	55		40	55	mA
$-I_{EE}$		IV		40	57		40	57	mA
Power Dissipation		VI		1.0	1.3		1.0	1.3	W
Power Supply Rejection	(5 V ±0.25 V, -5.2 ±0.25 V)	V		1.0			1.0		LSB

[2] 64 distortion BINS from 4096 pt FFT.

Figure 1A: Timing Diagram

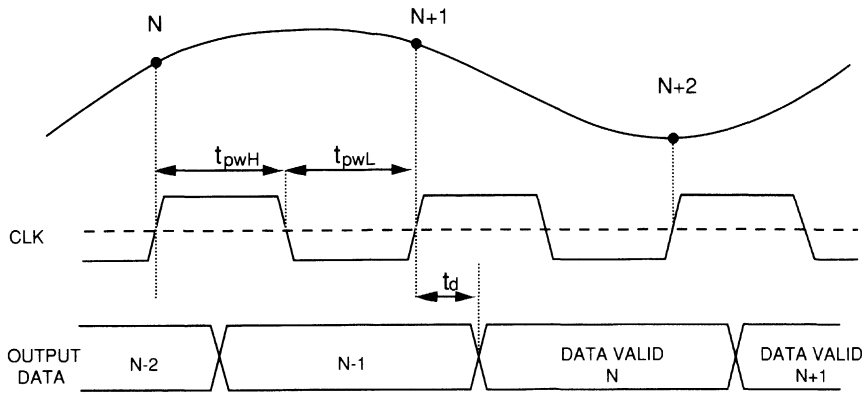

Figure 1B: Single Event Clock

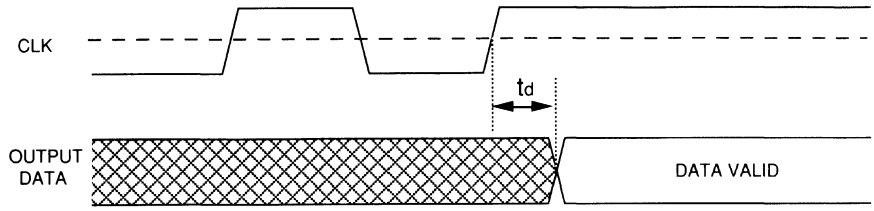

Table 1 - Timing Parameters

PARAMETERS	DESCRIPTION	MIN	TYP	MAX	UNITS
t_d	CLK to Data Valid Prop Delay	-	14	18	ns
t_{pwH}	CLK High Pulse Width	20	-	300	ns
t_{pwL}	CLK Low Pulse Width	20	-	-	ns

TEST LEVEL CODES

All electrical characteristics are subject to the following conditions:

All parameters having min/max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality Assurance inspection. Any blank section in the data column indicates that the specification is not tested at the specified condition.

Unless otherwise noted, all tests are pulsed tests; therefore, $T_J = T_C = T_A$.

TEST LEVEL	TEST PROCEDURE
I	100% production tested at the specified temperature.
II	100% production tested at T_A=25 °C, and sample tested at the specified temperatures.
III	QA sample tested only at the specified temperatures.
IV	Parameter is guaranteed (but not tested) by design and characterization data.
V	Parameter is a typical value for information purposes only.
VI	100% production tested at T_A = 25 °C. Parameter is guaranteed over specified temperature range.

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SPECIFICATION DEFINITIONS

APERTURE DELAY

Aperture delay represents the point in time, relative to the rising edge of the CLOCK input, that the analog input is sampled.

APERTURE JITTER

The variations in aperture delay for successive samples.

DIFFERENTIAL GAIN (DG)

A signal consisting of a sine wave superimposed on various DC levels is applied to the input. Differential gain is the maximum variation in the sampled sine wave amplitudes at these DC levels.

DIFFERENTIAL PHASE (DP)

A signal consisting of a sine wave superimposed on various DC levels that is applied to the input. Differential phase is the maximum variation in the sampled sine wave phases at these DC levels.

EFFECTIVE NUMBER OF BITS (ENOB)

SINAD = 6.02N + 1.76, where N is equal to the effective number of bits.

$$N = \frac{SINAD - 1.76}{6.02}$$

+/- FULL-SCALE ERROR (GAIN ERROR)

Difference between measured full scale response [(+Fs) - (-Fs)] and the theoretical response (+4 V -2 LSBs) where the +FS (full scale) input voltage is defined as the output transition between 1-10 and 1-11 and the -FS input voltage is defined as the output transition between 0-00 and 0-01.

INPUT BANDWIDTH

Small signal (50 mV) bandwidth (3 dB) of analog input stage.

DIFFERENTIAL NONLINEARITY (DNL)

Error in the width of each code from its theoretical value. (Theoretical = $V_{FS}/2^N$)

INTEGRAL NONLINEARITY (INL)

Linearity error refers to the deviation of each individual code (normalized) from a straight line drawn from -Fs through +Fs. The deviation is measured from the edge of each particular code to the true straight line.

OUTPUT DELAY

Time between the clock's triggering edge and output data valid.

OVERVOLTAGE RECOVERY TIME

The time required for the ADC to recover to full accuracy after an analog input signal 125% of full scale is reduced to 50% of the full-scale value.

SIGNAL-TO-NOISE RATIO (SNR)

The ratio of the fundamental sinusoid power to the total noise power. Harmonics are excluded.

SIGNAL-TO-NOISE AND DISTORTION (SINAD)

The ratio of the fundamental sinusoid power to the total noise and distortion power.

TOTAL HARMONIC DISTORTION (THD)

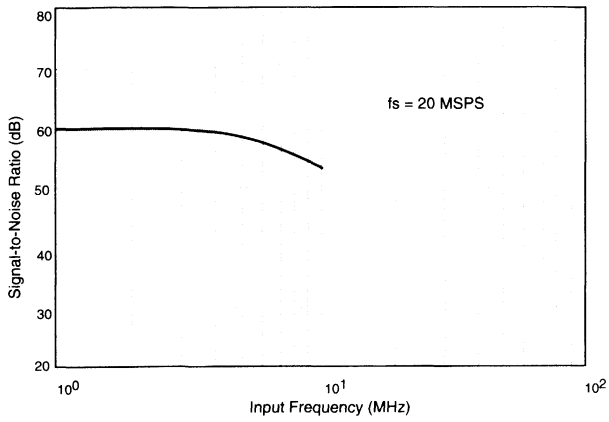
The ratio of the total power of the first 64 harmonics to the power of the measured sinusoidal signal.

SPURIOUS FREE DYNAMIC RANGE (SFDR)

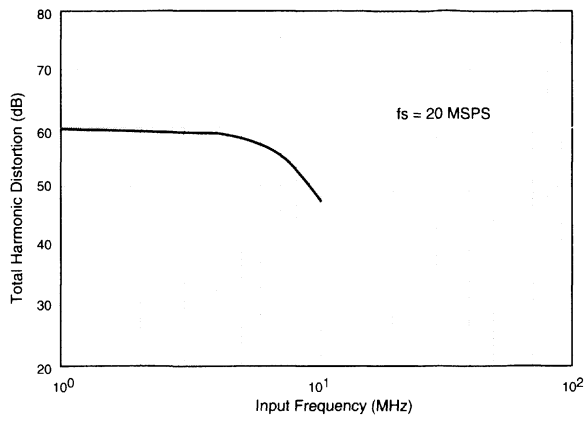
The ratio of the fundamental sinusoidal amplitude to the single largest harmonic or spurious signal.

PERFORMANCE CHARACTERISTICS

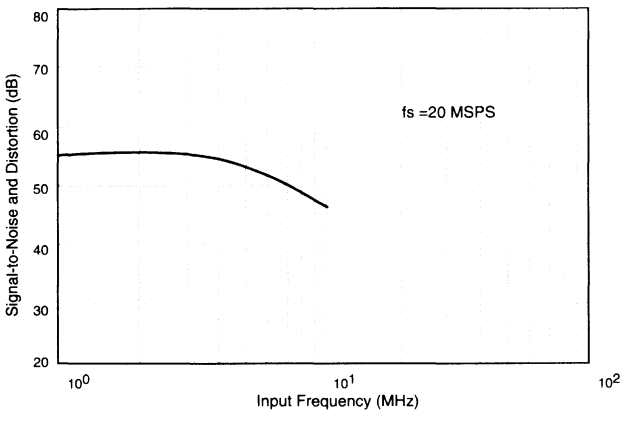
SNR vs Input Frequency



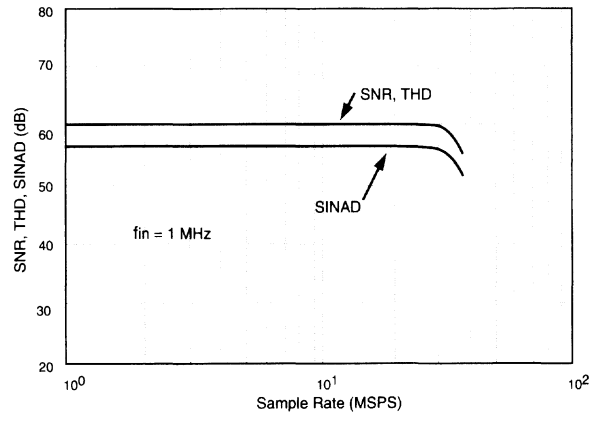
THD vs Input Frequency



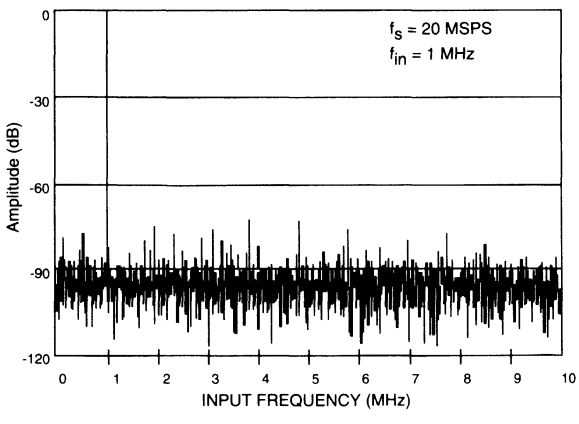
SINAD vs Input Frequency



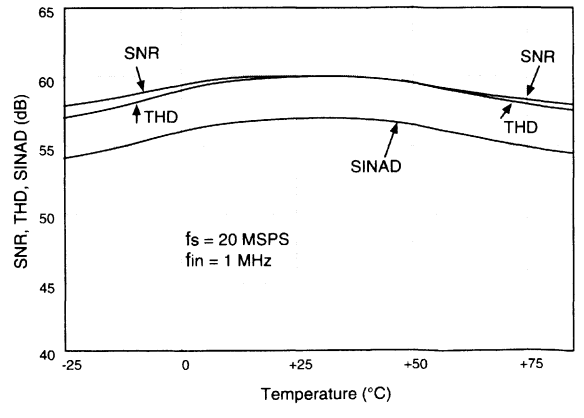
SNR, THD, SINAD vs Sample Rate



Spectral Response



SNR, THD, SINAD vs Temperature



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TYPICAL INTERFACE CIRCUIT

The SPT7820 requires few external components to achieve the stated operation and performance. Figure 2 shows the typical interface requirements when using the SPT7820 in normal circuit operation. The following section provides a description of the pin functions and outlines critical performance criteria to consider for achieving the optimal device performance.

POWER SUPPLIES AND GROUNDING

The SPT7820 requires -5.2 V and +5 V analog supply voltages. The +5 V supply is common to analog VCC and digital DVCC. A ferrite bead in series with each supply line is intended to reduce the transient noise injected into the analog VCC. These beads should be connected as closely as possible to the device. The connection between the beads and the SPT7820 should not be shared with any other device. Each power supply pin should be bypassed as closely as possible to the device. Use 0.1 µF for VEE and VCC, and 0.01 µF for DVCC (chip caps are preferred).

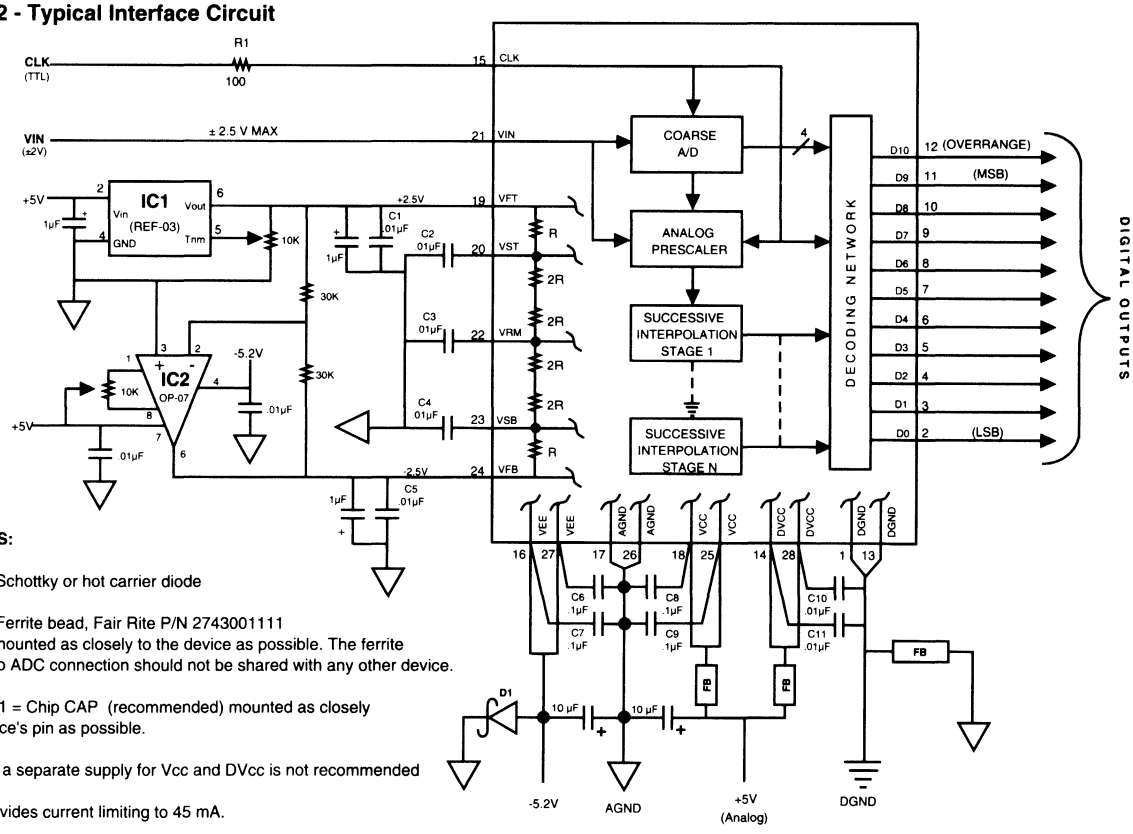
AGND and DGND are the two grounds available on the SPT7820. These two internal grounds are isolated on the device. The use of ground planes is recommended to achieve optimum device performance. DGND is needed for the DVCC return path (40 mA typical) and for the return path for all digital output logic interfaces. AGND and DGND should be separated from each other and connected together only at the device through a ferrite bead.

A Schottky or hot carrier diode connected between AGND and VEE is required. The use of separate power supplies between VCC and DVCC is not recommended due to potential power supply sequencing latch-up conditions. Using the recommended interface circuit shown in figure 2 will provide optimum device performance for the SPT7820.

VOLTAGE REFERENCE

The SPT7820 requires the use of two voltage references: V_{FT} and V_{FB}. V_{FT} is the force for the top of the voltage reference ladder (+2.5 V typ), V_{FB} (-2.5 V typ) is the force for the bottom of the voltage reference ladder. Both voltages are applied across an internal reference ladder resistance of 800 ohms. The +2.5 V voltage source for reference VFT must be current limited to 20 mA maximum if a different driving circuit is used in place of the recommended reference circuit shown in figures

Figure 2 - Typical Interface Circuit



NOTES:

1) D1 = Schottky or hot carrier diode

2) FB = Ferrite bead, Fair Rite P/N 2743001111 to be mounted as closely to the device as possible. The ferrite bead to ADC connection should not be shared with any other device.

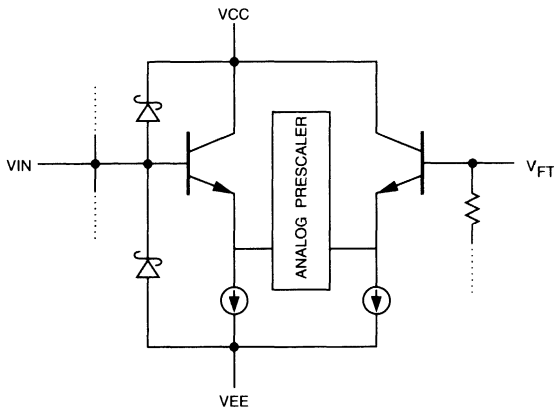
3) C1-C11 = Chip CAP (recommended) mounted as closely to device's pin as possible.

4) Use of a separate supply for Vcc and DVcc is not recommended

5) R1 provides current limiting to 45 mA.

2 and 3. In addition, there are three reference ladder taps (V_{ST}, V_{RM} and V_{SB}). V_{ST} is the sense for the top of the reference ladder (+2.0 V), V_{RM} is the midpoint of the ladder (0.0 V typ) and V_{SB} is the sense for the bottom of the reference ladder (-2.0 V). The voltages seen at V_{ST} and V_{SB} are the true full scale input voltages of the device when V_{FT} and V_{FB} are driven to the recommended voltages (+2.5 V and -2.5 V typical respectively). These points should be used to monitor the actual full scale input voltage of the device and should not be driven to the expected ideal values as is commonly done with standard flash converters. When not being used, a decoupling capacitor of .01 uF (chip cap preferred) connected to AGND from each tap is recommended to minimize high frequency noise injection.

Figure 3 - Analog Equivalent Input Circuit



An example of a reference driver circuit recommended is shown in figure 2. IC1 is REF-03, the +2.5 V reference with a tolerance of 0.6% or +/- 0.015 V. The potentiometer R1 is 10k ohms and supports a minimum adjustable range of up to 150 mV. IC2 is recommended to be an OP-07 or equivalent device. R2 and R3 must be matched to within 0.1% with good TC tracking to maintain a 0.3 LSB matching between V_{FT} and V_{FB}. If 0.1% matching is not met, then potentiometer R4 can be used to adjust the V_{FB} voltage to the desired level. V_{FT} and V_{FB} should be adjusted such that V_{ST} and V_{SB} are exactly +2.0 V and -2.0 V respectively.

The analog input range will scale proportionally with respect to the reference voltage if a different input range is required. The maximum scaling factor for device operation is ± 10% of the recommended reference voltages of V_{FT} and V_{FB}. However, because the device is laser trimmed to optimize performance with ± 2.5 V references, the accuracy of the device will degrade if operated beyond a ± 2% range.

The following errors are defined:
+FS error = top of ladder offset voltage = Δ(+FS -V_{ST}+1 LSB)
-FS error = bottom of ladder offset voltage = Δ(-FS -V_{SB}-1 LSB)
where the +FS (full scale) input voltage is defined as the output transition between 1-10 and 1-11 and the -FS input voltage is defined as the output transition between 0-00 and 0-01.

ANALOG INPUT

V_{IN} is the analog input. The full scale input range will be 80% of the reference voltage or ±2 volts with V_{FB}=-2.5 V and V_{FT}=+2.5 V.

The drive requirements for the analog inputs are minimal when compared to conventional Flash converters due to the SPT7820's extremely low input capacitance of only 5 pF and very high input resistance of 300 kΩ. For example, for an input signal of ±2 V p-p with an input frequency of 10 MHz, the peak output current required for the driving circuit is only 628 µA.

CLOCK INPUT

The SPT7820 is driven from a single-ended TTL input (CLK). The CLK pulse width (tpwH) must be kept between 20 ns and 300 ns to ensure proper operation of the internal track-and-hold amplifier. (See timing diagram.) When operating the SPT7820 at sampling rates above 3 MSPS, it is recommended that the clock input duty cycle be kept at 50% but performance will not be degraded if kept within the range of 40-60%. The analog input signal is latched on the rising edge of the CLK.

The clock input must be driven from fast TTL logic (V_{IH} ≤4.5 V, T_{RISE} <6 ns). In the event the clock is driven from a high current source, use a 100 Ω resistor in series to current limit to approximately 45 mA.

DIGITAL OUTPUTS

The format of the output data (D0-D9) is straight binary. (See table 2.) The outputs are latched on the rising edge of CLK with a propagation delay of 14 ns (typ). There is a one clock cycle latency between CLK and the valid output data. (See timing diagram.)

Table 2 - Output Data Information

ANALOG INPUT	OVERRANGE D1O	OUTPUT CODE D9-DO
>+2.0 V + 1/2 LSB	1	11 1111 1111
+2.0 V -1 LSB	O	11 1111 111Ø
0.0 V	O	ØØ ØØØØ ØØØØ
-2.0 V +1 LSB	O	OO OOOO OOOØ
<2.0 V	O	OO OOOO OOOO

(Ø indicates the flickering bit between logic 0 and 1).

The rise times and fall times of the digital outputs are not symmetrical. The propagation delay of the rise time is typically 14 ns and the fall time is typically 6 ns. (See figure 4.) The nonsymmetrical rise and fall times create approximately 8 ns of invalid data.

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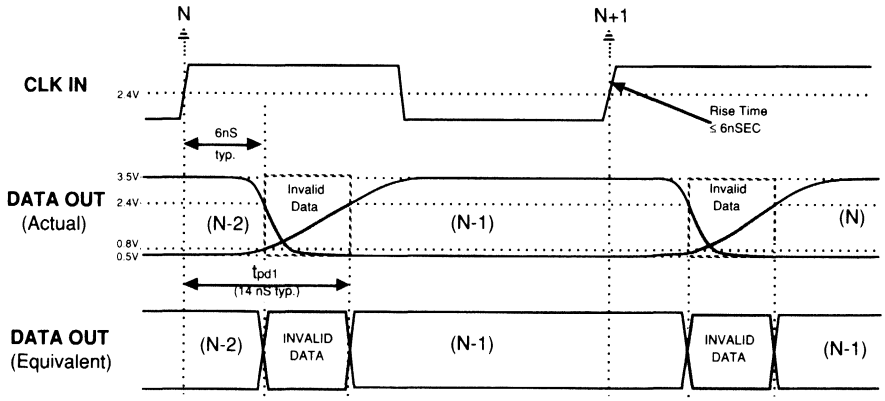
Figure 4 - Digital Output Characteristics



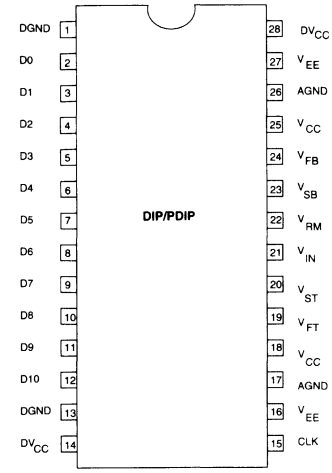
OVERRANGE OUTPUT

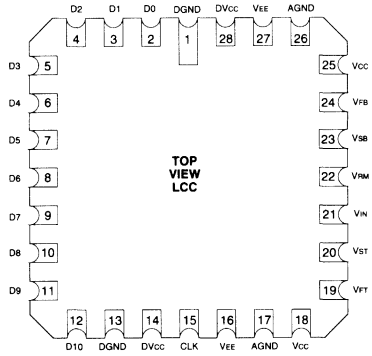
The OVERRANGE OUTPUT (D10) is an indication that the analog input signal has exceeded the positive full scale input voltage by 1 LSB. When this condition occurs, D10 will switch to logic 1. All other data outputs (D0 to D9) will remain at logic 1 as long as D10 remains at logic 1. This feature makes it possible to include the SPT7820 into higher resolution systems.

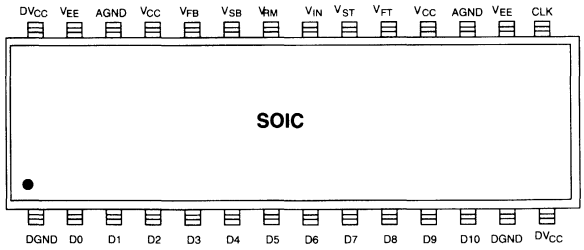
EVALUATION BOARD

The EB7820 Evaluation Board is available to aid designers in demonstrating the full performance of the SPT7820. This board includes a reference circuit, clock driver circuit, output data latches and an on-board reconstruction of the digital data. An application note describing the operation of this board as well as information on the testing of the SPT7820 is also available. Contact the factory for price and availability.

PIN ASSIGNMENT







PIN FUNCTIONS

NAME	FUNCTION
DGND	Digital Ground
D0-D9	TTL Outputs (D0=LSB)
D10	TTL Output Overrange
CLK	Clock Input
V_{EE}	-5.2 V Supply (Analog)
AGND	Analog Ground
V_{CC}	+5.0 V supply (Analog)
V_{IN}	Analog Input
DV_{CC}	Digital +5.0 V Supply
V_{RM}	Middle of Voltage Reference Ladder
V_{FT}	Force for Top of Reference Ladder
V_{ST}	Sense for Top of Reference Ladder
V_{FB}	Force for Bottom of Reference Ladder
V_{SB}	Sense for Bottom of Reference Ladder

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LEADERSHIP IN DATA CONVERSION AND SIGNAL PROCESSING

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SPT
SIGNAL PROCESSING TECHNOLOGIES

SPT7824

10-BIT, 40 MSPS, TTL OUTPUT A/D CONVERTER

FEATURES

- Monolithic 40 MSPS Converter
- On-Chip Track/Hold
- Bipolar ±2.0 V Analog Input
- 57 dB SNR @ 3.58 MHz Input
- Low Power (1.0 W Typical)
- 5 pF Input Capacitance
- TTL Outputs

APPLICATIONS

- Medical Imaging
- Professional Video
- Radar Receivers
- Instrumentation
- Electronic Warfare
- Digital Communications

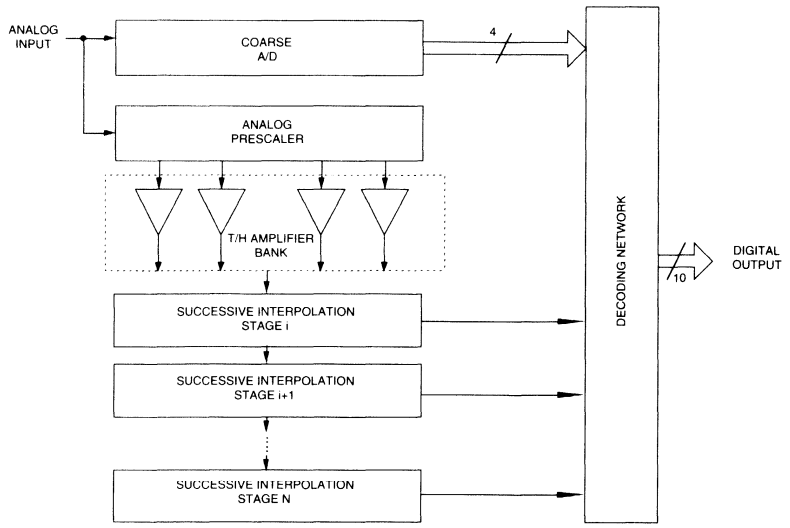
GENERAL DESCRIPTION

The SPT7824 A/D converter is a 10-bit monolithic converter capable of word rates a minimum of 40 MSPS. On board track/hold function assures excellent dynamic performance without the need for external components. Drive requirement problems are minimized with an input capacitance of only 5 pF.

Inputs and outputs are TTL compatible to interface with TTL logic systems. An overrange output signal is provided to indicate overflow conditions. Output data format is straight binary. Power dissipation is very low at only 1.0 watt with power supply voltages of +5.0 and -5.2 volts. The SPT7824 also provides a wide input voltage swing of ±2.0 volts.

The SPT7824 is available in a small 28-lead ceramic sidebrazed DIP, PDIP, LCC, SOIC, and die form. Commercial, industrial and military temperature ranges are currently offered. Contact the factory for availability of /883 processed units.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Beyond which damage may occur)[1] 25 °C

Supply Voltages

V_{CC} ..... +6 V
V_{EE} ..... -6 V

Input Voltages

Analog Input ..... $V_{FB} \leq V_{IN} \leq V_{FT}$
V_{FT}, V_{FB} ..... +3.0 V, -3.0 V
Reference Ladder Current ..... 12 mA
CLK Input ..... V_{CC}

Output

Digital Outputs ..... +30 to -30 mA

Temperature

Operating Temperature ..... -55 to +125 °C
Junction Temperature[1] ..... 175 °C
Lead Temperature, (soldering 10 seconds) ..... 300 °C
Storage Temperature ..... -65 to +150 °C

Note: 1. Operation at any Absolute Maximum Rating is not implied. See Electrical Specifications for proper nominal applied conditions in typical applications.

ELECTRICAL SPECIFICATIONS

$T_A=T_{min}$ - T_{max}, V_{CC}=+5.0 V, V_{EE}=-5.2 V, DV_{CC}=+5.0 V, V_{IN}=±2.0 V, V_{SB}=-2.0 V, V_{ST}=+2.0 V, f_{clock}=40 MHz, 50% clock duty cycle, unless otherwise specified.

PARAMETERS	TEST CONDITIONS	TEST LEVEL	SPT7824A MIN	SPT7824A TYP	SPT7824A MAX	SPT7824B MIN	SPT7824B TYP	SPT7824B MAX	UNITS
Resolution			10			10			Bits
DC Accuracy (+25 °C)	+/- Full Scale								
Integral Nonlinearity	250 kHz Sample Rate	I		±1.0			±1.5		LSB
Differential Nonlinearity		I		±0.5			±0.75		LSB
No Missing Codes				Guaranteed			Guaranteed		
Analog Input									
Input Voltage Range		VI		±2.0			±2.0		V
Input Bias Current	V_{IN}=0 V	VI		30	60		30	60	µA
Input Bias Current	T_A=-55 to +125 °C	VI			75			75	µA
Input Resistance		VI	100	300		100	300		kΩ
Input Resistance	-55 to +125 °C	VI	75	300		75	300		kΩ
Input Capacitance		V		5			5		pF
Input Bandwidth	3 dB Small Signal	V		120			120		MHz
+FS Error		V		±2.0			±2.0		LSB
-FS Error		V		±2.0			±2.0		LSB
Reference Input									
Reference Ladder Resistance		VI	500	800		500	800		Ω
Reference Ladder Tempco		V		0.8			0.8		Ω/°C
Timing Characteristics									
Maximum Conversion Rate		VI	40			40			MHz
Overvoltage Recovery Time		V		20			20		ns
Pipeline Delay (Latency)		VI			1			1	Clock Cycle
Output Delay	T_A=+25 °C	V		14	18		14	18	ns
Aperture Delay Time	T_A=+25 °C	V		1			1		ns
Aperture Jitter Time	T_A=+25 °C	V		5			5		ps-RMS
Acquisition Time	T_A=+25 °C	V		12			12		ns
Dynamic Performance									
Effective Number of Bits									
fin=1 MHz				8.7			8.2		Bits
fin=3.58 MHz				8.7			8.2		Bits
fin=10.3 MHz				7.3			6.9		Bits

[1] Typical thermal impedances (unsoldered, in free air): 28L sidebrazed DIP. θ_{ja} = 50 °C/W, 28L LCC θ_{ja} = 99 °C/W, 28L plastic DIP θ_{ja} = 50°C/W, SOIC θ_{ja} = 100 °C/W.

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ELECTRICAL SPECIFICATIONS

$T_A=T_{MIN}-T_{MAX}$, V_{CC}=+5.0 V, V_{EE}=-5.2 V, DV_{CC}=+5.0 V, V_{IN}=±2.0 V, V_{SB}=-2.0 V, V_{ST}=+2.0 V, f_{clock}=40 MHz, 50% clock duty cycle unless otherwise specified.

PARAMETERS	TEST CONDITIONS	TEST LEVEL	SPT7824A MIN	SPT7824A TYP	SPT7824A MAX	SPT7824B MIN	SPT7824B TYP	SPT7824B MAX	UNITS
Dynamic Performance									
Signal-To-Noise Ratio (without Harmonics)									
fin=1 MHz	+25 °C	I	55	57		52	54		dB
	(0 to 70, -25 to +85 °C)	IV	53	55		50	52		dB
	-55 to +125 °C	I	49	51		46	48		dB
fin=3.58 MHz	+25 °C	I	55	57		52	54		dB
	(0 to 70, -25 to +85 °C)	IV	53	55		50	52		dB
	-55 to +125 °C	I	49	51		46	48		dB
fin=10.3 MHz	+25 °C	I	48	50		46	48		dB
	(0 to 70, -25 to +85 °C)	IV	45	47		43	45		dB
	-55 to +125 °C	I	41	43		39	41		dB
Harmonic Distortion[2]									
fin=1 MHz	+25 °C	I	54	56		52	54		dB
	(0 to 70, -25 to +85 °C)	IV	51	53		49	51		dB
	-55 to +125 °C	I	50	52		48	50		dB
fin=3.58 MHz	+25 °C	I	54	56		52	54		dB
	(0 to 70, -25 to +85 °C)	IV	51	53		49	51		dB
	-55 to +125 °C	I	50	52		48	50		dB
fin=10.3 MHz	+25 °C	I	46	48		43	45		dB
	(0 to 70, -25 to +85 °C)	IV	45	47		41	44		dB
	-55 to +125 °C	I	44	46		40	42		dB
Signal-to-Noise and Distortion									
fin=1 MHz	+25 °C	I	52	54		49	51		dB
	(0 to 70, -25 to +85 °C)	IV	49			46			dB
	-55 to +125 °C	I	48			45			dB
fin=3.58 MHz	+25 °C	I	52	54		49	51		dB
	(0 to 70, -25 to +85 °C)	IV	49			46			dB
	-55 to +125 °C	I	48			45			dB
fin=10.3 MHz	+25 °C	I	44	46		41	43		dB
	(0 to 70, -25 to +85 °C)	IV	43			40			dB
	-55 to +125 °C	I	40			37			dB
Spurious Free Dynamic Range	+25 °C, fin = 1 MHz	V		67			67		dB
Differential Phase	+25 °C	V		0.2			0.2		Degree
Differential Gain	+25 °C, fin = 3.58 & 4.35 MHz	V		0.5			0.7		%
Digital Inputs									
Logic "1" Voltage		V	2.4		4.5	2.4		4.5	V
Logic "0" Voltage		V			0.8			0.8	V
Maximum Input Current Low		IV	0	+5	+20	0	+5	+20	µA
Maximum Input Current High		IV	0	+5	+20	0	+5	+20	µA
Pulse Width Low (CLK)		IV	10			10			ns
Pulse Width High (CLK)		IV	10		300	10		300	ns
Digital Outputs									
Logic "1" Voltage		IV	2.4			2.4			V
Logic "0" Voltage		IV			0.6			0.6	V
Power Supply Requirements									
Voltages V_{CC}		IV	4.75		5.25	4.75		5.25	V
DV_{CC}		IV	4.75	5.0	5.25	4.75	5.0	5.25	V
$-V_{EE}$		IV	-4.95	-5.2	-5.45	-4.95	-5.2	-5.45	V
Currents I_{CC}		IV		118	145		118	145	mA
DI_{CC}		IV		40	55		40	55	mA
$-I_{EE}$		IV		40	57		40	57	mA
Power Dissipation		VI		1.0	1.3		1.0	1.3	W
Power Supply Rejection	(5 V ±0.25 V, -5.2 V ±0.25 V)	V		1.0			1.0		LSB

[2] 64 distortion BINS from 4096 pt FFT.

Figure 1A: Timing Diagram

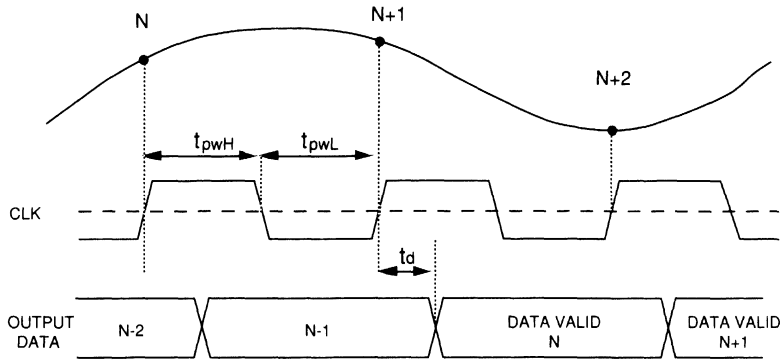

Figure 1B: Single Event Clock

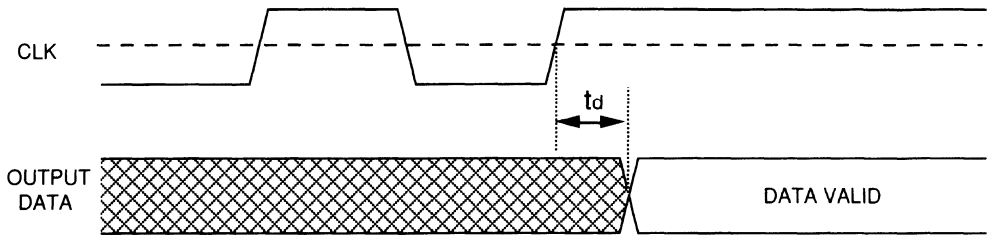

Table 1 - Timing Parameters

PARAMETERS	DESCRIPTION	MIN	TYP	MAX	UNITS
t_d	CLK to Data Valid Prop Delay	-	14	18	ns
t_{pwH}	CLK High Pulse Width	10	-	300	ns
t_{pwL}	CLK Low Pulse Width	10	-	-	ns

TEST LEVEL CODES

All electrical characteristics are subject to the following conditions:

All parameters having min/max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality Assurance inspection. Any blank section in the data column indicates that the specification is not tested at the specified condition.

Unless otherwise noted, all tests are pulsed tests; therefore, $T_J = T_C = T_A$.

TEST LEVEL	TEST PROCEDURE
I	100% production tested at the specified temperature.
II	100% production tested at T_A=25 °C, and sample tested at the specified temperatures.
iII	QA sample tested only at the specified temperatures.
IV	Parameter is guaranteed (but not tested) by design and characterization data.
V	Parameter is a typical value for information purposes only.
VI	100% production tested at T_A = 25 °C. Parameter is guaranteed over specified temperature range.

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SPECIFICATION DEFINITIONS

APERTURE DELAY

Aperture delay represents the point in time, relative to the rising edge of the CLOCK input, that the analog input is sampled.

APERTURE JITTER

The variations in aperture delay for successive samples.

DIFFERENTIAL GAIN (DG)

A signal consisting of a sine wave superimposed on various DC levels is applied to the input. Differential gain is the maximum variation in the sampled sine wave amplitudes at these DC levels.

DIFFERENTIAL PHASE (DP)

A signal consisting of a sine wave superimposed on various DC levels that is applied to the input. Differential phase is the maximum variation in the sampled sine wave phases at these DC levels.

EFFECTIVE NUMBER OF BITS (ENOB)

SINAD = 6.02N + 1.76, where N is equal to the effective number of bits.

$$N = \frac{SINAD - 1.76}{6.02}$$

+/- FULL-SCALE ERROR (GAIN ERROR)

Difference between measured full scale response [(+Fs) - (-Fs)] and the theoretical response (+4 V -2 LSBs) where the +FS (full scale) input voltage is defined as the output transition between 1-10 and 1-11 and the -FS input voltage is defined as the output transition between 0-00 and 0-01.

INPUT BANDWIDTH

Small signal (50 mV) bandwidth (3 dB) of analog input stage.

DIFFERENTIAL NONLINEARITY (DNL)

Error in the width of each code from its theoretical value. (Theoretical = $V_{FS}/2^N$)

INTEGRAL NONLINEARITY (INL)

Linearity error refers to the deviation of each individual code (normalized) from a straight line drawn from -Fs through +Fs. The deviation is measured from the edge of each particular code to the true straight line.

OUTPUT DELAY

Time between the clock's triggering edge and output data valid.

OVERVOLTAGE RECOVERY TIME

The time required for the ADC to recover to full accuracy after an analog input signal 125% of full scale is reduced to 50% of the full-scale value.

SIGNAL-TO-NOISE RATIO (SNR)

The ratio of the fundamental sinusoid power to the total noise power. Harmonics are excluded.

SIGNAL-TO-NOISE AND DISTORTION (SINAD)

The ratio of the fundamental sinusoid power to the total noise and distortion power.

TOTAL HARMONIC DISTORTION (THD)

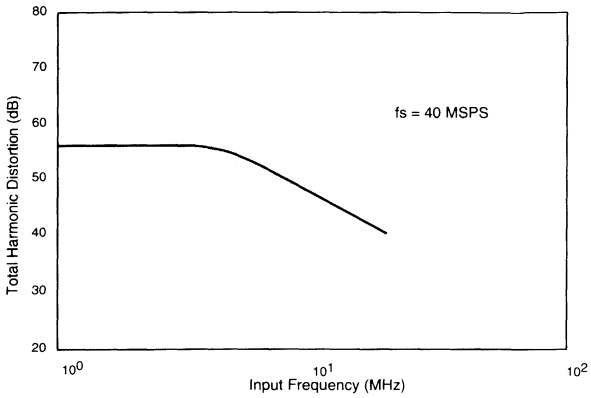
The ratio of the total power of the first 64 harmonics to the power of the measured sinusoidal signal.

SPURIOUS FREE DYNAMIC RANGE (SFDR)

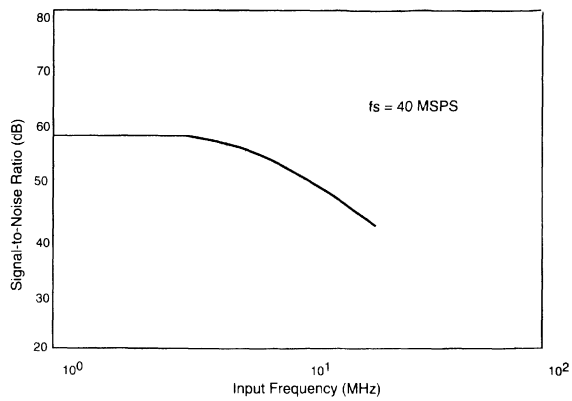
The ratio of the fundamental sinusoidal amplitude to the single largest harmonic or spurious signal.

PERFORMANCE CHARACTERISTICS

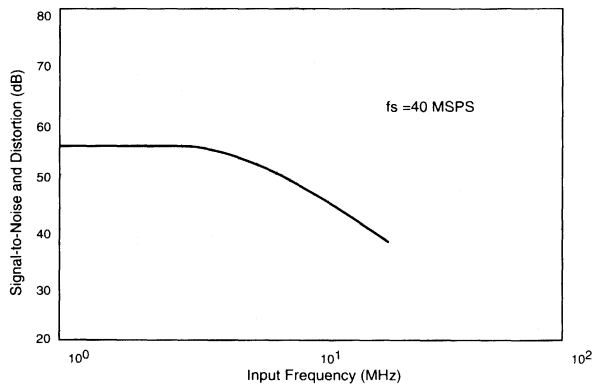
THD vs Input Frequency



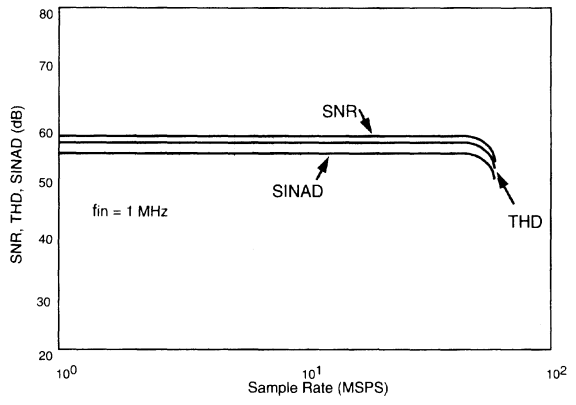
SNR vs Input Frequency



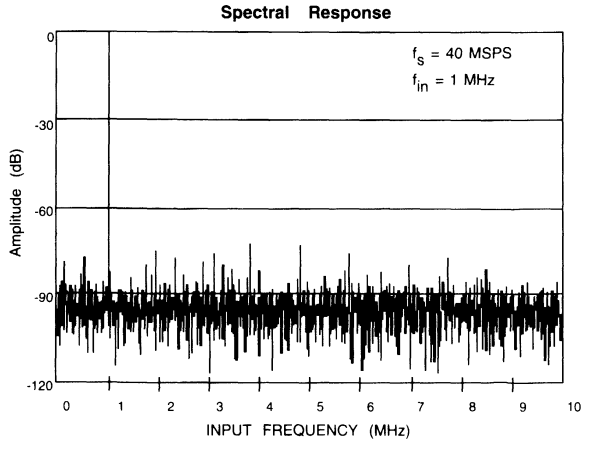
SINAD vs Input Frequency



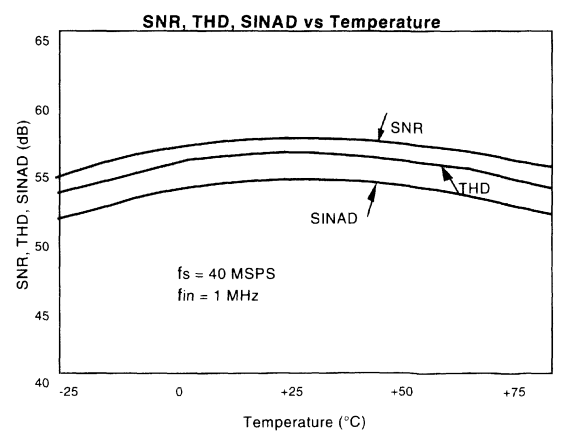
SNR, THD, SINAD vs Sample Rate



Spectral Response



SNR, THD, SINAD vs Temperature



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TYPICAL INTERFACE CIRCUIT

The SPT7824 requires few external components to achieve the stated operation and performance. Figure 2 shows the typical interface requirements when using the SPT7824 in normal circuit operation. The following section provides a description of the pin functions and outlines critical performance criteria to consider for achieving the optimal device performance.

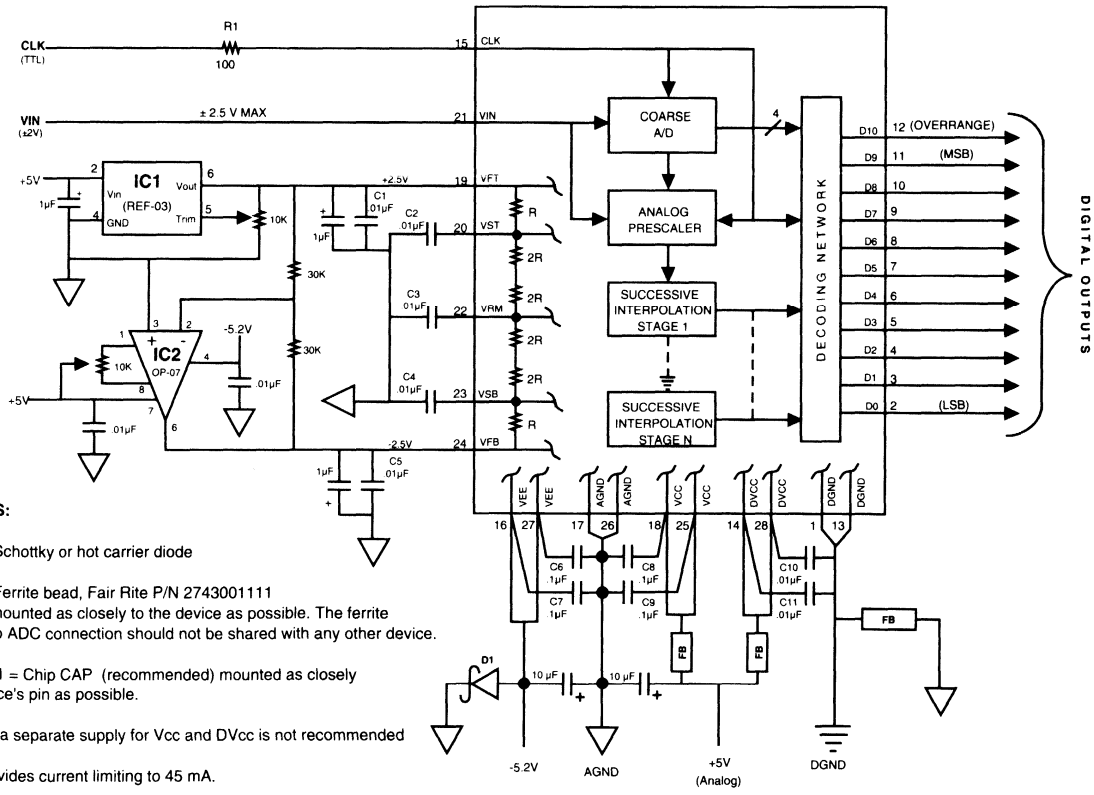
POWER SUPPLIES AND GROUNDING

The SPT7824 requires -5.2 V and +5 V analog supply voltages. The +5 V supply is common to analog VCC and digital DVCC. A ferrite bead in series with each supply line is intended to reduce the transient noise injected into the analog VCC. These beads should be connected as closely as possible to the device. The connection between the beads and the SPT7824 should not be shared with any other device. Each power supply pin should be bypassed as closely as possible to the device. Use 0.1 µF for VEE and VCC, and 0.01 µF for DVCC (chip caps are preferred).

AGND and DGND are the two grounds available on the SPT7824. These two internal grounds are isolated on the device. The use of ground planes is recommended to achieve optimum device performance. DGND is needed for the DVCC return path (40 mA typical) and for the return path for all digital output logic interfaces. AGND and DGND should be separated from each other and connected together only at the device through a ferrite bead.

A Schottky or hot carrier diode connected between AGND and VEE is required. The use of separate power supplies between VCC and DVCC is not recommended due to potential power supply sequencing latch-up conditions. Using the recommended interface circuit shown in figure 2 will provide optimum device performance for the SPT7824.

Figure 2 - Typical Interface Circuit



NOTES:

1) D1 = Schottky or hot carrier diode

2) FB = Ferrite bead, Fair Rite P/N 2743001111
to be mounted as closely to the device as possible. The ferrite bead to ADC connection should not be shared with any other device.

3) C1-C11 = Chip CAP (recommended) mounted as closely to device's pin as possible.

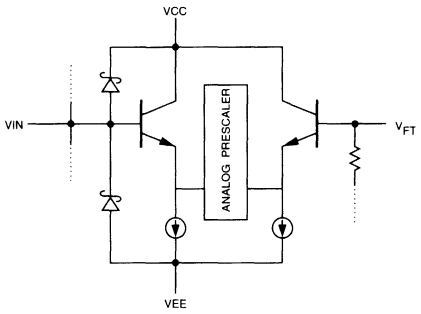
4) Use of a separate supply for Vcc and DVcc is not recommended

5) R1 provides current limiting to 45 mA.

VOLTAGE REFERENCE

The SPT7824 requires the use of two voltage references: V_{FT} and V_{FB}. V_{FT} is the force for the top of the voltage reference ladder (+2.5 V typ), V_{FB} (-2.5 V typ) is the force for the bottom of the voltage reference ladder. Both voltages are applied across an internal reference ladder resistance of 800 ohms. The +2.5 V voltage source for reference VFT must be current limited to 20 mA maximum if a different driving circuit is used in place of the recommended reference circuit shown in figures 2 and 3. In addition, there are three reference ladder taps (V_{ST}, V_{RM} and V_{SB}). V_{ST} is the sense for the top of the reference ladder (+2.0 V), V_{RM} is the midpoint of the ladder (0.0 V typ) and V_{SB} is the sense for the bottom of the reference ladder (-2.0 V). The voltages seen at V_{ST} and V_{SB} are the true full scale input voltages of the device when V_{FT} and V_{FB} are driven to the recommended voltages (+2.5 V and -2.5 V typical respectively). These points should be used to monitor the actual full scale input voltage of the device and should not be driven to the expected ideal values as is commonly done with standard flash converters. When not being used, a decoupling capacitor of .01 uF (chip carrier preferred) connected to AGND from each tap is recommended to minimize high frequency noise injection.

Figure 3 - Analog Equivalent Input Circuit



An example of a reference driver circuit recommended is shown in figure 2. IC1 is REF-03, the +2.5 V reference with a tolerance of 0.6% or +/- 0.015 V. The potentiometer R1 is 10k ohms and supports a minimum adjustable range of up to 150 mV. IC2 is recommended to be an OP-07 or equivalent device. R2 and R3 must be matched to within 0.1% with good TC tracking to maintain a 0.3 LSB matching between V_{FT} and V_{FB}. If 0.1% matching is not met, then potentiometer R4 can be used to adjust the V_{FB} voltage to the desired level. V_{FT} and V_{FB} should be adjusted such that V_{ST} and V_{SB} are exactly +2.0 V and -2.0 V respectively.

The analog input range will scale proportionally with respect to the reference voltage if a different input range is required. The maximum scaling factor for device operation is ± 10% of the recommended reference voltages of V_{FT} and V_{FB}. However, because the device is laser trimmed to optimize performance with ± 2.5 V references, the accuracy of the device will degrade if operated beyond a ± 2% range.

The following errors are defined:
+FS error = top of ladder offset voltage = Δ(+FS -V_{ST}+1 LSB)
-FS error = bottom of ladder offset voltage = Δ(-FS -V_{SB} -1 LSB)
where the +FS (full scale) input voltage is defined as the output transition between 1-10 and 1-11 and the -FS input voltage is defined as the output transition between 0-00 and 0-01.

ANALOG INPUT

V_{IN} is the analog input. The full scale input range will be 80% of the reference voltage or ±2 V with V_{FB}=-2.5 V and V_{FT}=+2.5 V.

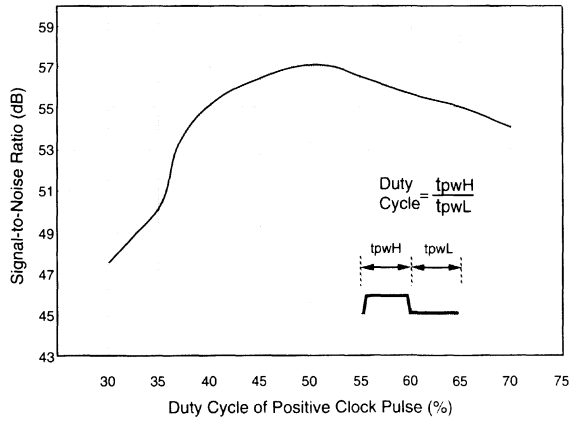
The drive requirements for the analog inputs are minimal when compared to conventional Flash converters due to the SPT7824's extremely low input capacitance of only 5 pF and very high input resistance of 300 kΩ. For example, for an input signal of ± 2 V p-p with an input frequency of 10 MHz, the peak output current required for the driving circuit is only 628 µA.

CLOCK INPUT

The SPT7824 is driven from a single-ended TTL input (CLK). The CLK pulse width (tpwH) must be kept between 10 ns and 300 ns to ensure proper operation of the internal track-and-hold amplifier. (See timing diagram.) When operating the SPT7824 at sampling rates above 3 MSPS, it is recommended that the clock input duty cycle be kept at 50% to optimize performance. (See figure 4.) The analog input signal is latched on the rising edge of the CLK.

The clock input must be driven from fast TTL logic (V_{IH} ≤4.5 V, T_{RISE} <6 ns). In the event the clock is driven from a high current source, use a 100 Ω resistor in series to current limit to approximately 45 mA.

Figure 4 - SNR vs Clock Duty Cycle



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DIGITAL OUTPUTS

The format of the output data (D0-D9) is straight binary. (See table 2.) The outputs are latched on the rising edge of CLK with a propagation delay of 14 ns (typ). There is a one clock cycle latency between CLK and the valid output data. (See timing diagram.)

Table 2 - Output Data Information

ANALOG INPUT	OVERRANGE D1O	OUTPUT CODE D9-DO
>+2.0 V + 1/2 LSB	1	11 1111 1111
+2.0 V -1 LSB	O	11 1111 111Ø
0.0 V	O	ØØ ØØØØ ØØØØ
-2.0 V +1 LSB	O	OO OOOO OOOØ
<2.0 V	O	OO OOOO OOOO

(Ø indicates the flickering bit between logic 0 and 1).

The rise times and fall times of the digital outputs are not symmetrical. The propagation delay of the rise time is typically 14 ns and the fall time is typically 6 ns. (See figure 5.) The nonsymmetrical rise and fall times create approximately 8 ns of invalid data.

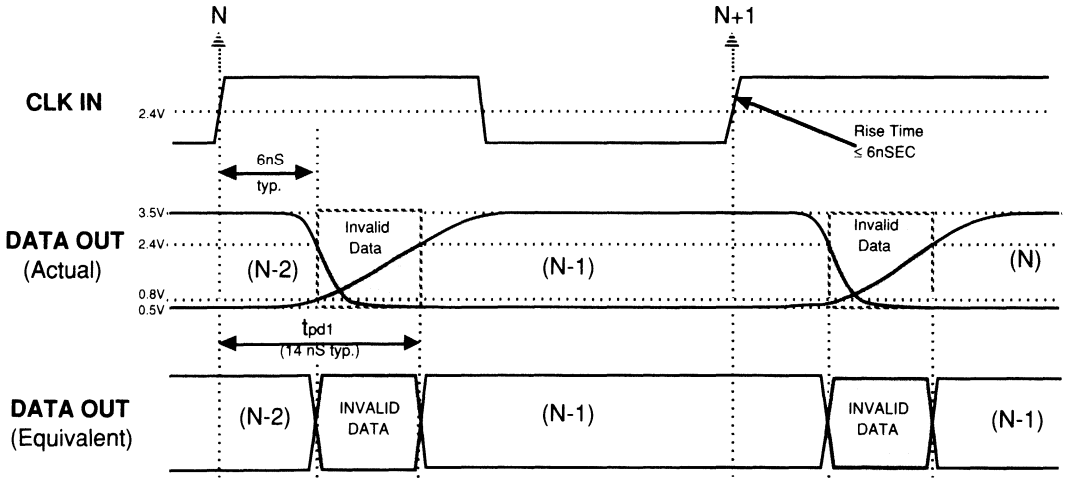
OVERRANGE OUTPUT

The OVERRANGE OUTPUT (D10) is an indication that the analog input signal has exceeded the positive full scale input voltage by 1 LSB. When this condition occurs, D10 will switch to logic 1. All other data outputs (D0 to D9) will remain at logic 1 as long as D10 remains at logic 1. This feature makes it possible to include the SPT7824 into higher resolution systems.

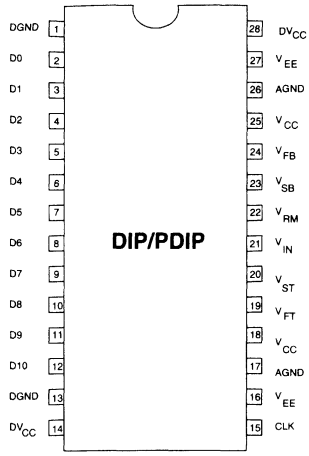
EVALUATION BOARD

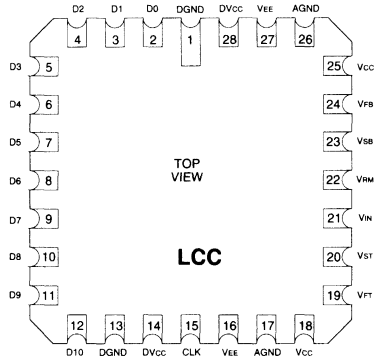
The EB7824 Evaluation Board is available to aid designers in demonstrating the full performance of the SPT7824. This board includes a reference circuit, clock driver circuit, output data latches and an on-board reconstruction of the digital data. An application note describing the operation of this board as well as information on the testing of the SPT7824 is also available. Contact the factory for price and availability.

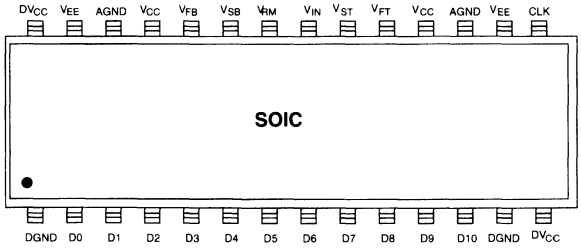
Figure 5 - Digital Output Characteristics



PIN ASSIGNMENT







PIN FUNCTIONS

NAME	FUNCTION
DGND	Digital Ground
D0-D9	TTL Outputs (D0=LSB)
D10	TTL Output Overrange
CLK	Clock
V_{EE}	-5.2 V Supply (Analog)
AGND	Analog Ground
V_{CC}	+5.0 V supply (Analog)
V_{IN}	Analog Input
DV_{CC}	Digital +5.0 V Supply
V_{RM}	Middle of Voltage Reference Ladder
V_{FT}	Force for Top of Reference Ladder
V_{ST}	Sense for Top of Reference Ladder
V_{FB}	Force for Bottom of Reference Ladder
V_{SB}	Sense for Bottom of Reference Ladder

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SIGNAL PROCESSING TECHNOLOGIES

SPT7840

10-BIT, 10 MSPS, 70 mW A/D CONVERTER

PRELIMINARY INFORMATION

3

FEATURES

- Monolithic 10 MSPS Converter
- 70 mW Power Dissipation
- On-Chip Track-and-Hold
- +5 V Power Supply Only
- TTL Outputs
- 5 pF Input Capacitance
- Low Cost
- Tri-State Output Buffers
- High ESD Protection: 6,000 V Minimum

APPLICATIONS

- All High-Speed Applications Where Low Power Dissipation is Required
- Video Imaging
- Medical Imaging
- Radar Receivers
- IR Imaging
- Scanners
- Digital Communications

GENERAL DESCRIPTION

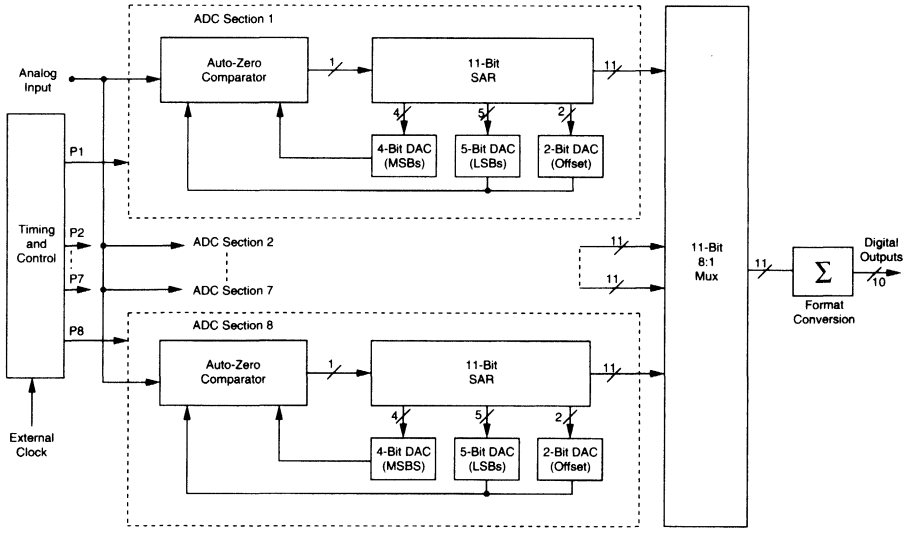
The SPT7840 is a 10-bit monolithic, low cost, ultra-low power analog-to-digital converter capable of word rates of a mimimum of 10 MSPS. The on-chip track-and-hold function assures very good dynamic performance without the need for external components. The input drive requirements are minimized due to the SPT7840's input capacitance of only 5 pF.

Power dissipation is extremely low at only 70 mW typical (100 mW maximum) at 10 MSPS with a power supply of +5.0 V.

The SPT7840 has incorporated proprietary circuit design (*) and double-poly CMOS processing technologies to achieve its advanced performance. Inputs and outputs are TTL-compatible to interface with TTL-logic systems. Output data format is straight binary.

The SPT7840 is available in 28-lead 300 mil cerdip, PDIP, and SOIC packages over the temperature range of 0 to 70 °C. For extended temperature ranges and /883 processing requirements, consult the factory.

BLOCK DIAGRAM



*** Patent pending.**

ABSOLUTE MAXIMUM RATINGS (Beyond which damage may occur)[1] 25 °C

Supply Voltages
- AV_{DD} ..... +6 V
- DV_{DD} ..... +6 V

Input Voltages
- Analog Input ..... -0.5 to 6 V
- V_{REF} ..... 0 to AV_{DD}
- CLK Input ..... V_{DD}

Output
- Digital Outputs ..... TBD mA

Temperature
- Operating Temperature ..... 0 to 70 °C
- Junction Temperature ..... 175 °C
- Lead Temperature, (soldering 10 seconds) ..... 300 °C
- Storage Temperature ..... -65 to +150 °C

Note: 1. Operation at any Absolute Maximum Rating is not implied. See Electrical Specifications for proper nominal applied conditions in typical applications.

ELECTRICAL SPECIFICATIONS

$T_A=T_{MIN}$ to T_{MAX}, AV_{DD} = +5.0 V, DV_{DD}=+5.0 V, V_{REF}=+4.0 V, V_{IN}=+4.0 V(p-p), f_{CLK}=20 MHz, (f_S=10 MSPS) unless otherwise specified.

TEST PARAMETERS	TEST CONDITIONS	LEVEL	MIN	TYP	MAX	UNITS
Resolution			10			Bits
DC Accuracy						
Integral Nonlinearity		I		±1.0		LSB
Differential Nonlinearity		I		±0.5		LSB
No Missing Codes		I		Guaranteed		
Analog Input						
Input Voltage Range		I	0		4.0	V
Input Resistance		I		250		kΩ
Input Capacitance		V		5		pF
Input Bandwidth		V		100		MHz
Offset		II		±2		LSB
Gain Error		II		±2		LSB
Reference Resistance		V		500		Ω
Conversion Characteristics						
Maximum Conversion Rate		I	10			MHz
Pipeline Delay (Latency)		I			12	Clock Cycles
Aperture Delay Time		V		5		ns
Aperture Jitter Time		V		10		ps
Dymamic Performance						
Effective Number of Bits						
f_{IN}=1 MHz		I		8.8		Bits
f_{IN}=3.58 MHz		I		8.5		Bits
Signal-to-Noise Ratio (without Harmonics)						
f_{IN}=1 MHz		I		56		dB
f_{IN}=3.58 MHz		I		53		dB
Harmonic Distortion						
f_{IN}=1 MHz		I		60		dB
f_{IN}=3.58 MHz		I		57		dB
Signal-to-Noise and Distortion (SINAD)						
f_{IN}=1 MHz		I		55		dB
f_{IN}=3.58 MHz		I		53		dB

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ELECTRICAL SPECIFICATIONS

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TEST PARAMETERS	TEST CONDITIONS	LEVEL	MIN	TYP	MAX	UNITS
Spurious Free Dynamic Range		V		62		dB
Differential Phase		V		TBD		Degree
Differential Gain		V		TBD		%
Digital Inputs						
Logic "1" Voltage		I	2.0			V
Logic "0" Voltage		I			0.8	V
Maximum Input Current Low		V	-10		+10	µA
Maximum Input Current High		V	-10		+10	µA
Input Capacitance		V		5		pF
Digital Outputs						
Logic "1" Voltage	(I_{OH}=0.5 mA)	I	2.4			V
Logic "0" Voltage	(I_{OL}=1.6 mA)	I			0.5	V
Power Supply Requirements						
Voltages DV_{DD}		IV	4.5	5.0	5.5	V
AV_{DD}		IV	4.5	5.0	5.5	V
Currents AI_{DD}		IV		8		mA
DI_{DD}		IV		6		mA
Power Dissipation		VI		70	100	mW

TEST LEVEL CODES

All electrical characteristics are subject to the following conditions:

All parameters having min/max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality Assurance inspection. Any blank section in the data column indicates that the specification is not tested at the specified condition.

Unless otherwise noted, all tests are pulsed tests; therefore, $T_J = T_C = T_A$.

TEST LEVEL	TEST PROCEDURE
I	100% production tested at the specified temperature.
II	100% production tested at T_A=25 °C, and sample tested at the specified temperatures.
III	QA sample tested only at the specified temperatures.
IV	Parameter is guaranteed (but not tested) by design and characterization data.
V	Parameter is a typical value for information purposes only.
VI	100% production tested at T_A = 25 °C. Parameter is guaranteed over specified temperature range.

Figure 1A: Timing Diagram 1

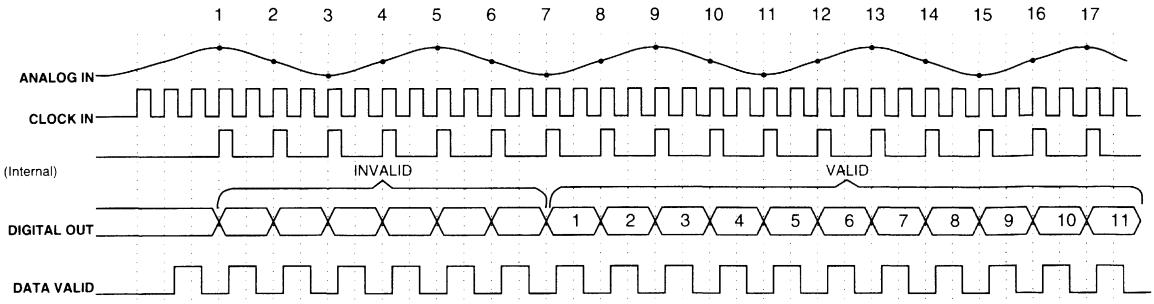

Figure 1A: Timing Diagram 2

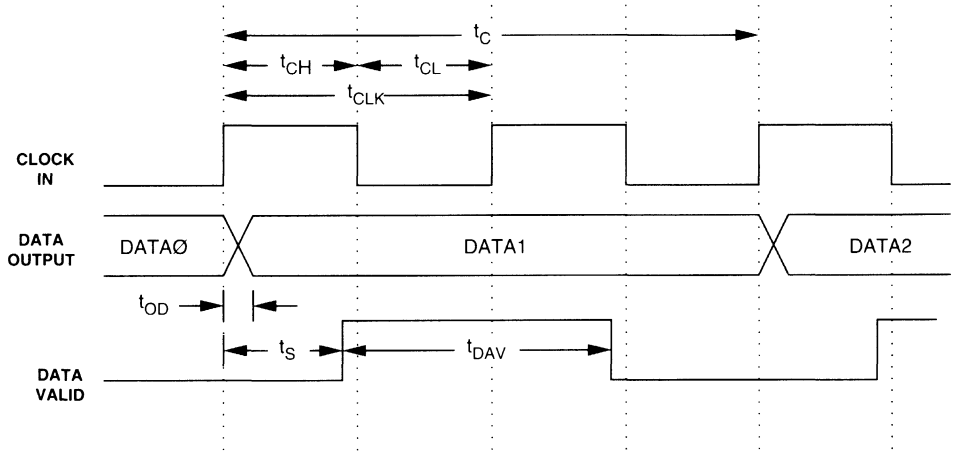

Table 1 - Timing Parameters

DESCRIPTION	PARAMETERS	MIN	TYP	MAX	UNITS
Conversion Time	t_c	$2*t_{CLK}$			ns
Clock Period	t_{CLK}	25			ns
Clock High	t_{CH}	40	50	60	%
Clock Low	t_{CL}	40	50	60	%
Output Delay	t_{OD}		5		ns
DAV Pulse Width	t_{DAV}		t_{CLK}		ns
Clock to Rising Edge of DAV	t_S		12		ns

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SPECIFICATION DEFINITIONS

APERTURE DELAY

Aperture delay represents the point in time, relative to the rising edge of the CLOCK input, that the analog input is sampled.

APERTURE JITTER

The variations in aperture delay for successive samples.

DIFFERENTIAL GAIN (DG)

A signal consisting of a sine wave superimposed on various DC levels is applied to the input. Differential gain is the maximum variation in the sampled sine wave amplitudes at these DC levels.

DIFFERENTIAL PHASE (DP)

A signal consisting of a sine wave superimposed on various DC levels that is applied to the input. Differential phase is the maximum variation in the sampled sine wave phases at these DC levels.

EFFECTIVE NUMBER OF BITS (ENOB)

SINAD = 6.02N + 1.76, where N is equal to the effective number of bits.

$$N = \frac{SINAD - 1.76}{6.02}$$

INPUT BANDWIDTH

Small signal (50 mV) bandwidth (3 dB) of analog input stage.

DIFFERENTIAL NONLINEARITY (DNL)

Error in the width of each code from its theoretical value. (Theoretical = $V_{FS}/2^N$)

INTEGRAL NONLINEARITY (INL)

Linearity error refers to the deviation of each individual code (normalized) from a straight line drawn from -Fs through +Fs. The deviation is measured from the edge of each particular code to the true straight line.

OUTPUT DELAY

Time between the clock's triggering edge and output data valid.

SIGNAL-TO-NOISE RATIO (SNR)

The ratio of the fundamental sinusoid power to the total noise power. Harmonics are excluded.

SIGNAL-TO-NOISE AND DISTORTION (SINAD)

The ratio of the fundamental sinusoid power to the total noise and distortion power.

TOTAL HARMONIC DISTORTION (THD)

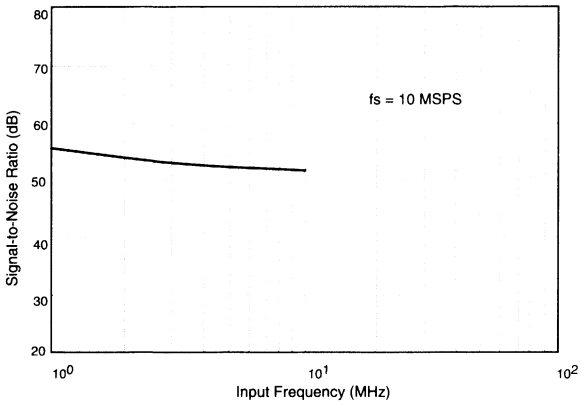
The ratio of the total power of the first 9 harmonics to the power of the measured sinusoidal signal.

SPURIOUS FREE DYNAMIC RANGE (SFDR)

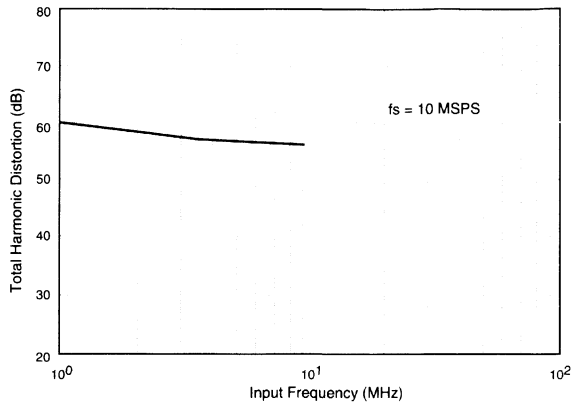
The ratio of the fundamental sinusoidal amplitude to the single largest harmonic or spurious signal.

TYPICAL PERFORMANCE CHARACTERISTICS

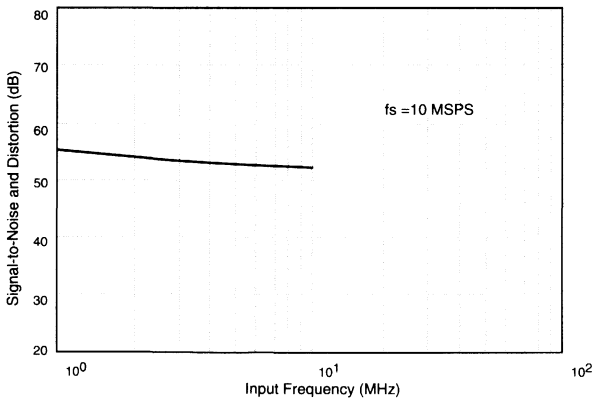
SNR vs Input Frequency



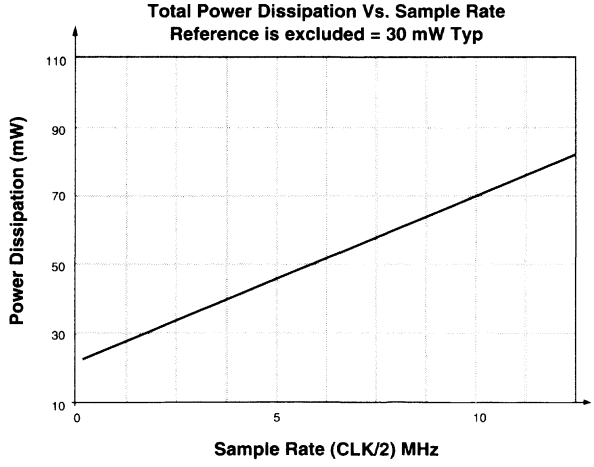
THD vs Input Frequency



SINAD vs Input Frequency



Total Power Dissipation Vs. Sample Rate
Reference is excluded = 30 mW Typ



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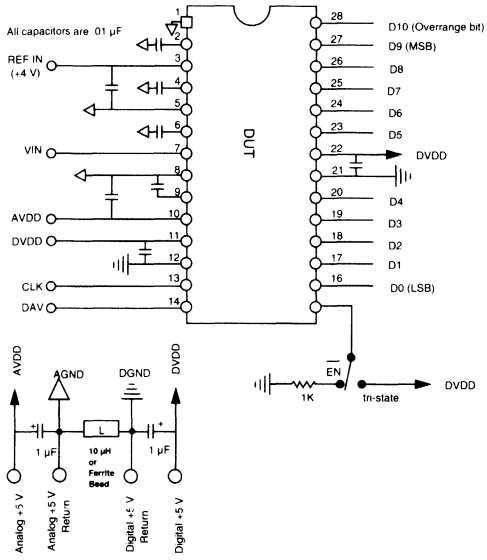
TYPICAL INTERFACE CIRCUIT

Very few external components are required to achieve the stated device performance. Figure 1 shows the typical interface requirements when using the SPT7840 in normal circuit operation. The following sections provide descriptions of the major functions and outline critical performance criteria to consider for achieving the optimal device performance.

Figure 1 - Typical Interface Circuit



POWER SUPPLIES AND GROUNDING

The SPT7840 requires the use of two supply voltages, AV_{DD} and DV_{DD}. AV_{DD} is the analog supply (typically +5.0 V) and DV_{DD} is the digital supply (typically +5.0 V). The analog and digital supplies should be referenced to the analog (AGND) and digital (DGND) grounds, respectively. Each supply should be bypassed as closely as possible to the device with a .01 µF capacitor (chip cap preferred) as shown in figure 1.

OPERATING DESCRIPTION

The general architecture for the CMOS ADC is shown in the block diagram. The design contains eight identical successive approximation ADC sections, all operating in parallel, a 16-phase clock generator, an 11-bit 8:1 digital output multiplexer, correction logic, and a voltage reference generator which provides common reference levels for each ADC section.

The high sample rate is achieved by using multiple SAR ADC sections in parallel, each of which samples the input signal in sequence. Each ADC uses 16 clock cycles to complete a conversion. The clock cycles are allocated as follows:

Clock	Operation
1	Reference zero sampling
2	Auto-zero comparison
3	Auto-calibrate comparison
4	Input sample
5-15	11-bit SAR conversion
16	Data transfer

The 16 phase clock, which is derived from the input clock, synchronizes these events. The timing signals for adjacent ADC sections are shifted by two clock cycles so that the analog input is sampled on every other cycle of the input clock by exactly one ADC section. After 16 clock periods, the timing cycle repeats. The sample rate for the configuration is one-half of the clock rate, e.g., for a 20 MHz clock rate, the input sample rate is 10 MHz. The latency from analog input sample to the corresponding digital output is 12 clock cycles.

- Since only eight comparators are used, a huge power savings is realized.
- The auto-zero operation is done using a closed loop system that uses multiple samples of the comparators response to a reference zero.
- The auto-calibrate operation, which calibrates the gain of the MSB DAC and the LSB ADC, is also done with a closed loop system. Multiple samples of the gain error are integrated to produce a calibration voltage for each ADC section.
- Capacitive displacement currents, which can induce sampling error, are minimized since only one comparator samples the input during a clock cycle.
- The total input capacitance is very low since sections of the converter which are not sampling the signal are isolated from the input by transmission gates.

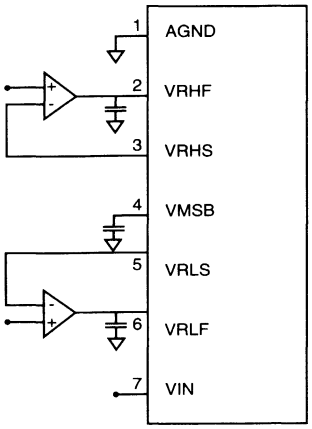
VOLTAGE REFERENCE

The SPT7840 requires the use of a single external voltage reference V_{REF}. The reference value must be within the range of 3 V to 5 V. The reference value determines the full scale input voltage range of the device.

Internal binarily weighted reference voltages are generated from V_{REF} using a resistor ladder. An equivalent circuit for the ladder is shown in figure 3. Force, sense and midpoint taps are provided to ensure force externally accurate offset and gain parameters.

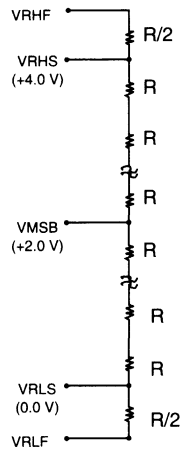
When offset and gain errors of less than ±2 LSB are required, the configuration shown in figure 2 should be used.

Figure 2 - Ladder Force/Sense Circuit



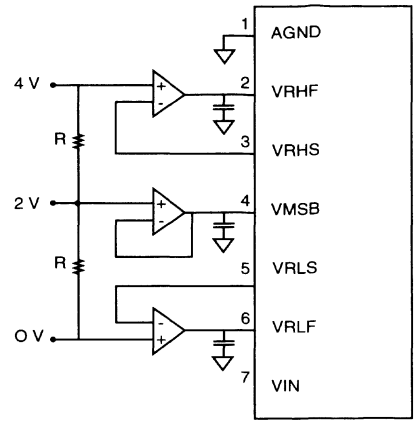
All capacitors are 0.01 µF

Figure 3 - Reference Ladder



R=30 Ω (TYP)

Figure 4 - Force/Sense INL Correction



All capacitors are 0.01 µF

In this configuration:
Offset = VRLS
Gain (Full scale) = VRHS + VRLS

To improve INL performance, the center of the ladder can be driven to $V_{MSB}= \frac{VRHS + VRLS}{2}$. This configuration is shown in figure 4. When not being driven, V_{MSB} should be decoupled to AGND with a .01 µF capacitor to minimize high-frequency noise injection.

If offset and gain errors of greater than ±2 LSB but less than ±10 LSB can be tolerated, simply apply V_{REF} to VRHS and AGND to VRLS as shown in figure 1. Decouple force and sense lines to AGND with a .01 µF capacitor to minimize high-frequency noise injection.

The analog input range will scale proportionally with respect to the reference voltage if a different input range is required. The full scale input voltage range is equal to the value of the voltage reference (i.e., 4 V reference yields a 0 to 4 V input range).

ANALOG INPUT

V_{IN} is the analog input. The input voltage range is from 0 V to AV_{DD} (typically 4.0 V) and will scale proportionally with respect to the voltage reference. (See voltage reference section.)

The drive requirements for the analog inputs are very minimal when compared to most other converters due to the SPT7840's extremely low input capacitance of only 5 pF and very high input resistance of 250k ohms.

CALIBRATION

The SPT7840 uses an auto calibration scheme to ensure 10-bit accuracy over time and temperature. Gain and offset errors are continually adjusted to 10-bit accuracy during device operation. This process is completely transparent to the user. Included in each conversion cycle of the SAR are a gain and an offset calibration cycle.

Upon power-up, the SPT7840 begins its calibration algorithm. In order to achieve the calibration accuracy required, the offset and gain adjustment step size is a fraction of a 10-bit LSB. Since the calibration algorithm is an oversampling process, a minimum of 10k clock cycles are required. This results in a minimum calibration time upon power-up of 250 µsec. Once calibrated, the SPT7840 remains calibrated over time and temperature.

Since the calibration cycles are initiated on the rising edge of the clock, the clock must be continuously applied for the SPT7840 to remain in calibration.

INPUT PROTECTION

All I/O pads are protected with an on-chip protection circuit shown in figure 5. This circuit provides ESD robustness to 6 kV and prevents latch-up under severe discharge conditions without degrading analog transition times.

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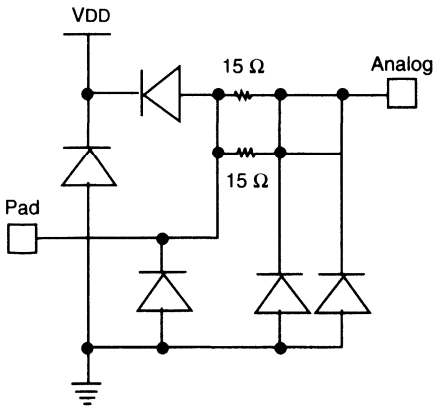
Figure 5 - On-Chip Protection Circuit



POWER SUPPLY SEQUENCING CONSIDERATIONS

All logic inputs should be held low until power to the device has settled to the specific tolerances. Avoid power decoupling networks with large time constants which could delay V_{DD} power to the device.

CLOCK INPUT

The SPT7840 is driven from a single-ended TTL-input clock. Because the pipelined architecture operates on the rising edge of the clock input, the device can operate over a wide range of input clock duty cycles without degrading the dynamic performance. The device's sample rate is 1/2 of the input clock frequency. (See timing diagram.)

DIGITAL OUTPUTS

The format of the output data (D0-D9) is straight binary. (See table 1.) The outputs are latched on the rising edge of CLK. These outputs can be switched into a tri-state mode by bringing $\overline{EN}$ high.

Table 2 - Output Data Information

ANALOG INPUT	OVERRANGE D10	OUTPUT CODE D9-D0
+F.S. + 1/2 LSB	1	11 1111 1111
+F.S. -1/2 LSB	O	11 1111 111Ø
+1/2 F.S.	O	ØØ ØØØØ ØØØØ
+1/2 LSB	O	OO OOOO OOOØ
0.0 V	O	OO OOOO OOOO

(Ø indicates the flickering bit between logic 0 and 1).

OVERRANGE OUTPUT

The OVERRANGE OUTPUT (D10) is an indication that the analog input signal has exceeded the positive full scale input voltage by 1 LSB. When this condition occurs, D10 will switch to logic 1. All other data outputs (D0 to D9) will remain at logic 1 as long as D10 remains at logic 1. This feature makes it possible to include the SPT7840 into higher resolution systems.

EVALUATION BOARD

The EB7850 Evaluation Board will be available to aid designers in demonstrating the full performance of the SPT7840. This board includes a reference circuit, clock driver circuit, output data latches and an on-board reconstruction of the digital data. An application note describing the operation of this board as well as information on the testing of the SPT7840 is also available. Contact the factory for price and availability.

LEADERSHIP IN DATA CONVERSION AND SIGNAL PROCESSING

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SIGNAL PROCESSING TECHNOLOGIES

SPT7850

10-BIT, 20 MSPS, 100 mW A/D CONVERTER

PRELIMINARY INFORMATION

3

FEATURES

- Monolithic 20 MSPS Converter
- 100 mW Power Dissipation
- On-Chip Track-and-Hold
- +5 V Power Supply Only
- TTL Outputs
- 5 pF Input Capacitance
- Low Cost
- Tri-State Output Buffers
- High ESD Protection: 6,000 V Minimum

APPLICATIONS

- All High-Speed Applications Where Low Power Dissipation is Required
- Video Imaging
- Medical Imaging
- Radar Receivers
- IR Imaging
- Scanners
- Digital Communications

GENERAL DESCRIPTION

The SPT7850 is a 10-bit monolithic, low cost, ultra-low power analog-to-digital converter capable of word rates of a mimimum of 20 MSPS. The on-chip track-and-hold function assures very good dynamic performance without the need for external components. The input drive requirements are minimized due to the SPT7850's input capacitance of only 5 pF.

Power dissipation is extremely low at only 100 mW typical (125 mW maximum) at 20 MSPS with a power supply of +5.0 V.

The SPT7850 has incorporated proprietary circuit design (*) and double-poly CMOS processing technologies to achieve its advanced performance. Inputs and outputs are TTL-compatible to interface with TTL-logic systems. Output data format is straight binary.

The SPT7850 is available in 28-lead 300 mil cerdip, PDIP, and SOIC packages over the temperature range of 0 to 70 °C. For extended temperature ranges and /883 processing requirements, consult the factory.

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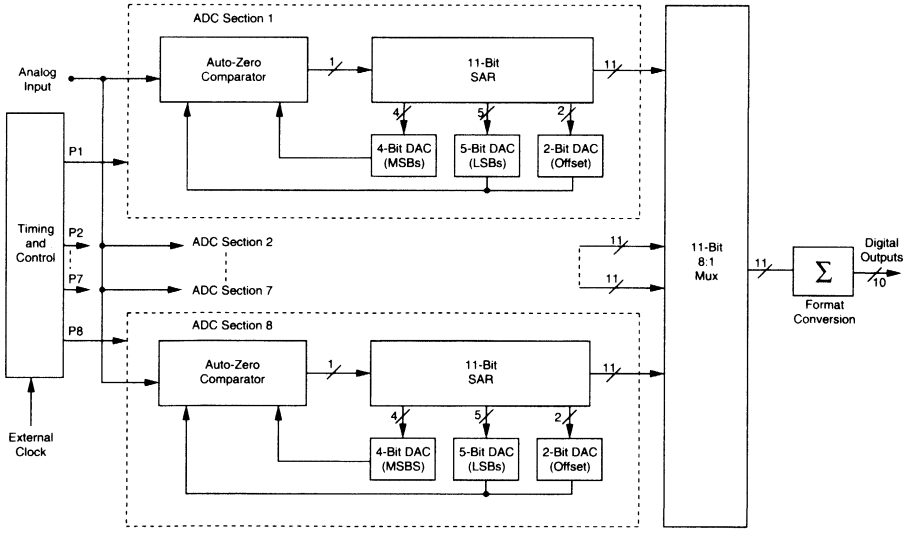

*** Patent pending.**

ABSOLUTE MAXIMUM RATINGS (Beyond which damage may occur)[1] 25 °C

Supply Voltages
- AV_{DD} ..... +6 V
- DV_{DD} ..... +6 V

Input Voltages
- Analog Input ..... -0.5 to 6 V
- V_{REF} ..... 0 to AV_{DD}
- CLK Input ..... V_{DD}

Output
- Digital Outputs ..... TBD mA

Temperature
- Operating Temperature ..... 0 to 70 °C
- Junction Temperature ..... 175 °C
- Lead Temperature, (soldering 10 seconds) ..... 300 °C
- Storage Temperature ..... -65 to +150 °C

Note: 1. Operation at any Absolute Maximum Rating is not implied. See Electrical Specifications for proper nominal applied conditions in typical applications.

ELECTRICAL SPECIFICATIONS

$T_A=T_{MIN}$ to T_{MAX}, AV_{DD} = +5.0 V, DV_{DD}=+5.0 V, V_{REF}=+4.0 V, V_{IN}=+4.0 V(p-p), f_{CLK}=40 MHz, (f_S=20 MSPS) unless otherwise specified.

TEST PARAMETERS	TEST CONDITIONS	LEVEL	MIN	TYP	MAX	UNITS
Resolution			10			Bits
DC Accuracy						
Integral Nonlinearity		I		±1.0		LSB
Differential Nonlinearity		I		±0.5		LSB
No Missing Codes		I		Guaranteed		
Analog Input						
Input Voltage Range		I	0	4.0	4.0	V
Input Resistance		I		250		kΩ
Input Capacitance		V		5		pF
Input Bandwidth		V		100		MHz
Offset		II		±2		LSB
Gain Error		II		±2		LSB
Reference Resistance		V		500		Ω
Conversion Characteristics						
Maximum Conversion Rate		I	20			MHz
Pipeline Delay (Latency)		I			12	Clock Cycles
Aperture Delay Time		V		5		ns
Aperture Jitter Time		V		10		ps
Dymamic Performance						
Effective Number of Bits						
f_{IN}=1 MHz		I		8.8		Bits
f_{IN}=3.58 MHz		I		8.5		Bits
f_{IN}=10.3 MHz		I		8.3		Bits
Signal-to-Noise Ratio (without Harmonics)						
f_{IN}=1 MHz		I		56		dB
f_{IN}=3.58 MHz		I		53		dB
f_{IN}=10.3 MHz		I		52		dB
Harmonic Distortion						
f_{IN}=1 MHz		I		60		dB
f_{IN}=3.58 MHz		I		57		dB
f_{IN}=10.3 MHz		I		56		dB
Signal-to-Noise and Distortion (SINAD)						
f_{IN}=1 MHz		I		55		dB
f_{IN}=3.58 MHz		I		53		dB
f_{IN}=10.3 MHz		I		52		dB

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ELECTRICAL SPECIFICATIONS

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TEST PARAMETERS	TEST CONDITIONS	LEVEL	MIN	TYP	MAX	UNITS
Spurious Free Dynamic Range		V		62		dB
Differential Phase		V		TBD		Degree
Differential Gain		V		TBD		%
Digital Inputs						
Logic "1" Voltage		I	2.0			V
Logic "0" Voltage		I			0.8	V
Maximum Input Current Low		V	-10		+10	µA
Maximum Input Current High		V	-10		+10	µA
Input Capacitance		V		5		pF
Digital Outputs						
Logic "1" Voltage	(I_{OH}=0.5 mA)	I	2.4			V
Logic "0" Voltage	(I_{OS}=1.6 mA)	I			0.5	V
Power Supply Requirements						
Voltages DV_{DD}		IV	4.5	5.0	5.5	V
AV_{DD}		IV	4.5	5.0	5.5	V
Currents AI_{DD}		IV		11		mA
DI_{DD}		IV		8		mA
Power Dissipation		VI		100	125	mW

TEST LEVEL CODES

All electrical characteristics are subject to the following conditions:

All parameters having min/max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality Assurance inspection. Any blank section in the data column indicates that the specification is not tested at the specified condition.

Unless otherwise noted, all tests are pulsed tests; therefore, $T_J = T_C = T_A$.

TEST LEVEL	TEST PROCEDURE
I	100% production tested at the specified temperature.
II	100% production tested at T_A=25 °C, and sample tested at the specified temperatures.
III	QA sample tested only at the specified temperatures.
IV	Parameter is guaranteed (but not tested) by design and characterization data.
V	Parameter is a typical value for information purposes only.
VI	100% production tested at T_A = 25 °C. Parameter is guaranteed over specified temperature range.

Figure 1A: Timing Diagram 1

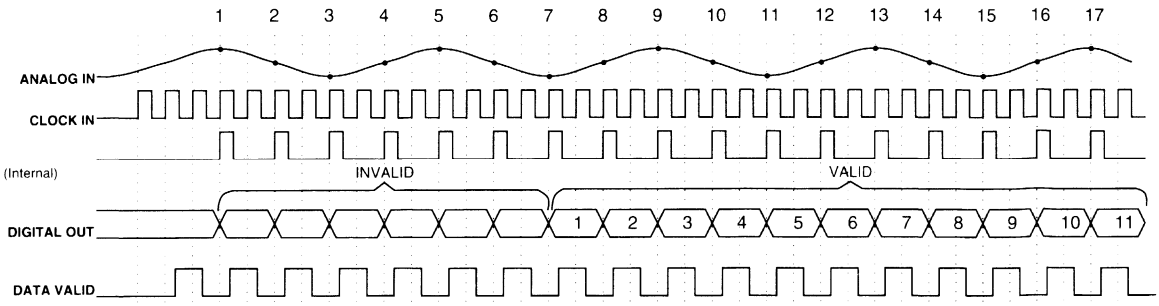

Figure 1A: Timing Diagram 2

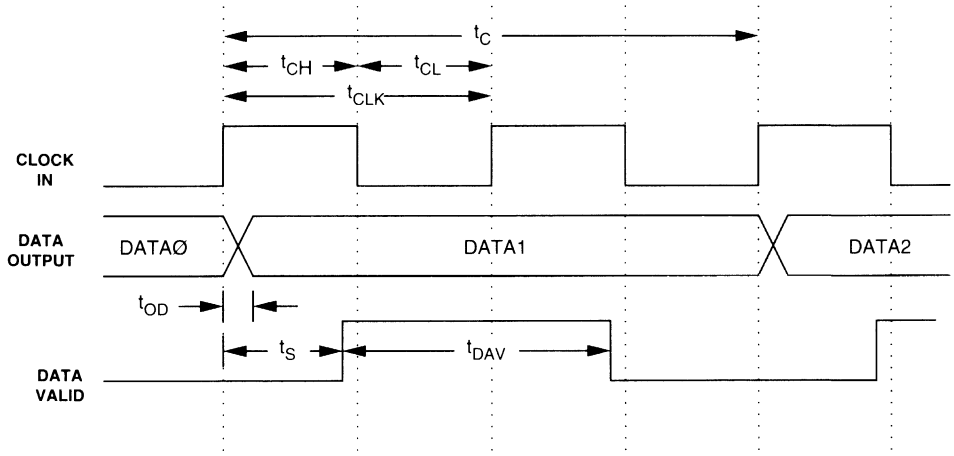

Table 1 - Timing Parameters

DESCRIPTION	PARAMETERS	MIN	TYP	MAX	UNITS
Conversion Time	t_c	$2*t_{CLK}$			ns
Clock Period	t_{CLK}	25			ns
Clock High	t_{CH}	40	50	60	%
Clock Low	t_{CL}	40	50	60	%
Output Delay	t_{OD}		5		ns
DAV Pulse Width	t_{DAV}		t_{CLK}		ns
Clock to Rising Edge of DAV	t_S		12		ns

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SPECIFICATION DEFINITIONS

APERTURE DELAY

Aperture delay represents the point in time, relative to the rising edge of the CLOCK input, that the analog input is sampled.

APERTURE JITTER

The variations in aperture delay for successive samples.

DIFFERENTIAL GAIN (DG)

A signal consisting of a sine wave superimposed on various DC levels is applied to the input. Differential gain is the maximum variation in the sampled sine wave amplitudes at these DC levels.

DIFFERENTIAL PHASE (DP)

A signal consisting of a sine wave superimposed on various DC levels that is applied to the input. Differential phase is the maximum variation in the sampled sine wave phases at these DC levels.

EFFECTIVE NUMBER OF BITS (ENOB)

SINAD = 6.02N + 1.76, where N is equal to the effective number of bits.

$$N = \frac{SINAD - 1.76}{6.02}$$

INPUT BANDWIDTH

Small signal (50 mV) bandwidth (3 dB) of analog input stage.

DIFFERENTIAL NONLINEARITY (DNL)

Error in the width of each code from its theoretical value. (Theoretical = $V_{FS}/2^N$)

INTEGRAL NONLINEARITY (INL)

Linearity error refers to the deviation of each individual code (normalized) from a straight line drawn from -Fs through +Fs. The deviation is measured from the edge of each particular code to the true straight line.

OUTPUT DELAY

Time between the clock's triggering edge and output data valid.

SIGNAL-TO-NOISE RATIO (SNR)

The ratio of the fundamental sinusoid power to the total noise power. Harmonics are excluded.

SIGNAL-TO-NOISE AND DISTORTION (SINAD)

The ratio of the fundamental sinusoid power to the total noise and distortion power.

TOTAL HARMONIC DISTORTION (THD)

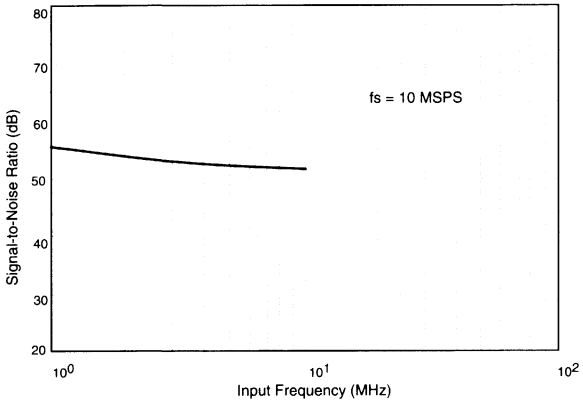
The ratio of the total power of the first 9 harmonics to the power of the measured sinusoidal signal.

SPURIOUS FREE DYNAMIC RANGE (SFDR)

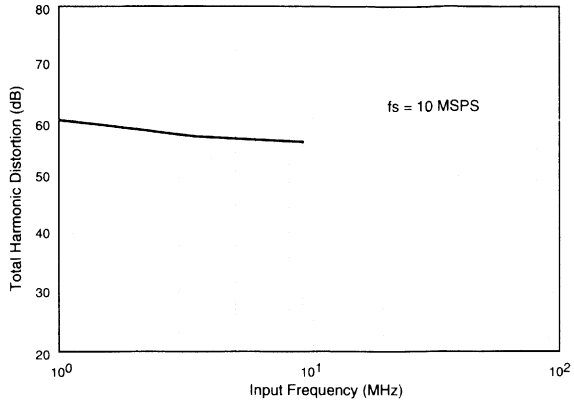
The ratio of the fundamental sinusoidal amplitude to the single largest harmonic or spurious signal.

TYPICAL PERFORMANCE CHARACTERISTICS

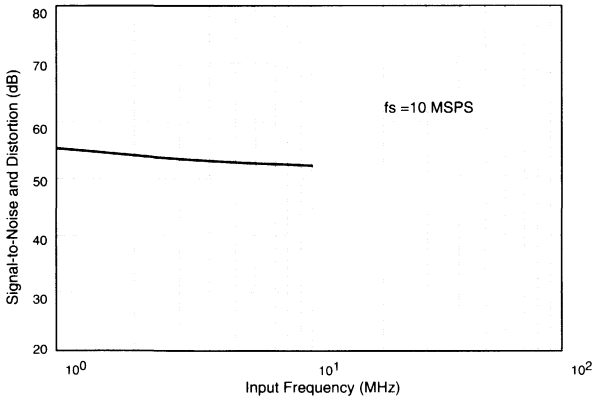
SNR vs Input Frequency



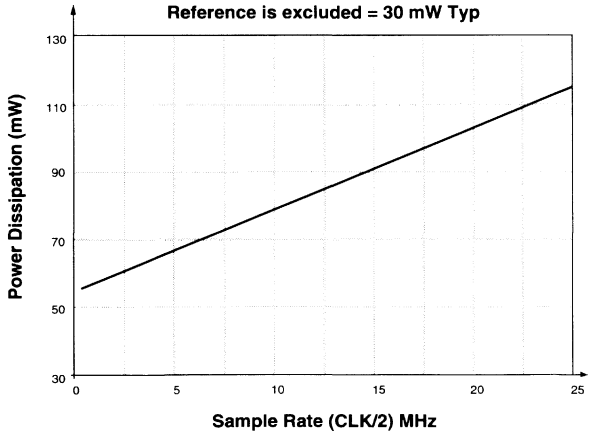
THD vs Input Frequency



SINAD vs Input Frequency



Total Power Dissipation Vs. Sample Rate
Reference is excluded = 30 mW Typ



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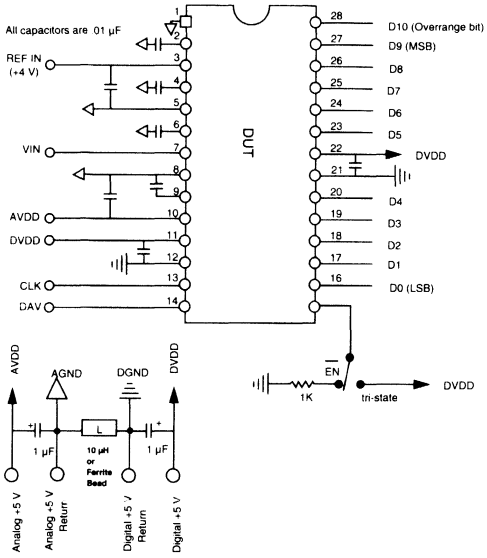
TYPICAL INTERFACE CIRCUIT

Very few external components are required to achieve the stated device performance. Figure 1 shows the typical interface requirements when using the SPT7850 in normal circuit operation. The following sections provide descriptions of the major functions and outline critical performance criteria to consider for achieving the optimal device performance.

Figure 1 - Typical Interface Circuit



POWER SUPPLIES AND GROUNDING

The SPT7850 requires the use of two supply voltages, AV_{DD} and DV_{DD}. AV_{DD} is the analog supply (typically +5.0 V) and DV_{DD} is the digital supply (typically +5.0 V). The analog and digital supplies should be referenced to the analog (AGND) and digital (DGND) grounds, respectively. Each supply should be bypassed as closely as possible to the device with a .01 µF capacitor (chip cap preferred) as shown in figure 1.

OPERATING DESCRIPTION

The general architecture for the CMOS ADC is shown in the block diagram. The design contains eight identical successive approximation ADC sections, all operating in parallel, a 16-phase clock generator, an 11-bit 8:1 digital output multiplexer, correction logic, and a voltage reference generator which provides common reference levels for each ADC section.

The high sample rate is achieved by using multiple SAR ADC sections in parallel, each of which samples the input signal in sequence. Each ADC uses 16 clock cycles to complete a conversion. The clock cycles are allocated as follows:

Clock	Operation
1	Reference zero sampling
2	Auto-zero comparison
3	Auto-calibrate comparison
4	Input sample
5-15	11-bit SAR conversion
16	Data transfer

The 16 phase clock, which is derived from the input clock, synchronizes these events. The timing signals for adjacent ADC sections are shifted by two clock cycles so that the analog input is sampled on every other cycle of the input clock by exactly one ADC section. After 16 clock periods, the timing cycle repeats. The sample rate for the configuration is one-half of the clock rate, e.g., for a 40 MHz clock rate, the input sample rate is 20 MHz. The latency from analog input sample to the corresponding digital output is 12 clock cycles.

- Since only eight comparators are used, a huge power savings is realized.
- The auto-zero operation is done using a closed loop system that uses multiple samples of the comparators response to a reference zero.
- The auto-calibrate operation, which calibrates the gain of the MSB DAC and the LSB ADC, is also done with a closed loop system. Multiple samples of the gain error are integrated to produce a calibration voltage for each ADC section.
- Capacitive displacement currents, which can induce sampling error, are minimized since only one comparator samples the input during a clock cycle.
- The total input capacitance is very low since sections of the converter which are not sampling the signal are isolated from the input by transmission gates.

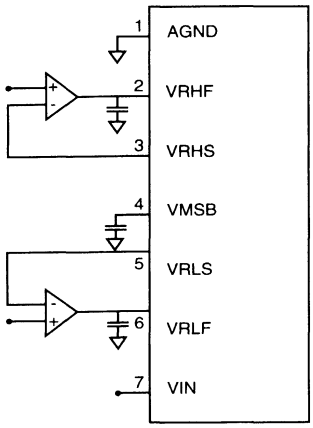
VOLTAGE REFERENCE

The SPT7850 requires the use of a single external voltage reference V_{REF}. The reference value must be within the range of 3 V to 5 V. The reference value determines the full scale input voltage range of the device.

Internal binarily weighted reference voltages are generated from V_{REF} using a resistor ladder. An equivalent circuit for the ladder is shown in figure 3. Force, sense and midpoint taps are provided to ensure force externally accurate offset and gain parameters.

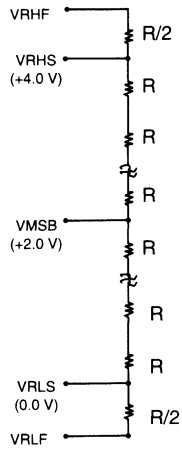
When offset and gain errors of less than ±2 LSB are required, the configuration shown in figure 2 should be used.

Figure 2 - Ladder Force/Sense Circuit



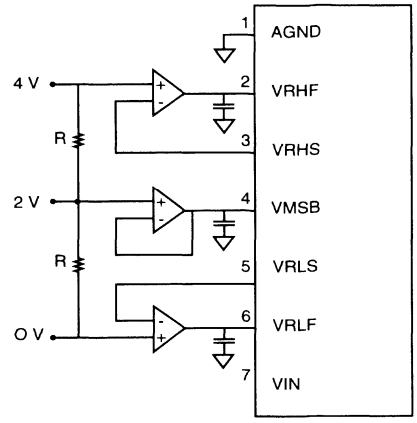
All capacitors are 0.01 µF

Figure 3 - Reference Ladder



R=30 Ω (TYP)

Figure 4 - Force/Sense INL Correction



All capacitors are 0.01 µF

In this configuration:
Offset = VRLS
Gain (Full scale) = VRHS + VRLS

To improve INL performance, the center of the ladder can be driven to $V_{MSB}= \frac{VRHS + VRLS}{2}$. This configuration is shown in figure 4. When not being driven, V_{MSB} should be decoupled to AGND with a .01 µF capacitor to minimize high-frequency noise injection.

If offset and gain errors of greater than ±2 LSB but less than ±10 LSB can be tolerated, simply apply V_{REF} to VRHS and AGND to VRLS as shown in figure 1. Decouple force and sense lines to AGND with a .01 µF capacitor to minimize high-frequency noise injection.

The analog input range will scale proportionally with respect to the reference voltage if a different input range is required. The full scale input voltage range is equal to the value of the voltage reference (i.e., 4 V reference yields a 0 to 4 V input range).

ANALOG INPUT

V_{IN} is the analog input. The input voltage range is from 0 V to AV_{DD} (typically 4.0 V) and will scale proportionally with respect to the voltage reference. (See voltage reference section.)

The drive requirements for the analog inputs are very minimal when compared to most other converters due to the SPT7850's extremely low input capacitance of only 5 pF and very high input resistance of 250k ohms.

CALIBRATION

The SPT7850 uses an auto calibration scheme to ensure 10-bit accuracy over time and temperature. Gain and offset errors are continually adjusted to 10-bit accuracy during device operation. This process is completely transparent to the user. Included in each conversion cycle of the SAR are a gain and an offset calibration cycle.

Upon power-up, the SPT7850 begins its calibration algorithm. In order to achieve the calibration accuracy required, the offset and gain adjustment step size is a fraction of a 10-bit LSB. Since the calibration algorithm is an oversampling process, a minimum of 10k clock cycles are required. This results in a minimum calibration time upon power-up of 250 µsec. Once calibrated, the SPT7850 remains calibrated over time and temperature.

Since the calibration cycles are initiated on the rising edge of the clock, the clock must be continuously applied for the SPT7850 to remain in calibration.

INPUT PROTECTION

All I/O pads are protected with an on-chip protection circuit shown in figure 5. This circuit provides ESD robustness to 6 kV and prevents latch-up under severe discharge conditions without degrading analog transition times.

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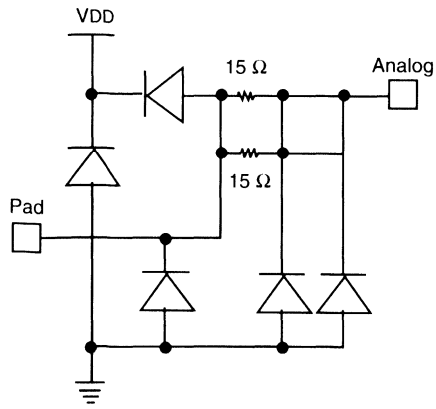
Figure 5 - On-Chip Protection Circuit



POWER SUPPLY SEQUENCING CONSIDERATIONS

All logic inputs should be held low until power to the device has settled to the specific tolerances. Avoid power decoupling networks with large time constants which could delay V_{DD} power to the device.

CLOCK INPUT

The SPT7850 is driven from a single-ended TTL-input clock. Because the pipelined architecture operates on the rising edge of the clock input, the device can operate over a wide range of input clock duty cycles without degrading the dynamic performance. The device's sample rate is 1/2 of the input clock frequency. (See timing diagram.)

DIGITAL OUTPUTS

The format of the output data (D0-D9) is straight binary. (See table 2.) The outputs are latched on the rising edge of CLK. These outputs can be switched into a tri-state mode by bringing $\overline{EN}$ high.

Table 2 - Output Data Information

ANALOG INPUT	OVERRANGE D10	OUTPUT CODE D9-D0
+F.S. + 1/2 LSB	1	11 1111 1111
+F.S. -1/2 LSB	O	11 1111 111Ø
+1/2 F.S.	O	ØØ ØØØØ ØØØØ
+1/2 LSB	O	OO OOOO OOOØ
0.0 V	O	OO OOOO OOOO

(Ø indicates the flickering bit between logic 0 and 1).

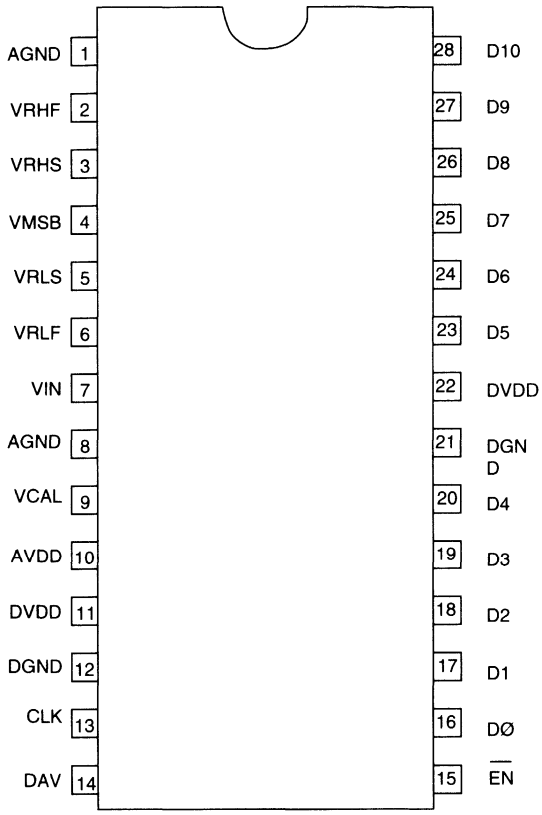
OVERRANGE OUTPUT

The OVERRANGE OUTPUT (D10) is an indication that the analog input signal has exceeded the positive full scale input voltage by 1 LSB. When this condition occurs, D10 will switch to logic 1. All other data outputs (D0 to D9) will remain at logic 1 as long as D10 remains at logic 1. This feature makes it possible to include the SPT7850 into higher resolution systems.

EVALUATION BOARD

The EB7850 Evaluation Board will be available to aid designers in demonstrating the full performance of the SPT7850. This board includes a reference circuit, clock driver circuit, output data latches and an on-board reconstruction of the digital data. An application note describing the operation of this board as well as information on the testing of the SPT7850 is also available. Contact the factory for price and availability.

PIN ASSIGNMENT



PIN FUNCTIONS

NAME	FUNCTION
VRHF	Reference High Force
VRHS	Reference High Sense
VMSB	Ladder Midpoint
VRLS	Reference Low Sense
VRLF	Reference Low Force
VCAL	Calibration Reference
VIN	Analog Input
AGND	Analog Ground
AVDD	Analog V_{DD}
DVDD	Digital V_{DD}
DGND	Digital Ground
CLK	Input Clock f_{CLK} = 2*fs (TTL)
$\overline{EN}$	Output Enable
D0-9	Tri-State Data Output, (DØ=LSB)
D10	Tri-State Output Overrange
DAV	Data Valid

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LEADERSHIP IN DATA CONVERSION AND SIGNAL PROCESSING

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SIGNAL PROCESSING TECHNOLOGIES

SPT7860

10-BIT, 40 MSPS, 200 mW A/D CONVERTER

PRELIMINARY INFORMATION

3

FEATURES

- Monolithic 40 MSPS Converter
- 200 mW Power Dissipation
- On-Chip Track-and-Hold
- +5 V Power Supply Only
- TTL Outputs
- 5 pF Input Capacitance
- Low Cost
- Tri-State Output Buffers
- High ESD Protection: 6,000 V Minimum

APPLICATIONS

- All High-Speed Applications Where Low Power Dissipation is Required
- Video Imaging
- Medical Imaging
- Radar Receivers
- IR Imaging
- Digital Communications

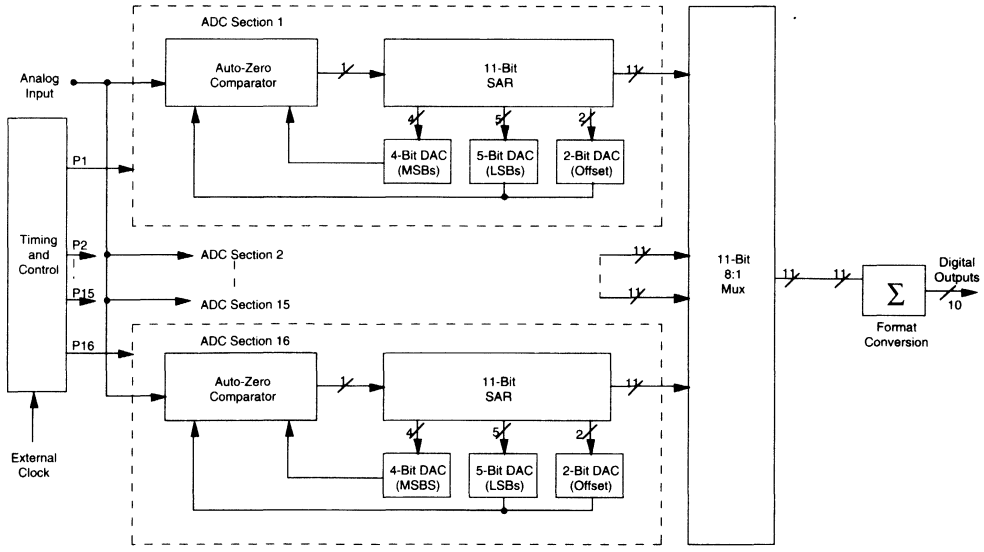
GENERAL DESCRIPTION

The SPT7860 is a 10-bit monolithic, low cost, ultra-low power analog-to-digital converter capable of word rates of a mimimum of 40 MSPS. The on-chip track-and-hold function assures very good dynamic performance without the need for external components. The input drive requirements are minimized due to the SPT7860's input capacitance of only 5 pF.

Power dissipation is extremely low at only 200 mW typical at 40 MSPS with a power supply of +5.0 V. The SPT7860 has incorporated proprietary circuit design (*) and double-poly CMOS processing technologies to achieve its advanced performance. Inputs and outputs are TTL-compatible to interface with TTL-logic systems. Output data format is straight binary.

The SPT7860 is available in 28-lead 300 mil, cerdip, PDIP and SOIC packages over the temperature range of 0 to 70 °C. For extended temperature ranges and /883 processing requirements, consult the factory.

BLOCK DIAGRAM



*PATENT PENDING

ABSOLUTE MAXIMUM RATINGS (Beyond which damage may occur)[1] 25 °C

Supply Voltages
- AV_{DD} ..... +6 V
- DV_{DD} ..... +6 V

Input Voltages
- Analog Input ..... -0.5 to 6 V
- V_{REF} ..... 0 to AV_{DD}
- CLK Input ..... V_{DD}

Output
- Digital Outputs ..... TBD mA

Temperature
- Operating Temperature ..... 0 to 70 °C
- Junction Temperature ..... 175 °C
- Lead Temperature, (soldering 10 seconds) ..... 300 °C
- Storage Temperature ..... -65 to +150 °C

Note: 1. Operation at any Absolute Maximum Rating is not implied. See Electrical Specifications for proper nominal applied conditions in typical applications.

ELECTRICAL SPECIFICATIONS

$T_A=T_{MIN}$ to T_{MAX}, AV_{DD} = +5.0 V, DV_{DD} = +5.0 V, V_{IN} = 0 to 4 V(p-p), f_{CLK} = 40 MHz, f_S = 40 MSPS, Vref= 4.0 V

TEST PARAMETERS	TEST CONDITIONS	LEVEL	MIN	TYP	MAX	UNITS
Resolution			10			Bits
DC Accuracy						
Integral Nonlinearity		I		±1.0		LSB
Differential Nonlinearity		I		±0.5		LSB
No Missing Codes		I		Guaranteed		
Analog Input						
Input Voltage Range		I	0		4.0	V
Input Resistance		I		250		kΩ
Input Capacitance		V		5		pF
Input Bandwidth		V	250			MHz
Offset		II			±2	LSB
Gain Error		II			±2	LSB
Reference Resistance		V	400	500	600	Ω
Reference Bandwidth		V	100	150		MHz
Conversion Characteristics						
Maximum Conversion Rate		I	40			MHz
Pipeline Delay (Latency)		I			12	Clock Cycles
Aperture Delay Time		V		8		ns
Aperture Jitter Time		V			15	ps(p-p)
Dymamic Performance						
Effective Number of Bits						
fin=1 MHz		I		8.8		Bits
fin=3.58 MHz		I		8.5		Bits
fin=10.3 MHz		I		8.3		Bits
Signal-to-Noise Ratio (without Harmonics)						
fin=1 MHz		I		56		dB
fin=3.58 MHz		I		53		dB
fin=10.3 MHz		I		52		dB
Harmonic Distortion	(9 Distortion bins from					
f_{IN}=1 MHz	4096 pt FFT)	I		60		dB
f_{IN}=3.58 MHz		I		57		dB
f_{IN}=10.3 MHz		I		56		dB
Signal-to-Noise and Distortion (SINAD)						
fin=1 MHz		I		55		dB
fin=3.58 MHz		I		53		dB
fin=10.3 MHz		I		52		dB

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SPT

ELECTRICAL SPECIFICATIONS

$T_A=T_{MIN}$ to T_{MAX}, AV_{DD} = +5.0 V, DV_{DD} = +5.0 V, V_{IN} = 0 to 4 V(p-p), f_{CLK} = 40 MHz, f_S = 40 MSPS, Vref= 4.0 V

TEST PARAMETERS	TEST CONDITIONS	LEVEL	MIN	TYP	MAX	UNITS
Spurious Free Dynamic Range		V		70		dB
Differential Phase		V		TBD		Degree
Differential Gain				TBD		%Digital
Intermodulation Distortion	f_A=1.0 MHz f_B=1.05 MHz			TBD		dB
Inputs						
Logic "1" Voltage		I	2.0			V
Logic "0" Voltage		I			0.8	V
Maximum Input Current Low		V	-10		+10	µA
Maximum Input Current High		V	-10		+10	µA
Input Capacitance		V		+5		pF
Digital Outputs						
Logic "1" Voltage	I_{OH} = 0.5 mA	I	2.4			V
Logic "0" Voltage	I_{OL} = 1.6 mA	I			0.4	V
Power Supply Requirements						
Voltages	DV_{DD}	IV	4.5	5.0	5.5	V
	AV_{DD}	IV	4.5	5.0	5.5	V
Currents	AI_{DD}	IV		11		mA
	DI_{DD}	IV		8		mA
Power Dissipation		VI		200	250	mW

TEST LEVEL CODES

All electrical characteristics are subject to the following conditions:

All parameters having min/max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality Assurance inspection. Any blank section in the data column indicates that the specification is not tested at the specified condition.

Unless otherwise noted, all tests are pulsed tests; therefore, $T_J = T_C = T_A$.

TEST LEVEL	TEST PROCEDURE
I	100% production tested at the specified temperature.
II	100% production tested at T_A=25 °C, and sample tested at the specified temperatures.
III	QA sample tested only at the specified temperatures.
IV	Parameter is guaranteed (but not tested) by design and characterization data.
V	Parameter is a typical value for information purposes only.
VI	100% production tested at T_A = 25 °C. Parameter is guaranteed over specified temperature range.

Figure 1A: Timing Diagram 1

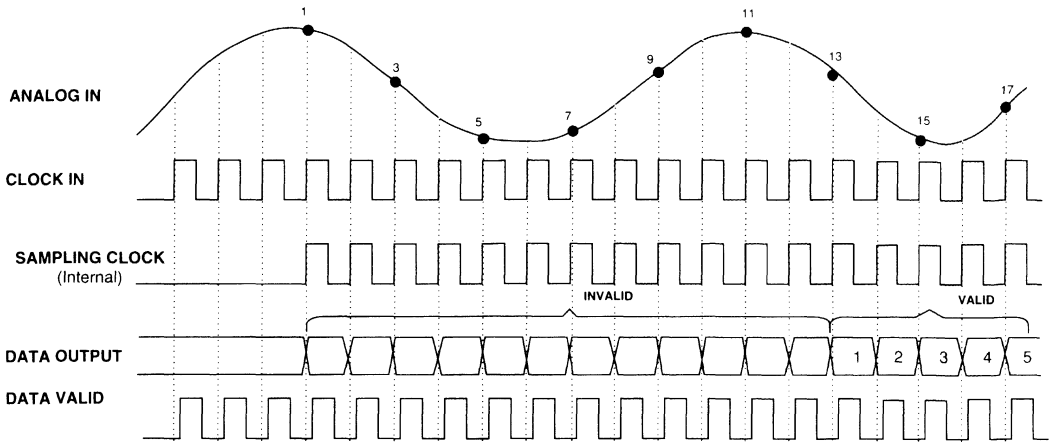

Figure 1B: Timing Diagram 2

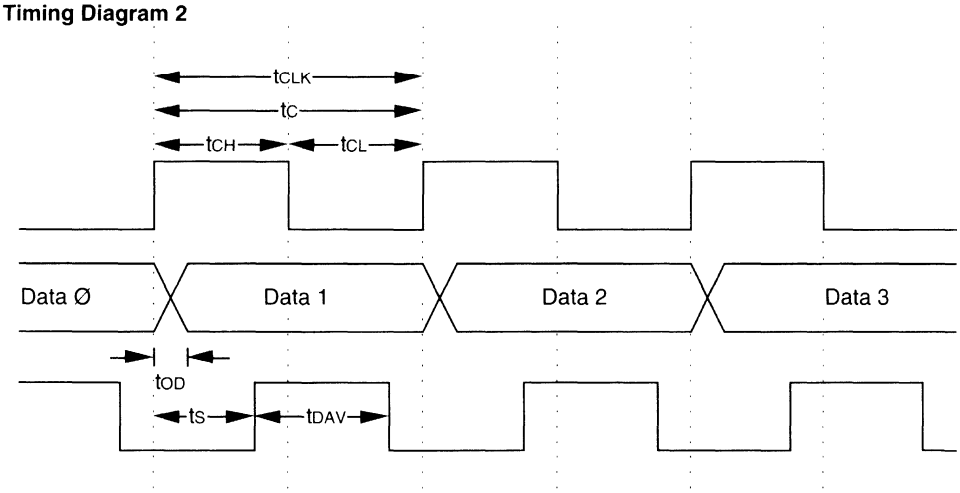

Table 1 - Timing Parameters

DESCRIPTION	PARAMETERS	MIN	TYP	MAX	UNITS
Conversion Time	t_c	t_{CLK}			ns
Clock Period	t_{CLK}	25			ns
Clock High	t_{CH}	40	50	60	%
Clock Low	t_{CL}	40	50	60	%
Output Delay	t_{OD}		5		ns
DAV Pulse Width	t_{DAV}		t_{CLK}		ns
Clock to Rising Edge of DAV	t_S		10		ns

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SPECIFICATION DEFINITIONS

APERTURE DELAY

Aperture delay represents the point in time, relative to the rising edge of the CLOCK input, that the analog input is sampled.

APERTURE JITTER

The variations in aperture delay for successive samples.

DIFFERENTIAL GAIN (DG)

A signal consisting of a sine wave superimposed on various DC levels is applied to the input. Differential gain is the maximum variation in the sampled sine wave amplitudes at these DC levels.

DIFFERENTIAL PHASE (DP)

A signal consisting of a sine wave superimposed on various DC levels that is applied to the input. Differential phase is the maximum variation in the sampled sine wave phases at these DC levels.

EFFECTIVE NUMBER OF BITS (ENOB)

SINAD = 6.02N + 1.76, where N is equal to the effective number of bits.

$$N = \frac{SINAD - 1.76}{6.02}$$

INPUT BANDWIDTH

Small signal (50 mV) bandwidth (3 dB) of analog input stage.

DIFFERENTIAL NONLINEARITY (DNL)

Error in the width of each code from its theoretical value. (Theoretical = $V_{FS}/2^N$)

INTEGRAL NONLINEARITY (INL)

Linearity error refers to the deviation of each individual code (normalized) from a straight line drawn from -Fs through +Fs. The deviation is measured from the edge of each particular code to the true straight line.

OUTPUT DELAY

Time between the clock's triggering edge and output data valid.

OVERVOLTAGE RECOVERY TIME

The time required for the ADC to recover to full accuracy after an analog input signal 125% of full scale is reduced to 50% of the full-scale value.

SIGNAL-TO-NOISE RATIO (SNR)

The ratio of the fundamental sinusoid power to the total noise power. Harmonics are excluded.

SIGNAL-TO-NOISE AND DISTORTION (SINAD)

The ratio of the fundamental sinusoid power to the total noise and distortion power.

TOTAL HARMONIC DISTORTION (THD)

The ratio of the total power of the first 9 harmonics to the power of the measured sinusoidal signal.

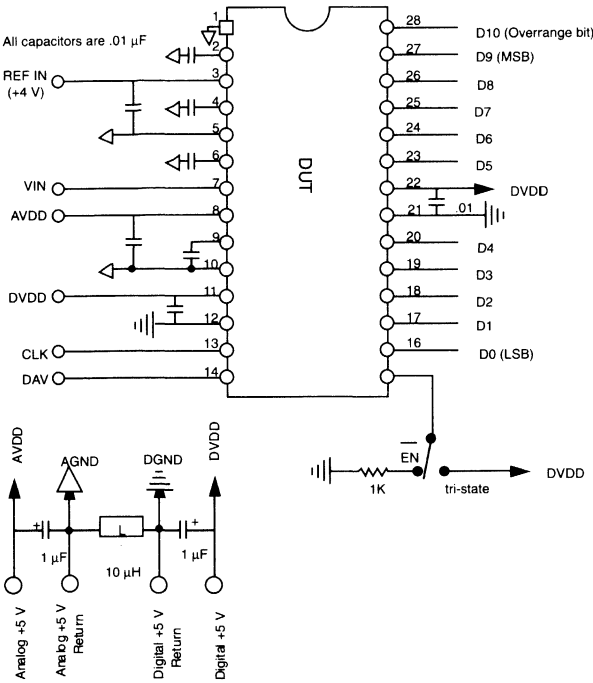
SPURIOUS FREE DYNAMIC RANGE (SFDR)

The ratio of the fundamental sinusoidal amplitude to the single largest harmonic or spurious signal.

TYPICAL INTERFACE CIRCUIT

Very few external components are required to achieve the stated device performance. Figure 1 shows the typical interface requirements when using the SPT7860 in normal circuit operation. The following sections provide descriptions of the major functions and outline critical performance criteria to consider for achieving the optimal device performance.

Figure 1 - Typical Interface Circuit



POWER SUPPLIES AND GROUNDING

The SPT7860 requires the use of two supply voltages, AV_{DD} and DV_{DD}. AV_{DD} is the analog supply (typically +5.0 V) and DV_{DD} is the digital supply (typically +5.0 V). The analog and digital supplies should be referenced to the analog (AGND) and digital (DGND) grounds, respectively. Each supply should be bypassed as closely as possible to the device with a .01 µF capacitor (chip cap preferred) as shown in figure 1.

OPERATING DESCRIPTION

The general architecture for the CMOS ADC is shown in the block diagram. The design contains 16 identical successive approximation ADC sections, all operating in parallel, a 16-phase clock generator, an 11-bit 16:1 digital output multiplexer, correction logic, and a voltage reference generator which provides common reference levels for each ADC section.

The high sample rate is achieved by using multiple SAR ADC sections in parallel, each of which samples the input signal in sequence. Each ADC uses 16 clock cycles to complete a conversion. The clock cycles are allocated as follows:

Clock	Operation
1	Reference zero sampling
2	Auto-zero comparison
3	Auto-calibrate comparison
4	Input sample
5-15	10-bit SAR conversion
16	Data transfer

The 16 phase clock, which is derived from the input clock, synchronizes these events. The timing signals for adjacent ADC sections are shifted by one clock cycle so that the analog input is sampled on every cycle of the input clock by exactly one ADC section. After 16 clock periods, the timing cycle repeats. The latency from analog input sample to the corresponding digital output is 12 clock cycles.

- Since only 16 comparators are used, a huge power savings is realized.
- The auto-zero operation is done using a closed loop system that uses multiple samples of the comparators response to a reference zero.
- The auto-calibrate operation, which calibrates the gain of the MSB DAC and the LSB ADC, is also done with a closed loop system. Multiple samples of the gain error are integrated to produce a calibration voltage for each ADC section.
- Capacitive displacement currents, which can induce sampling error, are minimized since only one comparator samples the input during a clock cycle.
- The total input capacitance is very low since sections of the converter which are not sampling the signal are isolated from the input by transmission gates.

VOLTAGE REFERENCE

The SPT7860 requires the use of a single external voltage reference V_{REF}. The reference value must be within the range of 3 V to 5 V. The reference value determines the full scale input voltage range of the device.

Internal binarily weighted reference voltages are generated from V_{REF} using a resistor ladder. An equivalent circuit for the ladder is shown in figure 3. Force, sense and midpoint taps are provided to ensure force externally accurate offset and gain parameters.

When offset and gain errors of less than ±2 LSB are required, the configuration shown in figure 2 should be used.
In this configuration:

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Figure 2 - Ladder Force/Sense Circuit

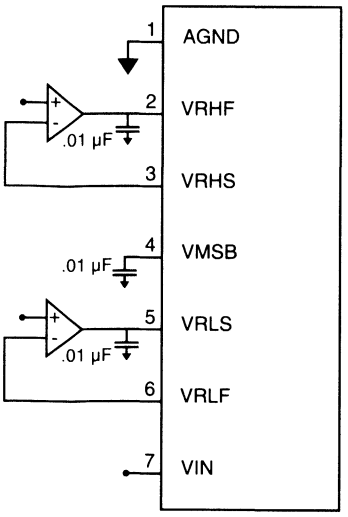


Figure 3 - Reference Ladder

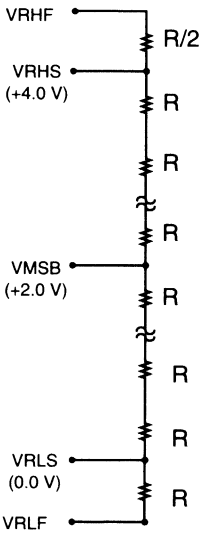
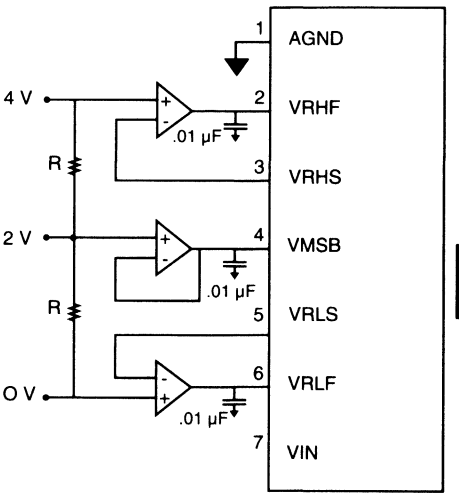


Figure 4 - Force/Sense INL Correction



Offset = VRLS
Gain (Full scale) = VRHS + VRLS

To improve INL performance, the center of the ladder can be driven to $\frac{VRHS + VRLS}{2}$. This configuration is shown in figure 4. When not being driven, MSB should be decoupled to AGND with a .01 µF capacitor to minimize high-frequency noise injection.

If offset and gain errors of greater than ±2 LSB but less than ±10 LSB can be tolerated, simply apply V_{REF} to VRHS and AGND to VRLS. Decouple force and sense lines to AGND with a .01 µF capacitor to minimize high-frequency noise injection.

The analog input range will scale proportionally with respect to the reference voltage if a different input range is required. The full scale input voltage range is equal to the value of the voltage reference (i.e., 4 V reference yields a 0 to 4 V input range).

ANALOG INPUT

V_{IN} is the analog input. The input voltage range is from 0 V to AV_{DD} (typically 4.0 V) and will scale proportionally with respect to the voltage reference. (See voltage reference section.)

The drive requirements for the analog inputs are very minimal when compared to most other converters due to the SPT7860's extremely low input capacitance of only 5 pF and very high input resistance of 250k ohms.

CALIBRATION

The SPT7860 uses an auto calibration scheme to ensure 10-bit accuracy over time and temperature. Gain and offset errors are continually adjusted to 10-bit accuracy during device operation. This process is completely transparent to the user. Included in each conversion cycle of the SAR are a gain and an offset calibration cycle.

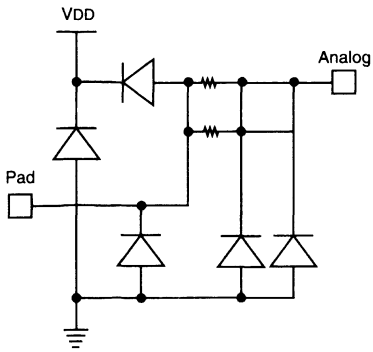
Upon power-up, the SPT7860 begins its calibration algorithm. In order to achieve the calibration accuracy required, the offset and gain adjustment step size is a fraction of a 10-bit LSB. Since the calibration algorithm is an oversampling process, a minimum of 10,000 clock cycles are required. This results in a minimum calibration time upon power-up of 250 µsec. Once calibrated, the SPT7860 remains calibrated over time and temperature.

Since the calibration cycles are initiated on the rising edge of the clock, the clock must be continuously applied for the SPT7860 to remain in calibration.

INPUT PROTECTION

All I/O pads are protected with an on-chip protection circuit shown in figure 5. This circuit provides ESD robustness to 6 kV and prevents latch-up under severe discharge conditions without degrading analog transition times.

Figure 5 - On-Chip Protection Circuit



POWER SUPPLY SEQUENCING CONSIDERATIONS

All logic inputs should be held low until power to the device has settled to the specific tolerances. Avoid power decoupling networks with large time constants which could delay V_{DD} power to the device.

CLOCK INPUT

The SPT7860 is driven from a single-ended TTL-input clock. Because the pipelined architecture operates on the rising edge of the clock input, the device can operate over a wide range of input clock duty cycles without degrading the dynamic performance.

DIGITAL OUTPUTS

The format of the output data (D0-D9) is straight binary. (See table 1.) The outputs are latched on the rising edge of CLK. These outputs can be switched into a tri-state mode by bringing $\overline{EN}$ high.

Table 2 - Output Data Information

ANALOG INPUT	OVERRANGE D10	OUTPUT CODE D9-D0
+F.S. + 1/2 LSB	1	11 1111 1111
+F.S. -1/2 LSB	O	11 1111 111Ø
+1/2 F.S.	O	ØØ ØØØØ ØØØØ
+1/2 LSB	O	OO OOOO OOOØ
0.0 V	O	OO OOOO OOOO

(Ø indicates the flickering bit between logic 0 and 1).

OVERRANGE OUTPUT

The OVERRANGE OUTPUT (D10) is an indication that the analog input signal has exceeded the positive full scale input voltage by 1 LSB. When this condition occurs, D10 will switch to logic 1. All other data outputs (D0 to D9) will remain at logic 1 as long as D10 remains at logic 1. This feature makes it possible to include the SPT7860 into higher resolution systems.

EVALUATION BOARD

The EB7860 evaluation board will be available to aid designers in demonstrating the full performance of the SPT7860. This board includes a reference circuit, clock driver circuit, output data latches and an on-board reconstruction of the digital data. An application note describing the operation of this board as well as information on the testing of the SPT7860 is also available. Contact the factory for price and availability.

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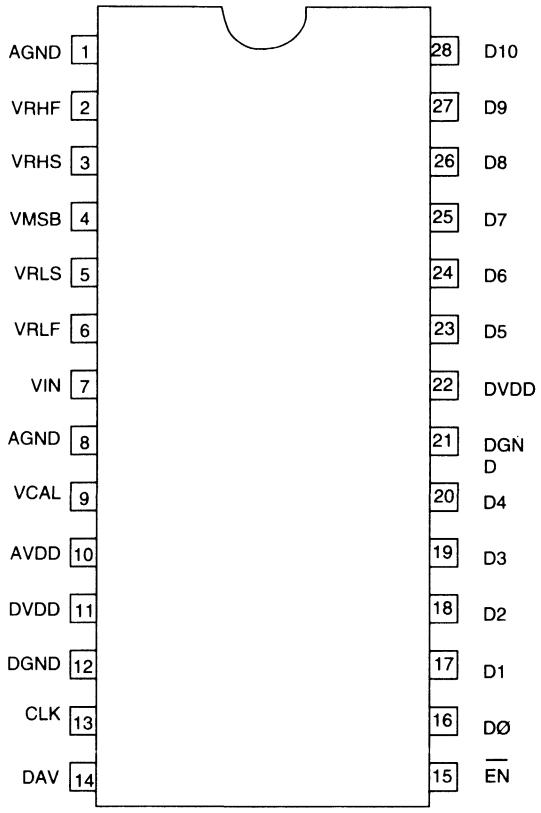
PIN ASSIGNMENT



PIN FUNCTIONS

NAME	FUNCTION
AGND1	Analog Ground
VREF	Input Reference
VRHF	Reference High Force
VRHS	Reference High Sense
VMSB	Ladder Midpoint
VRLS	Reference Low Sense
VRLF	Reference Low Force
VCAL	Calibration Reference
VIN	Analog Input
AGND	Analog Ground
AVDD	Analog V_{DD}
DVDD	Digital V_{DD}
DGND	Digital Ground
CLK	Input Clock f_{CLK} =fs (TTL)
$\overline{EN}$	Output Enable
D0-9	Tri-State Data Output, (DØ=LSB)
D10	Tri-State Output Overrange
ODVDD	+5 V for Output Drivers
ODGND	Ground for Output Drivers
DAV	Data Valid
AGND2	Analog Ground

LEADERSHIP IN DATA CONVERSION AND SIGNAL PROCESSING

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SIGNAL PROCESSING TECHNOLOGIES

SPT7910

12-BIT, 10 MSPS, ECL, A/D CONVERTER

FEATURES

- Monolithic
- 12-Bit 10 MSPS Converter
- 67 dB SNR @ 500 kHz Input
- On-Chip Track/Hold
- Bipolar ±2.0 V Analog Input
- Low Power (1.4 W Typical)
- 5 pF input Capacitance
- ECL Outputs

APPLICATIONS

- Radar Receivers
- Professional Video
- Instrumentation
- Medical Imaging
- Electronic Warfare
- Digital Communications
- Digital Spectrum Analyzers
- Electro-optics

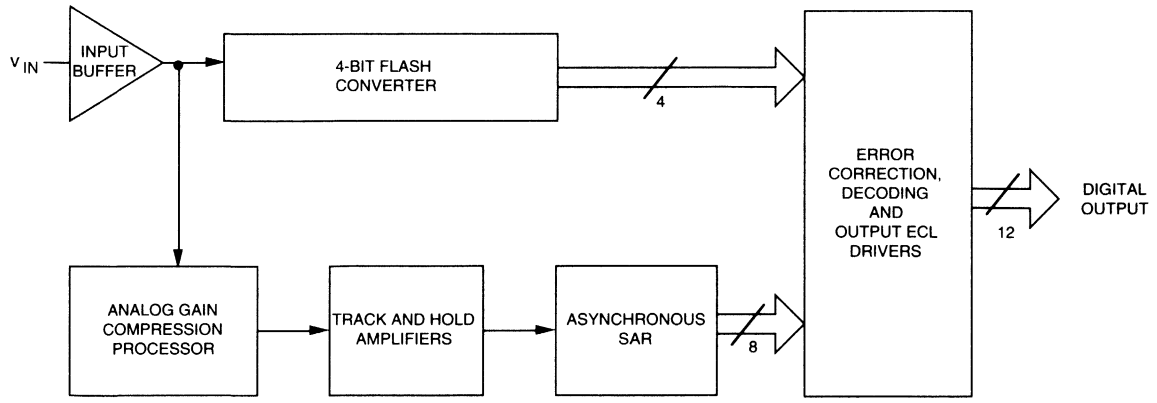
GENERAL DESCRIPTION

The SPT7910 A/D converter is industry's first 12-bit monolithic A-to-D converter capable of sample rates greater than 10 MSPS. On board input buffer and track/hold function assures excellent dynamic performance without the need for external components. Drive requirement problems are minimized with an input capacitance of only 5 pF.

Inputs and outputs are ECL to provide a higher level of noise immunity in high speed system applications. An overrange output signal is provided to indicate overflow conditions. Output data format is straight binary. Power dissipation is very low at only 1.4 watts with power supply voltages of +5.0 and -5.2 volts. The SPT7910 also provides a wide input voltage range of ±2.0 volts.

The SPT7910 is available in a small 32-lead ceramic sidebrazed DIP package and in die form. A commercial temperature range of 0 to +70 °C is currently offered. A surface mount package, military temperature, and /883 processed units will be available in the near future.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Beyond which damage may occur)[1] 25 °C

Supply Voltages

V_{CC} ..... +6 V
V_{EE} ..... -6 V

Input Voltages

Analog Input ..... $V_{FB} \leq V_{IN} \leq V_{FT}$
V_{FT}, V_{FB} ..... +3.0 V, -3.0 V
Reference Ladder Current ..... 12 mA

Output

Digital Outputs ..... 0 to -30 mA

Temperature

Operating Temperature ..... 0 to 70 °C
Junction Temperature ..... 175 °C
Lead Temperature, (soldering 10 seconds) ..... 300 °C
Storage Temperature ..... -65 to +150 °C

Note: 1. Operation at any Absolute Maximum Rating is not implied. See Electrical Specifications for proper nominal applied conditions in typical applications.

ELECTRICAL SPECIFICATIONS

$T_A=T_{MIN}$ to T_{MAX}, V_{CC}=+5.0 V, V_{EE}=-5.2 V, DV_{CC}=+5.0 V, V_{IN}=±2.0 V, V_{SB}=-2.0 V, V_{ST}=+2.0 V, f_{clock}=10 MHz, 50% clock duty cycle, unless otherwise specified.

PARAMETERS	TEST CONDITIONS	TEST LEVEL	SPT7910 MIN	SPT7910 TYP	SPT7910 MAX	UNITS
Resolution			12			Bits
DC Accuracy (+25 °C)						
Integral Nonlinearity	± Full Scale	I		±2.0		LSB
Differential Nonlinearity	250 kHz Sample Rate	I		±0.8		LSB
No Missing Codes		I		Guaranteed		
Analog Input						
Input Voltage Range		VI		±2.0		V
Input Bias Current		VI		30	60	µA
Input Resistance	V_{IN}=0 V	VI	100	300		kΩ
Input Capacitance		V		5		pF
Input Bandwidth	3 dB Small Signal	V		120		MHz
+FS Error		V		±5.0		LSB
-FS Error		V		±5.0		LSB
Reference Input						
Reference Ladder Resistance		VI	600	900		Ω
Reference Ladder Tempco		V		0.8		Ω/°C
Timing Characteristics						
Maximum Conversion Rate		VI	10			MHz
Overvoltage Recovery Time		V		20		ns
Pipeline Delay (Latency)		VI			1	Clock Cycle
Output Delay		V		14	18	ns
Aperture Delay Time		V		1		ns
Aperture Jitter Time		V		5		ps-RMS
Dynamic Performance						
Effective Number of Bits						
fin=500 kHz				10.2		Bits
fin=1.0 MHz				10.0		Bits
fin=3.58 MHz				9.5		Bits
Signal-To-Noise Ratio (without Harmonics)						
fin=500 kHz	+25 °C	I	64	67		dB
	T_{MIN} to T_{MAX}	IV	58	61		dB
fin=1 MHz	+25 °C	I	64	66		dB
	T_{MIN} to T_{MAX}	IV	58	60		dB
fin=3.58 MHz	+25 °C	I	62	64		dB
	T_{MIN} to T_{MAX}	IV	58	60		dB

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ELECTRICAL SPECIFICATIONS

$T_A=T_{MIN}$ to T_{MAX}, V_{CC}=+5.0 V, V_{EE}=-5.2 V, DV_{CC}=+5.0 V, V_{IN}=±2.0 V, V_{SB}=-2.0 V, V_{ST}=+2.0 V, f_{clock}=10 MHz, 50% clock duty cycle, unless otherwise specified.

PARAMETERS	TEST CONDITIONS	TEST LEVEL	SPT7910 MIN	SPT7910 TYP	SPT7910 MAX	UNITS
Dynamic Performance						
Harmonic Distortion[2]						
fin=500 kHz	+25 °C	I	63	66		dB
	T_{MIN} to T_{MAX}	IV	59	62		dB
fin=1.0 MHz	+25 °C	I	63	65		dB
	T_{MIN} to T_{MAX}	IV	59	61		dB
fin=3.58 MHz	+25 °C	I	59	61		dB
	T_{MIN} to T_{MAX}	IV	57	59		dB
Signal-to-Noise and Distortion						
fin=500 kHz	+25 °C	I	60	63		dB
	T_{MIN} to T_{MAX}	IV	55	58		dB
fin=1.0 MHz	+25 °C	I	60	62		dB
	T_{MIN} to T_{MAX}	IV	55	57		dB
fin=3.58 MHz	+25 °C	I	57	59		dB
	T_{MIN} to T_{MAX}	IV	54	56		dB
Spurious Free Dynamic Range[3]	+25 °C	V		74		dB
Differential Phase[4]	+25 °C	V		0.2		Degree
Differential Gain[4]	+25 °C	V		0.7		%
Digital Inputs						
Logic "1" Voltage		V	-1.1			V
Logic "0" Voltage		V			-1.5	V
Maximum Input Current Low		II	-500	±200	+750	µA
Maximum Input Current High		II	-500	±300	+750	µA
Pulse Width Low (CLK)		IV	30			ns
Pulse Width High (CLK)		IV	30		300	ns
Digital Outputs						
Logic "1" Voltage	50 Ω to -2 V	II	-1.1	-0.8		V
Logic "0" Voltage	50 Ω to -2 V	II		-1.8	-1.5	V
Power Supply Requirements						
Voltages V_{CC}		IV	+4.75		+5.25	V
$-V_{EE}$		IV	-4.95		-5.45	V
Currents I_{CC}		II		150	190	mA
$-I_{EE}$		II		125	160	mA
Power Dissipation	Outputs Open	II		1.4	1.8	W
Power Supply Rejection Ratio	(5 V±0.25 V, -5.2 V ±0.25 V)	V		1.0		LSB

[1] Typical thermal impedances (unsoldered, in free air): 32L sidebrazed DIP. θ_{ja} = 50 °C/W.
[2] 64 distortion BINS from 4096 pt FFT.
[3] fin = 1 MHz.
[4] fin = 3.58 and 4.35 MHz.

Figure 1A: Timing Diagram

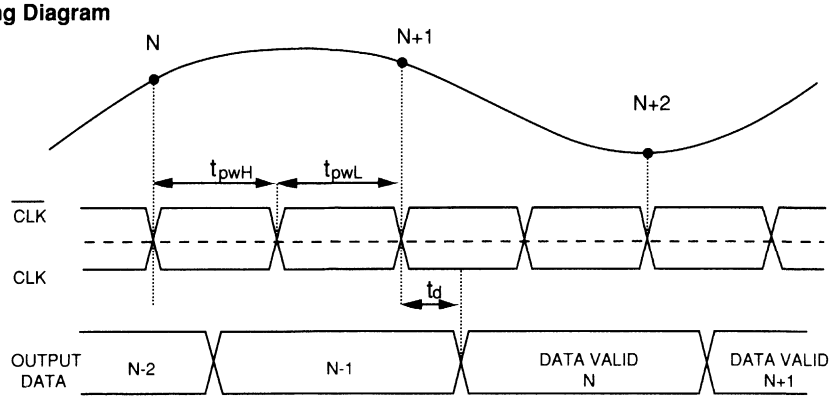

Figure 1B: Single Event Clock

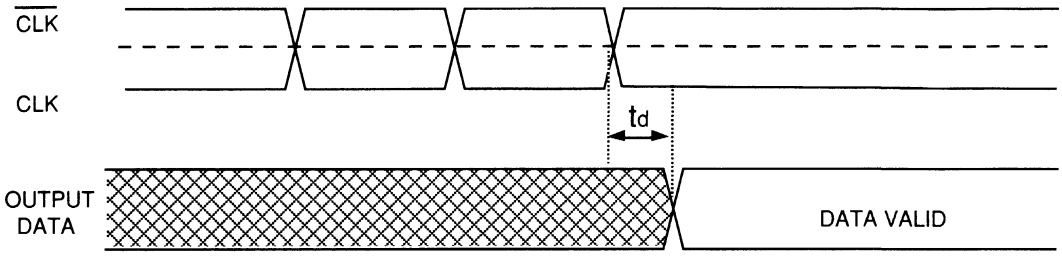

Table 1 - Timing Parameters

PARAMETERS	DESCRIPTION	MIN	TYP	MAX	UNITS
t_d	CLK to Data Valid Prop Delay	-	14	18	ns
t_{pwH}	CLK High Pulse Width	30	-	300	ns
t_{pwL}	CLK Low Pulse Width	30	-	-	ns

TEST LEVEL CODES

All electrical characteristics are subject to the following conditions:

All parameters having min/max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality Assurance inspection. Any blank section in the data column indicates that the specification is not tested at the specified condition.

Unless otherwise noted, all tests are pulsed tests; therefore, $T_J = T_C = T_A$.

TEST LEVEL	TEST PROCEDURE
I	100% production tested at the specified temperature.
II	100% production tested at T_A=25 °C, and sample tested at the specified temperatures.
III	QA sample tested only at the specified temperatures.
IV	Parameter is guaranteed (but not tested) by design and characterization data.
V	Parameter is a typical value for information purposes only.
VI	100% production tested at T_A = 25 °C. Parameter is guaranteed over specified temperature range.

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SPECIFICATION DEFINITIONS

APERTURE DELAY

Aperture delay represents the point in time, relative to the rising edge of the CLOCK input, that the analog input is sampled.

APERTURE JITTER

The variations in aperture delay for successive samples.

DIFFERENTIAL GAIN (DG)

A signal consisting of a sine wave superimposed on various DC levels is applied to the input. Differential gain is the maximum variation in the sampled sine wave amplitudes at these DC levels.

DIFFERENTIAL PHASE (DP)

A signal consisting of a sine wave superimposed on various DC levels that is applied to the input. Differential phase is the maximum variation in the sampled sine wave phases at these DC levels.

EFFECTIVE NUMBER OF BITS (ENOB)

SINAD = 6.02N + 1.76, where N is equal to the effective number of bits.

$$N = \frac{SINAD - 1.76}{6.02}$$

+/- FULL-SCALE ERROR (GAIN ERROR)

Difference between measured full scale response [(+Fs) - (-Fs)] and the theoretical response (+4 V -2 LSBs) where the +FS (full scale) input voltage is defined as the output transition between 1-10 and 1-11 and the -FS input voltage is defined as the output transition between 0-00 and 0-01.

INPUT BANDWIDTH

Small signal (50 mV) bandwidth (3 dB) of analog input stage.

DIFFERENTIAL NONLINEARITY (DNL)

Error in the width of each code from its theoretical value. (Theoretical = $V_{FS}/2^N$)

INTEGRAL NONLINEARITY (INL)

Linearity error refers to the deviation of each individual code (normalized) from a straight line drawn from -Fs through +Fs. The deviation is measured from the edge of each particular code to the true straight line.

OUTPUT DELAY

Time between the clock's triggering edge and output data valid.

OVERVOLTAGE RECOVERY TIME

The time required for the ADC to recover to full accuracy after an analog input signal 125% of full scale is reduced to 50% of the full-scale value.

SIGNAL-TO-NOISE RATIO (SNR)

The ratio of the fundamental sinusoid power to the total noise power. Harmonics are excluded.

SIGNAL-TO-NOISE AND DISTORTION (SINAD)

The ratio of the fundamental sinusoid power to the total noise and distortion power.

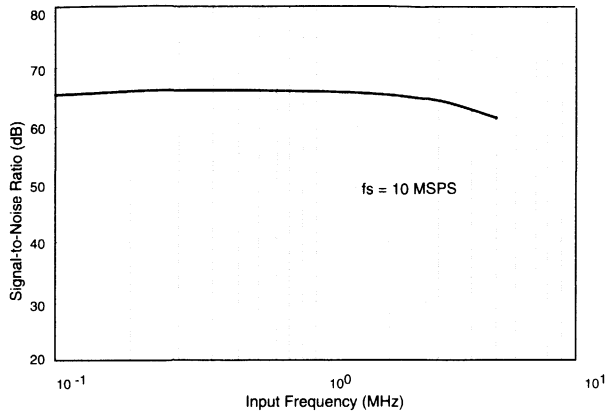
TOTAL HARMONIC DISTORTION (THD)

The ratio of the total power of the first 64 harmonics to the power of the measured sinusoidal signal.

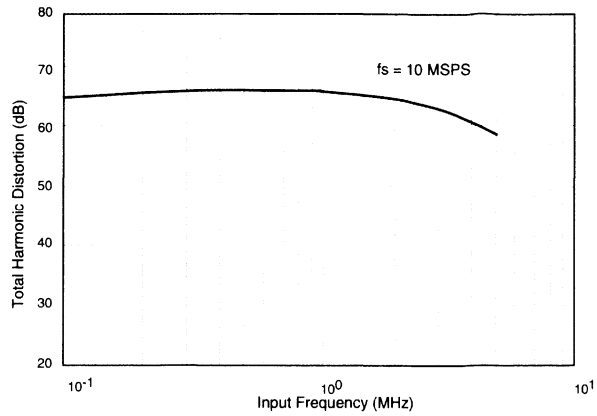
SPURIOUS FREE DYNAMIC RANGE (SFDR)

The ratio of the fundamental sinusoidal amplitude to the single largest harmonic or spurious signal.

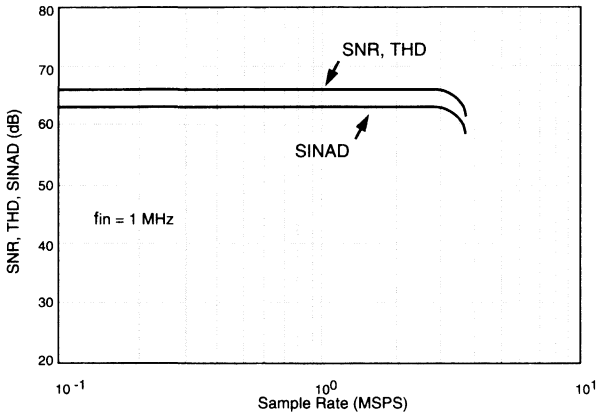
SNR vs Input Frequency



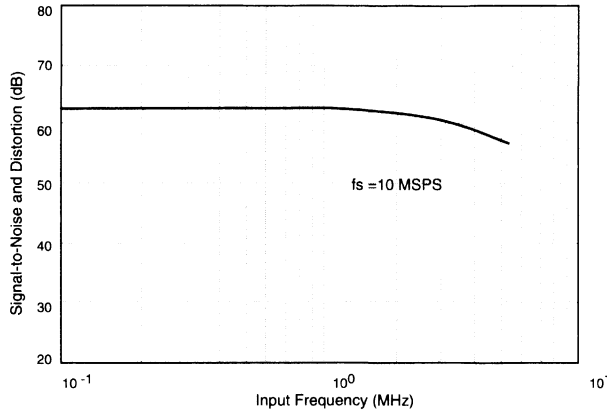
THD vs Input Frequency



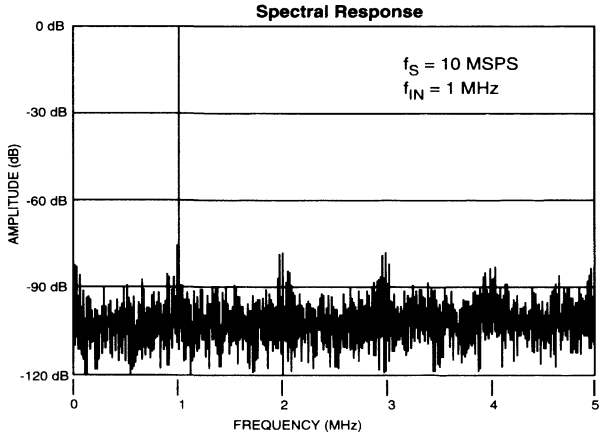
SNR, THD, SINAD vs Sample Rate



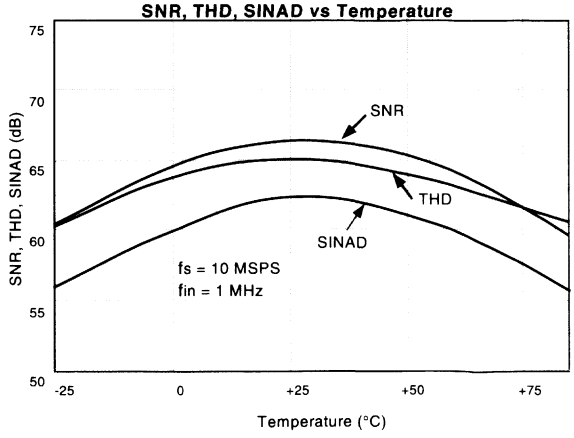
SINAD vs Input Frequency



SPT7910
Spectral Response



SNR, THD, SINAD vs Temperature



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TYPICAL INTERFACE CIRCUIT

The SPT7910 requires few external components to achieve the stated operation and performance. Figure 2 shows the typical interface requirements when using the SPT7910 in normal circuit operation. The following section provides a description of the pin functions and outlines critical performance criteria to consider for achieving the optimal device performance.

POWER SUPPLIES AND GROUNDING

The SPT7910 requires the use of two supply voltages, V_{EE} and V_{CC}. Both supplies should be treated as analog supply sources. This means the V_{EE} and V_{CC} ground returns of the device should both be connected to the analog ground plane. All other -5.2 V requirements of the external digital logic circuit should be connected to the digital ground plane. Each power supply pin should be bypassed as closely as possible to the device with .01 µF and 10 µF capacitors as shown in Figure 2.

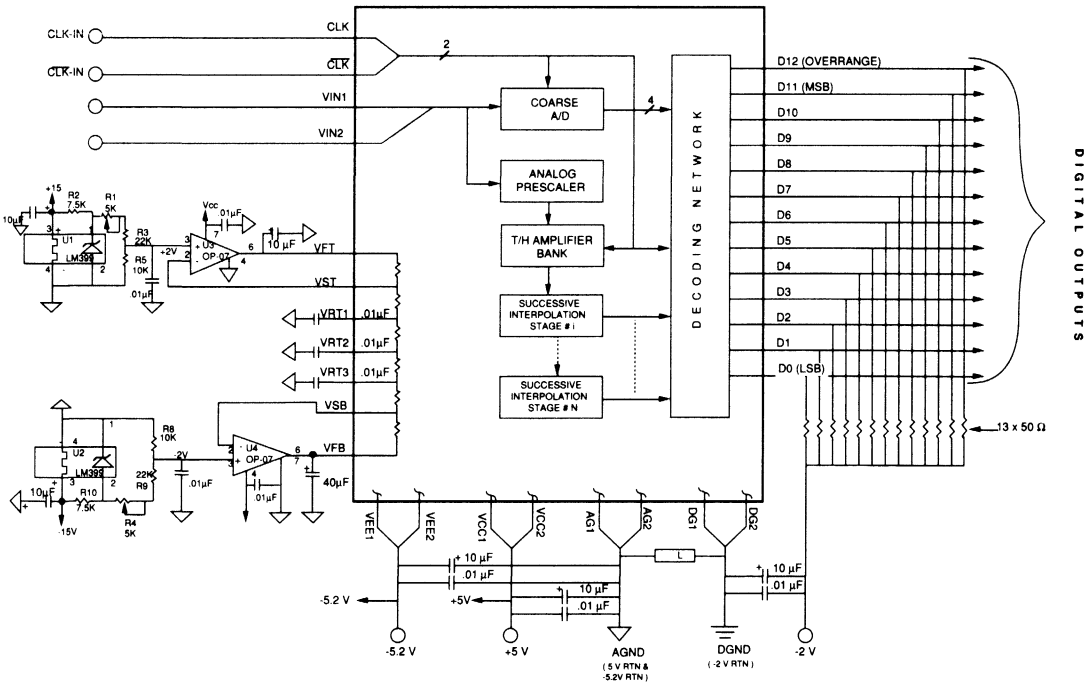
The two grounds available on the SPT7910 are AGND and DGND. DGND is used only for ECL outputs and is to be referenced to the output pulldown voltage. These grounds are not tied together internal to the device. The use of ground planes is recommended to achieve the best performance of the SPT7910. The AGND and the DGND ground planes should be separated from each other and only connected together at the device through an inductance or ferrite bead. Doing this will minimize the ground noise pickup.

VOLTAGE REFERENCE

The SPT7910 requires the use of two voltage references: V_{FT} and V_{FB}. V_{FT} is the force for the top of the voltage reference ladder (+2.5 V typ), V_{FB} (-2.5 V typ) is the force for the bottom of the voltage reference ladder. Both voltages are applied across an internal reference ladder resistance of 900 ohms. In addition, there are five reference ladder taps (V_{ST}, V_{RT1}, V_{RT2}, V_{RT3}, and V_{SB}). V_{ST} is the sense for the top of the reference ladder (+2.0 V), V_{RT2} is the midpoint of the ladder (0.0 V typ) and V_{SB} is the sense for the bottom of the reference ladder (-2.0 V). V_{RT1} and V_{RT3} are quarter point ladder taps (+1.0 and -1.0 V typical, respectively). The voltages seen at V_{ST} and V_{SB} are the true full scale input voltages of the device when V_{FT} and V_{FB} are driven to the recommended voltages (+2.5 V and -2.5 V typical respectively). V_{ST} and V_{SB} should be used to monitor the actual full scale input voltage of the device. V_{RT1}, V_{RT2} and V_{RT3} should not be driven to the expected ideal values as is commonly done with standard flash converters. When not being used, a decoupling capacitor of .01 uF connected to AGND from each tap is recommended to minimize high frequency noise injection.

The analog input range will scale proportionally with respect to the reference voltage if a different input range is required.

Figure 2 - Typical Interface Circuit



The maximum scaling factor for device operation is ± 4% of the recommended reference voltages of V_{FT} and V_{FB}. However, because the device is laser trimmed to optimize performance with V_{SB} and V_{ST} equal to -2.0 V and +2.0 V respectively, the accuracy of the device will degrade if operated beyond a ± 2% range.

The following errors are defined:

+FS error = top of ladder offset voltage = $\Delta(+FS - V_{ST})$
-FS error = bottom of ladder offset voltage = $\Delta(-FS - V_{SB})$

Where the +FS (full scale) input voltage is defined as the input approximately 1 LSB above the output transition of 1—10 and 1—11 and the -FS input voltage is defined as the input approximately 1 LSB below the output transition of 0—00 and 0—01.

An example of a typical reference driver circuit is shown in figure 2. This circuit is to be used to minimize the +FS and -FS errors over temperature. U1 and U2 are LM339s with an output voltage of +2 V and -2 V respectively. U3 and U4 are recommended to be OP-07s or equivalent. The input offset of these devices is 150 uV maximum. This circuit uses a true force and sense when driving the reference ladder of the SPT7910. U3 sources the current through V_{FT} (V_{ST} is a sense) while U4 is sinking current through V_{FB} (V_{SB} is a sense). To calibrate the reference, adjust R1 for V_{ST}=+2.0 V (V_{FT} will be typically +2.5 V) and adjust R4 for V_{SB}=-2.0 V (V_{FB} will be typically -2.5 V). This circuit is preferred because it allows the user to know exactly what the full scale input voltage is.

ANALOG INPUT

V_{IN1} and V_{IN2} are the analog inputs. Both inputs are tied to the same point internally. Either one may be used as an analog input "sense" and the other for an input "force." The inputs can also be tied together and driven from the same source. The full scale input range will be 80% of the reference voltage or ±2 volts with V_{FB}=-2.5 V and V_{FT}=+2.5 V.

The drive requirements for the analog inputs are minimal when compared to conventional Flash converters due the SPT7910's extremely low input capacitance of only 5 pF and very high input impedance of 300 kΩ. For example, for an input signal of ± 2 V p-p with an input frequency of 10 MHz, the peak output current required for the driving circuit is only 628 µA.

CLOCK INPUT

The clock inputs (CLK, $\overline{CLK}$) are designed to be driven differentially with ECL levels. Differential clock driving is highly recommended to minimize the effects of clock jitter. The clock may be driven single ended since $\overline{CLK}$ is internally biased to -1.3 V. $\overline{CLK}$ may be left open, but a .01 µF bypass capacitor to AGND is recommended. As with all high speed circuits, proper terminations are required to avoid signal reflections and possible ringing that can cause the device to trigger at an unwanted time.

The clock input duty cycle should be 50% where possible, but performance will not be degraded if kept within the range of 40-60%. However, in any case the clock pulse width (tpwH) must be kept at 300 ns maximum to ensure proper operation of the internal track and hold amplifier (see timing diagram). The analog input signal is latched on the rising edge of the CLK.

DIGITAL OUTPUTS

The format of the output data (D0-D11) is straight binary. (See table 2.) These outputs are ECL 10K and 10KH compatible with the output circuit shown in Figure 3. The outputs are latched on the rising edge of CLK with a propagation delay of 5 ns. There is a one clock cycle latency between CLK and the valid output data (see timing diagram). These digital outputs can drive 50 ohms to ECL levels when pulled down to -2 V. Output loading pulled down to -5.2 V is not recommended. The total specified power dissipation of the device does not include the power used by these loads. The additional power used by these loads can vary between 10 and 300 mW typically (including the overrange load) depending on the output codes. If lower power levels are desired, the output loads can be reduced, but careful consideration to the resistive and capacitive loads in relation to the operating frequency must be considered.

Table 2 - Output Data Information

ANALOG INPUT	OVERRANGE D12	OUTPUT CODE D11-DO
>+2.0 V + 1/2 LSB	1	1111 1111 1111
+2.0 V -1 LSB	O	1111 1111 111Ø
0.0 V	O	ØØØØ ØØØØ ØØØØ
-2.0 V +1 LSB	O	OOOO OOOO OOOØ
<2.0 V	O	OOOO OOOO OOOO

(Ø indicates the flickering bit between logic 0 and 1).

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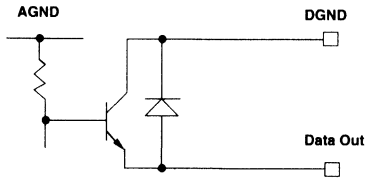
Figure 3 - Output Circuit



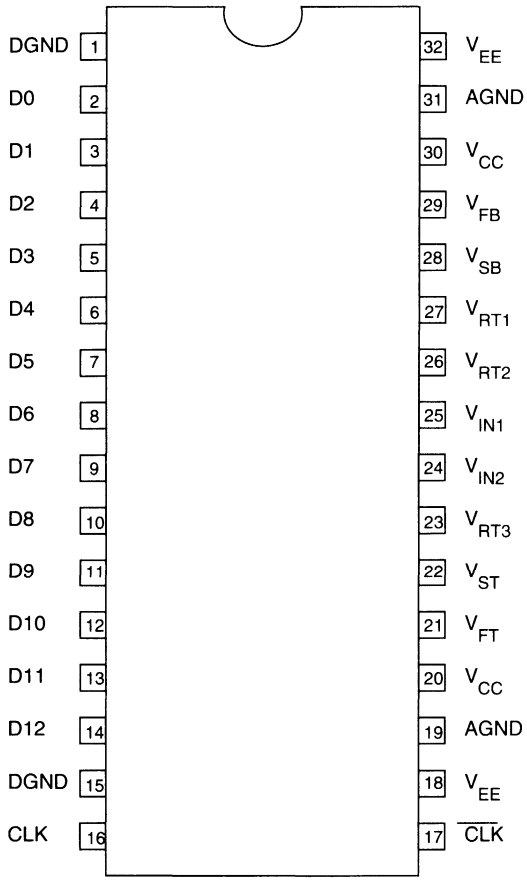
OVERRANGE OUTPUT

The OVERRANGE OUTPUT (D12) is an indication that the analog input signal has exceeded the full scale input voltage by 1 LSB. When this condition occurs, the output will switch to logic 1. All other data outputs are unaffected by this operation. This feature makes it possible to include the SPT7910 into higher resolution systems.

EVALUATION BOARD

The EB7910 Evaluation Board is available to aid designers in demonstrating the full performance of the SPT7910. This board includes a reference circuit, clock driver circuit, output data latches and an on-board reconstruction of the digital data. An application note (AN7910) describing the operation of this board as well as information on the testing of the SPT7910 is also available. Contact the factory for price and availability.

PIN ASSIGNMENT



PIN FUNCTIONS

NAME	FUNCTION
DGND	Digital Ground
AGND	Analog Ground
D0-D11	ECL Outputs (D0=LSB)
D12	ECL Output Overrange
CLK	Clock
$\overline{CLK}$	Inverted Clock
V_{EE}	-5.2 V Supply
V_{CC}	+5.0 V supply
$V_{RT1}, V_{RT2}, V_{RT3}$	Voltage Reference Taps
V_{IN1}, V_{IN2}	Inputs (tied together at the die)
V_{FT}	Force for Top of Reference Ladder
V_{ST}	Sense for Top of Reference Ladder
V_{FB}	Force for Bottom of Reference Ladder
V_{SB}	Sense for Bottom of Reference Ladder

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LEADERSHIP IN DATA CONVERSION AND SIGNAL PROCESSING

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SIGNAL PROCESSING TECHNOLOGIES

SPT7912

12-BIT, 30 MSPS, ECL, A/D CONVERTER

FEATURES

- Monolithic
- 12-Bit 30 MSPS Converter
- 65 dB SNR @ 1 MHz Input
- On-Chip Track/Hold
- Bipolar ±2.0 V Analog Input
- Low Power (1.4 W Typical)
- 5 pF input Capacitance
- ECL Outputs

APPLICATIONS

- Radar Receivers
- Professional Video
- Instrumentation
- Medical Imaging
- Electronic Warfare
- Digital Communications
- Digital Spectrum Analyzers
- Electro-optics

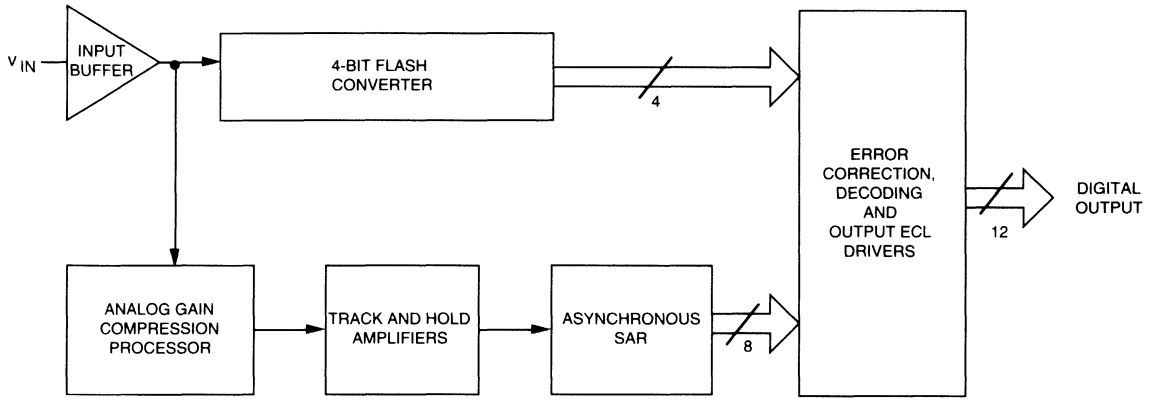
GENERAL DESCRIPTION

The SPT7912 A/D converter is industry's first 12-bit monolithic A-to-D converter capable of sample rates greater than 30 MSPS. On board input buffer and track/hold function assures excellent dynamic performance without the need for external components. Drive requirement problems are minimized with an input capacitance of only 5 pF.

Inputs and outputs are ECL to provide a higher level of noise immunity in high speed system applications. An overrange output signal is provided to indicate overflow conditions. Output data format is straight binary. Power dissipation is very low at only 1.4 watts with power supply voltages of +5.0 and -5.2 volts. The SPT7912 also provides a wide input voltage range of ±2.0 volts.

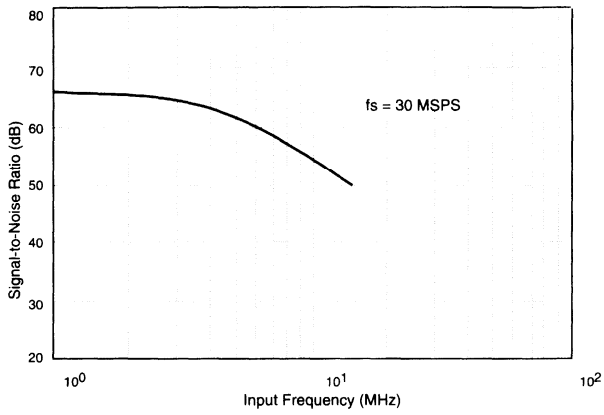
The SPT7912 is available in a small 32-lead ceramic sidebrazed DIP package and in die form. A commercial temperature range of 0 to +70 °C is currently offered. Contact the factory for availability of surface mount packages, military temperature, and /883 processed units.

BLOCK DIAGRAM

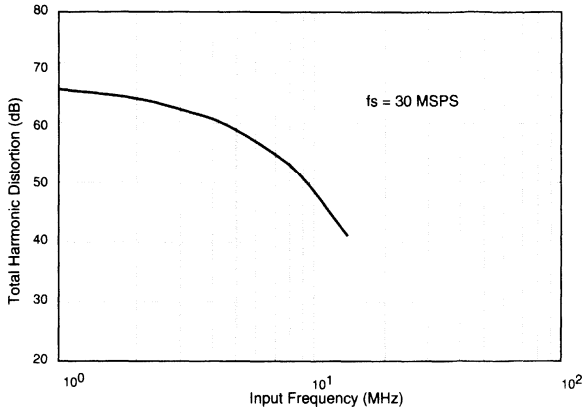


PERFORMANCE CHARACTERISTICS

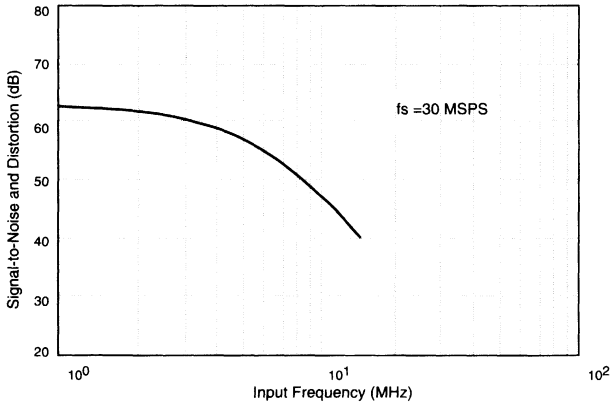
SNR vs Input Frequency



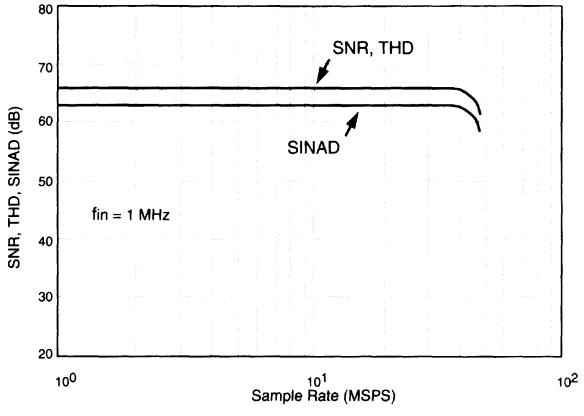
THD vs Input Frequency



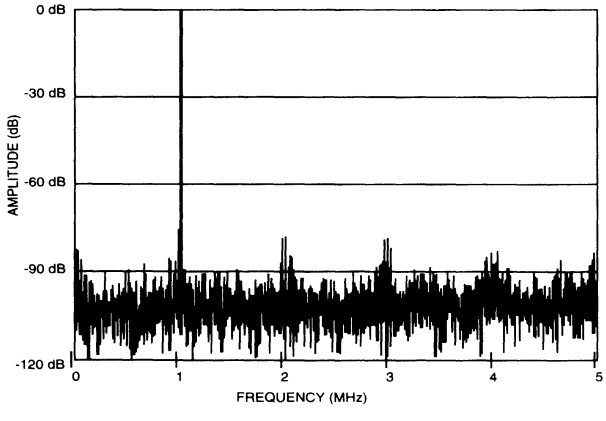
SINAD vs Input Frequency



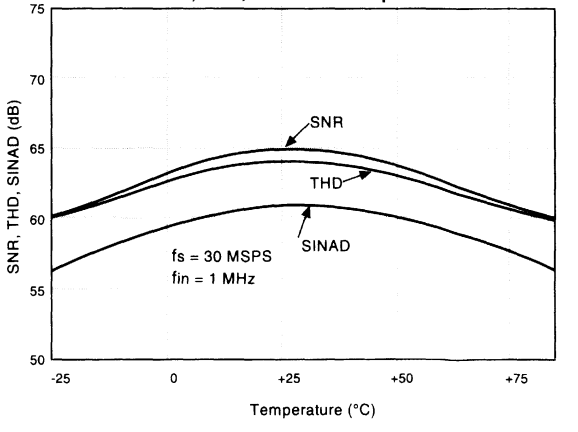
SNR, THD, SINAD vs Sample Rate



SPT7912
Spectral Response



SNR, THD, SINAD vs Temperature



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TYPICAL INTERFACE CIRCUIT

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POWER SUPPLIES AND GROUNDING

The SPT7912 requires the use of two supply voltages, V_{EE} and V_{CC}. Both supplies should be treated as analog supply sources. This means the V_{EE} and V_{CC} ground returns of the device should both be connected to the analog ground plane. All other -5.2 V requirements of the external digital logic circuit should be connected to the digital ground plane. Each power supply pin should be bypassed as closely as possible to the device with .01 µF and 10 µF capacitors as shown in Figure 2.

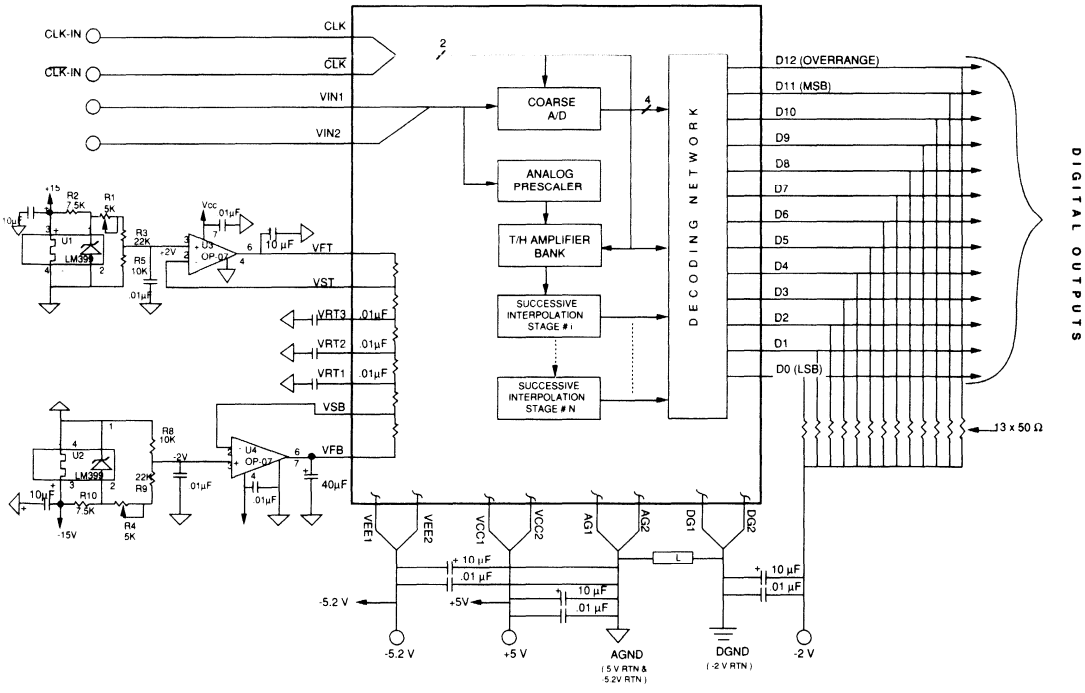
The two grounds available on the SPT7912 are AGND and DGND. DGND is used only for ECL outputs and is to be referenced to the output pulldown voltage. These grounds are not tied together internal to the device. The use of ground planes is recommended to achieve the best performance of the SPT7912. The AGND and the DGND ground planes should be separated from each other and only connected together at the device through an inductance or ferrite bead. Doing this will minimize the ground noise pickup.

VOLTAGE REFERENCE

The SPT7912 requires the use of two voltage references: V_{FT} and V_{FB}. V_{FT} is the force for the top of the voltage reference ladder (+2.5 V typ), V_{FB} (-2.5 V typ) is the force for the bottom of the voltage reference ladder. Both voltages are applied across an internal reference ladder resistance of 900 ohms. In addition, there are five reference ladder taps (V_{ST}, V_{RT1}, V_{RT2}, V_{RT3}, and V_{SB}). V_{ST} is the sense for the top of the reference ladder (+2.0 V), V_{RT2} is the midpoint of the ladder (0.0 V typ) and V_{SB} is the sense for the bottom of the reference ladder (-2.0 V). V_{RT1} and V_{RT3} are quarter point ladder taps (+1.0 and -1.0 V typical, respectively). The voltages seen at V_{ST} and V_{SB} are the true full scale input voltages of the device when V_{FT} and V_{FB} are driven to the recommended voltages (+2.5 V and -2.5 V typical respectively). V_{ST} and V_{SB} should be used to monitor the actual full scale input voltage of the device. V_{RT1}, V_{RT2} and V_{RT3} should not be driven to the expected ideal values as is commonly done with standard flash converters. When not being used, a decoupling capacitor of .01 uF connected to AGND from each tap is recommended to minimize high frequency noise injection.

The analog input range will scale proportionally with respect to the reference voltage if a different input range is required.

Figure 2 - Typical Interface Circuit



The maximum scaling factor for device operation is ± 4% of the recommended reference voltages of V_{FT} and V_{FB}. However, because the device is laser trimmed to optimize performance with V_{SB} and V_{ST} equal to -2.0 V and +2.0 V respectively, the accuracy of the device will degrade if operated beyond a ± 2% range.

The following errors are defined:

+FS error = top of ladder offset voltage = $\Delta(+FS - V_{ST})$
-FS error = bottom of ladder offset voltage = $\Delta(-FS - V_{SB})$

Where the +FS (full scale) input voltage is defined as the input approximately 1 LSB above the output transition of 1—10 and 1—11 and the -FS input voltage is defined as the input approximately 1 LSB below the output transition of 0—00 and 0—01.

An example of a typical reference driver circuit is shown in figure 2. This circuit is to be used to minimize the +FS and -FS errors over temperature. U1 and U2 are LM339s with an output voltage of +2 V and -2 V respectively. U3 and U4 are recommended to be OP-07s or equivalent. The input offset of these devices is 150 uV maximum. This circuit uses a true force and sense when driving the reference ladder of the SPT7912. U3 sources the current through V_{FT} (V_{ST} is a sense) while U4 is sinking current through V_{FB} (V_{SB} is a sense). To calibrate the reference, adjust R1 for V_{ST}=+2.0 V (V_{FT} will be typically +2.5 V) and adjust R4 for V_{SB}=-2.0 V (V_{FB} will be typically -2.5 V). This circuit is preferred because it allows the user to know exactly what the full scale input voltage is.

ANALOG INPUT

V_{IN1} and V_{IN2} are the analog inputs. Both inputs are tied to the same point internally. Either one may be used as an analog input "sense" and the other for an input "force." The inputs can also be tied together and driven from the same source. The full scale input range will be 80% of the reference voltage or ±2 volts with V_{FB}=-2.5 V and V_{FT}=+2.5 V.

The drive requirements for the analog inputs are minimal when compared to conventional Flash converters due the SPT7912's extremely low input capacitance of only 5 pF and very high input impedance of 300 kΩ. For example, for an input signal of ± 2 V p-p with an input frequency of 10 MHz, the peak output current required for the driving circuit is only 628 µA.

CLOCK INPUT

The clock inputs (CLK, $\overline{CLK}$) are designed to be driven differentially with ECL levels. Differential clock driving is highly recommended to minimize the effects of clock jitter. The clock may be driven single ended since $\overline{CLK}$ is internally biased to -1.3 V. $\overline{CLK}$ may be left open, but a .01 µF bypass capacitor to AGND is recommended. As with all high speed circuits, proper terminations are required to avoid signal reflections and possible ringing that can cause the device to trigger at an unwanted time.

The clock input duty cycle should be 50% where possible, but performance will not be degraded if kept within the range of 40-60%. However, in any case the clock pulse width (tpwH) must be kept at 300 ns maximum to ensure proper operation of the internal track and hold amplifier (see timing diagram). The analog input signal is latched on the rising edge of the CLK.

DIGITAL OUTPUTS

The format of the output data (D0-D11) is straight binary. (See table 2.) These outputs are ECL 10K and 10KH compatible with the output circuit shown in Figure 3. The outputs are latched on the rising edge of CLK with a propagation delay of 5 ns. There is a one clock cycle latency between CLK and the valid output data (see timing diagram). These digital outputs can drive 50 ohms to ECL levels when pulled down to -2 V. Output loading pulled down to -5.2 V is not recommended. The total specified power dissipation of the device does not include the power used by these loads. The additional power used by these loads can vary between 10 and 300 mW typically (including the overrange load) depending on the output codes. If lower power levels are desired, the output loads can be reduced, but careful consideration to the resistive and capacitive loads in relation to the operating frequency must be considered.

Table 2 - Output Data Information

ANALOG INPUT	OVERRANGE D12	OUTPUT CODE D11-DO
>+2.0 V + 1/2 LSB	1	1111 1111 1111
+2.0 V -1 LSB	0	1111 1111 111Ø
0.0 V	0	ØØØØ ØØØØ ØØØØ
-2.0 V +1 LSB	0	0000 0000 000Ø
<2.0 V	0	0000 0000 0000

(Ø indicates the flickering bit between logic 0 and 1).

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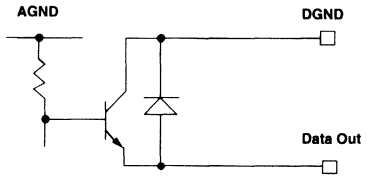
Figure 3 - Output Circuit



OVERRANGE OUTPUT

The OVERRANGE OUTPUT (D12) is an indication that the analog input signal has exceeded the full scale input voltage by 1 LSB. When this condition occurs, the output will switch to logic 1. All other data outputs are unaffected by this operation. This feature makes it possible to include the SPT7912 into higher resolution systems.

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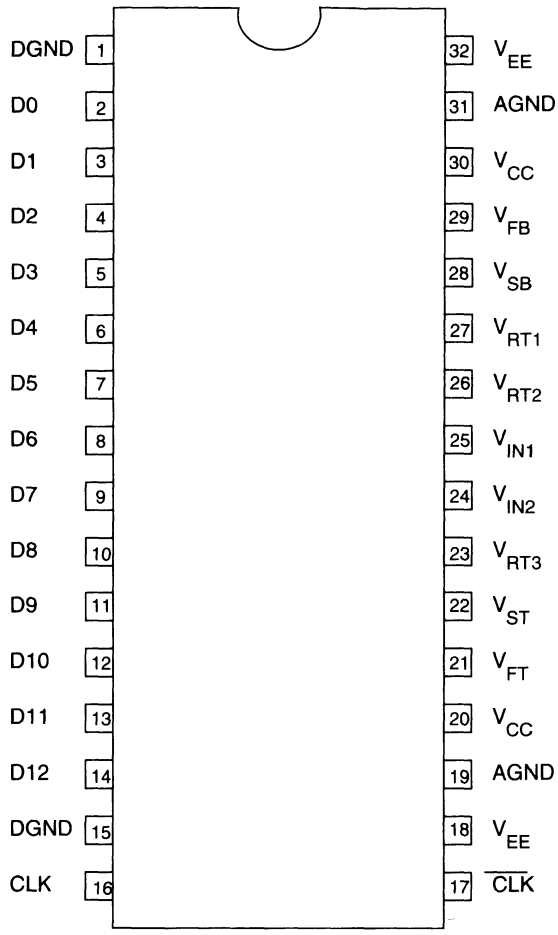

PIN FUNCTIONS

NAME	FUNCTION
DGND	Digital Ground
AGND	Analog Ground
D0-D11	ECL Outputs (D0=LSB)
D12	ECL Output Overrange
CLK	Clock
$\overline{CLK}$	Inverted Clock
V_{EE}	-5.2 V Supply
V_{CC}	+5.0 V supply
V_{RT1},V_{RT2},V_{RT3}	Voltage Reference Taps
V_{IN1}, V_{IN2}	Inputs (tied together at the die)
V_{FT}	Force for Top of Reference Ladder
V_{ST}	Sense for Top of Reference Ladder
V_{FB}	Force for Bottom of Reference Ladder
V_{SB}	Sense for Bottom of Reference Ladder

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LEADERSHIP IN DATA CONVERSION AND SIGNAL PROCESSING

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SIGNAL PROCESSING TECHNOLOGIES

SPT7920

12-BIT, 10 MSPS, TTL, A/D CONVERTER

FEATURES

- Monolithic
- 12-Bit 10 MSPS Converter
- 66 dB SNR @ 1 MHz Input
- On-Chip Track/Hold
- Bipolar ±2.0 V Analog Input
- Low Power (1.1 W Typical)
- 5 pF input Capacitance
- TTL Outputs

APPLICATIONS

- Radar Receivers
- Professional Video
- Instrumentation
- Medical Imaging
- Electronic Warfare
- Digital Communications
- Digital Spectrum Analyzers
- Electro-optics

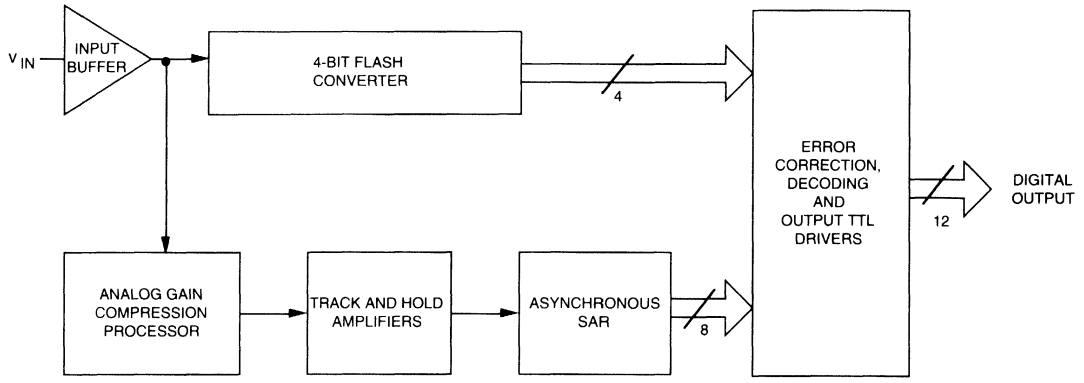
GENERAL DESCRIPTION

The SPT7920 A/D converter is the industry's first 12-bit monolithic A-to-D converter capable of sample rates greater than 10 MSPS. On board input buffer and track/hold function assures excellent dynamic performance without the need for external components. Drive requirement problems are minimized with an input capacitance of only 5 pF.

Logic inputs and outputs are TTL. An overrange output signal is provided to indicate overflow conditions. Output data format is straight binary. Power dissipation is very low at only 1.1 watts with power supply voltages of +5.0 and -5.2 volts. The SPT7920 also provides a wide input voltage range of ±2.0 volts.

The SPT7920 is available in a small 32-lead ceramic sidebrazed DIP package. A commercial temperature range of 0 to +70 °C is currently offered. A surface-mount package, die, military temperature, and /883 processed units will be available in the near future. Consult the factory for availability.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Beyond which damage may occur)[1] 25 °C

Supply Voltages

V_{CC} ..... +6 V
V_{EE} ..... -6 V

Input Voltages

Analog Input ..... $V_{FB} \leq V_{IN} \leq V_{FT}$
V_{FT}, V_{FB} ..... +3.0 V, -3.0 V
Reference Ladder Current ..... 12 mA
CLK IN ..... V_{CC}

Output

Digital Outputs ..... 0 to -30 mA

Temperature

Operating Temperature ..... 0 to 70 °C
Junction Temperature ..... 175 °C
Lead Temperature, (soldering 10 seconds) ..... 300 °C
Storage Temperature ..... -65 to +150 °C

Note: 1. Operation at any Absolute Maximum Rating is not implied. See Electrical Specifications for proper nominal applied conditions in typical applications.

ELECTRICAL SPECIFICATIONS

$T_A=T_{MIN}$ to T_{MAX}, V_{CC}=+5.0 V, V_{EE}=-5.2 V, DV_{CC}=+5.0 V, V_{IN}=±2.0 V, V_{SB}=-2.0 V, V_{ST}=+2.0 V, f_{clock}=10 MHz, 50% clock duty cycle, unless otherwise specified.

PARAMETERS	TEST CONDITIONS	TEST LEVEL	SPT7920 MIN	SPT7920 TYP	SPT7920 MAX	UNITS
Resolution			12			Bits
DC Accuracy (+25 °C)						
Integral Nonlinearity	± Full Scale	I		±2.0		LSB
Differential Nonlinearity	250 kHz Sample Rate	I		±0.8		LSB
No Missing Codes		I		Guaranteed		
Analog Input						
Input Voltage Range		VI		±2.0		V
Input Bias Current		VI		30	60	µA
Input Resistance	V_{IN}=0 V	VI	100	300		kΩ
Input Capacitance		V		5		pF
Input Bandwidth	3 dB Small Signal	V		120		MHz
+FS Error		V		±5.0		LSB
-FS Error		V		±5.0		LSB
Reference Input						
Reference Ladder Resistance		VI	600	900		Ω
Reference Ladder Tempco		V		0.8		Ω/°C
Timing Characteristics						
Maximum Conversion Rate		VI	10			MHz
Overvoltage Recovery Time		V		20		ns
Pipeline Delay (Latency)		VI			1	Clock Cycle
Output Delay	T_A=+25 °C	V		14	18	ns
Aperture Delay Time	T_A=+25 °C	V		1		ns
Aperture Jitter Time	T_A=+25 °C	V		5		ps-RMS
Dynamic Performance						
Effective Number of Bits						
fin=500 kHz				10.2		Bits
fin=1.0 MHz				10.0		Bits
fin=3.58 MHz				9.5		Bits
Signal-To-Noise Ratio (without Harmonics)						
fin=500 kHz	+25 °C	I	64	67		dB
	T_{MIN} to T_{MAX}	IV	58	61		dB
fin=1 MHz	+25 °C	I	64	66		dB
	T_{MIN} to T_{MAX}	IV	58	60		dB
fin=3.58 MHz	+25 °C	I	62	64		dB
	T_{MIN} to T_{MAX}	IV	58	60		dB

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ELECTRICAL SPECIFICATIONS

T_A=T_{MIN} to T_{MAX}, V_{CC}=+5.0 V, V_{EE}=-5.2 V, DV_{CC}=+5.0 V, V_{IN}=±2.0 V, V_{SB}=-2.0 V, V_{ST}=+2.0 V, f_{clock}=10 MHz, 50% clock duty cycle, unless otherwise specified.

PARAMETERS	TEST CONDITIONS	TEST LEVEL	SPT7920 MIN	SPT7920 TYP	SPT7920 MAX	UNITS
Dynamic Performance						
Harmonic Distortion[2]						
fin=500 kHz	+25 °C	I	63	66		dB
	T_{MIN} to T_{MAX}	IV	59	62		dB
fin=1.0 MHz	+25 °C	I	63	65		dB
	T_{MIN} to T_{MAX}	IV	59	61		dB
fin=3.58 MHz	+25 °C	I	59	61		dB
	T_{MIN} to T_{MAX}	IV	57	59		dB
Signal-to-Noise and Distortion						
fin=500 kHz	+25 °C	IV	60	63		dB
	T_{MIN} to T_{MAX}	IV	55	58		dB
fin=1.0 MHz	+25 °C	IV	60	62		dB
	T_{MIN} to T_{MAX}	IV	55	57		dB
fin=3.58 MHz	+25 °C	IV	57	59		dB
	T_{MIN} to T_{MAX}	IV	54	56		dB
Spurious Free Dynamic Range[3]	+25 °C	V		74		dB
Differential Phase[4]	+25 °C	V		0.2		Degree
Differential Gain[4]	+25 °C	V		0.7		%
Digital Inputs						
Logic "1" Voltage		V	2.4		4.5	V
Logic "0" Voltage		V			0.8	V
Maximum Input Current Low		IV	0	+5	+20	µA
Maximum Input Current High		IV	0	+5	+20	µA
Pulse Width Low (CLK)		IV	30			ns
Pulse Width High (CLK)		IV	30		300	ns
Digital Outputs						
Logic "1" Voltage		IV	2.4			V
Logic "0" Voltage		IV			0.6	V
Power Supply Requirements						
Voltages V_{CC}		IV	4.75	5.0	5.25	V
DV_{CC}		IV	4.75	5.0	5.25	V
$-V_{EE}$		IV	-4.95	-5.2	-5.45	V
Currents I_{CC}		IV		135	150	mA
DI_{CC}		IV		40	55	mA
$-I_{EE}$		IV		45	70	mA
Power Dissipation		VI		1.1	1.3	W
Power Supply Rejection	(5 V ±0.25 V, -5.2 ±0.25 V)	V		1.0		LSB

[1] Typical thermal impedances (unsoldered, in free air): 32L sidebrazed DIP. θ_{ja} = 50 °C/W.
[2] 64 distortion BINS from 4096 pt FFT.
[3] fin = 1 MHz.
[4] fin = 3.58 and 4.35 MHz.

Figure 1A: Timing Diagram

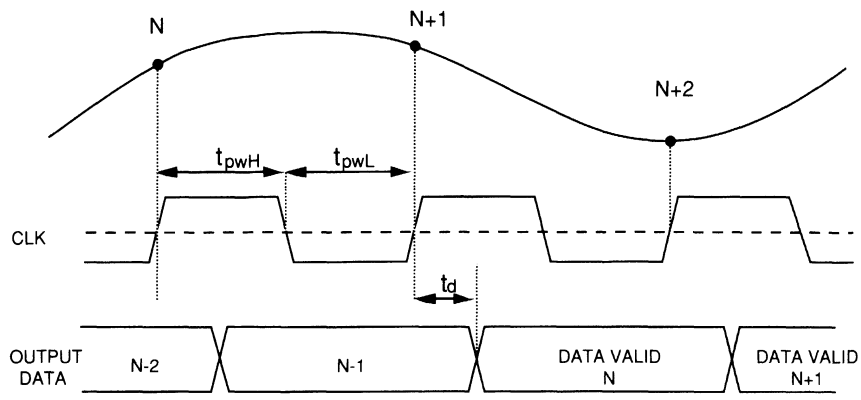

Figure 1B: Single Event Clock

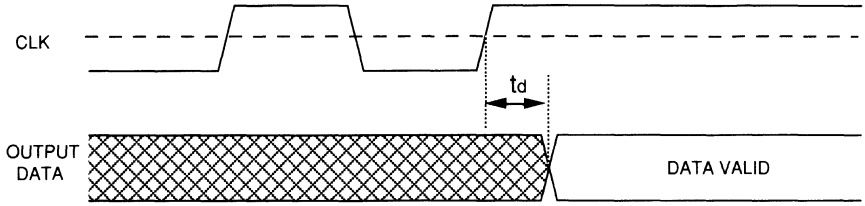

Table 1 - Timing Parameters

PARAMETERS	DESCRIPTION	MIN	TYP	MAX	UNITS
t_d	CLK to Data Valid Prop Delay	-	14	18	ns
t_{pwH}	CLK High Pulse Width	30	-	300	ns
t_{pwL}	CLK Low Pulse Width	30	-	-	ns

TEST LEVEL CODES

All electrical characteristics are subject to the following conditions:

All parameters having min/max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality Assurance inspection. Any blank section in the data column indicates that the specification is not tested at the specified condition.

Unless otherwise noted, all tests are pulsed tests; therefore, $T_J = T_C = T_A$.

TEST LEVEL	TEST PROCEDURE
I	100% production tested at the specified temperature.
II	100% production tested at T_A=25 °C, and sample tested at the specified temperatures.
III	QA sample tested only at the specified temperatures.
IV	Parameter is guaranteed (but not tested) by design and characterization data.
V	Parameter is a typical value for information purposes only.
VI	100% production tested at T_A = 25 °C. Parameter is guaranteed over specified temperature range.

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SPECIFICATION DEFINITIONS

APERTURE DELAY

Aperture delay represents the point in time, relative to the rising edge of the CLOCK input, that the analog input is sampled.

APERTURE JITTER

The variations in aperture delay for successive samples.

DIFFERENTIAL GAIN (DG)

A signal consisting of a sine wave superimposed on various DC levels is applied to the input. Differential gain is the maximum variation in the sampled sine wave amplitudes at these DC levels.

DIFFERENTIAL PHASE (DP)

A signal consisting of a sine wave superimposed on various DC levels that is applied to the input. Differential phase is the maximum variation in the sampled sine wave phases at these DC levels.

EFFECTIVE NUMBER OF BITS (ENOB)

SINAD = 6.02N + 1.76, where N is equal to the effective number of bits.

$$N = \frac{SINAD - 1.76}{6.02}$$

+/- FULL-SCALE ERROR (GAIN ERROR)

Difference between measured full scale response [(+Fs) - (-Fs)] and the theoretical response (+4 V -2 LSBs) where the +FS (full scale) input voltage is defined as the output transition between 1-10 and 1-11 and the -FS input voltage is defined as the output transition between 0-00 and 0-01.

INPUT BANDWIDTH

Small signal (50 mV) bandwidth (3 dB) of analog input stage.

DIFFERENTIAL NONLINEARITY (DNL)

Error in the width of each code from its theoretical value. (Theoretical = $V_{FS}/2^N$)

INTEGRAL NONLINEARITY (INL)

Linearity error refers to the deviation of each individual code (normalized) from a straight line drawn from -Fs through +Fs. The deviation is measured from the edge of each particular code to the true straight line.

OUTPUT DELAY

Time between the clock's triggering edge and output data valid.

OVERVOLTAGE RECOVERY TIME

The time required for the ADC to recover to full accuracy after an analog input signal 125% of full scale is reduced to 50% of the full-scale value.

SIGNAL-TO-NOISE RATIO (SNR)

The ratio of the fundamental sinusoid power to the total noise power. Harmonics are excluded.

SIGNAL-TO-NOISE AND DISTORTION (SINAD)

The ratio of the fundamental sinusoid power to the total noise and distortion power.

TOTAL HARMONIC DISTORTION (THD)

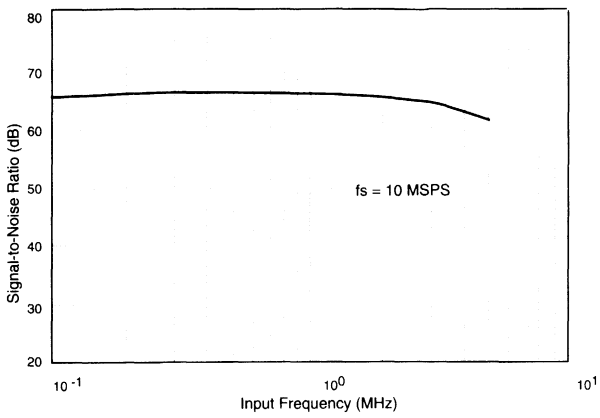
The ratio of the total power of the first 64 harmonics to the power of the measured sinusoidal signal.

SPURIOUS FREE DYNAMIC RANGE (SFDR)

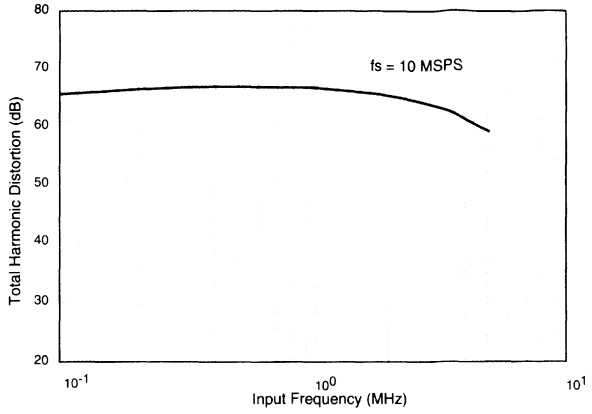
The ratio of the fundamental sinusoidal amplitude to the single largest harmonic or spurious signal.

PERFORMANCE CHARACTERISTICS

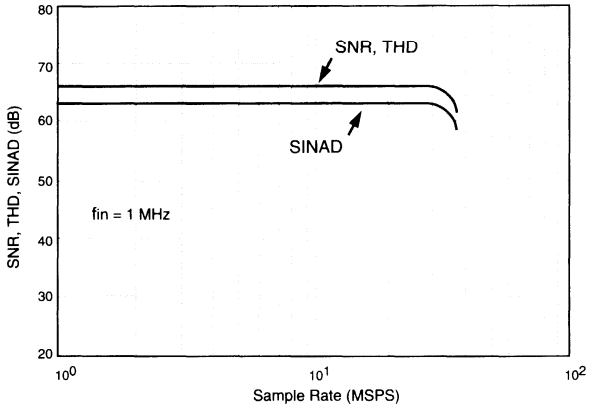
SNR vs Input Frequency



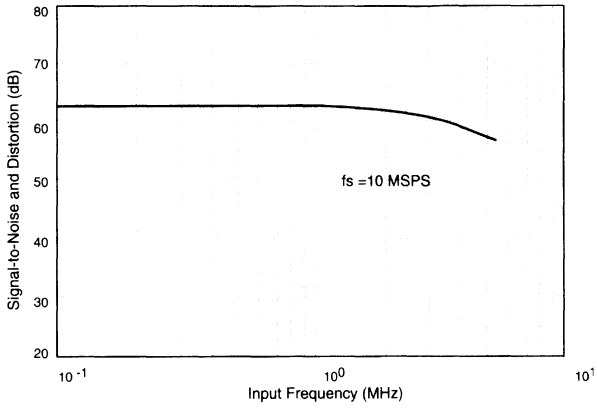
THD vs Input Frequency



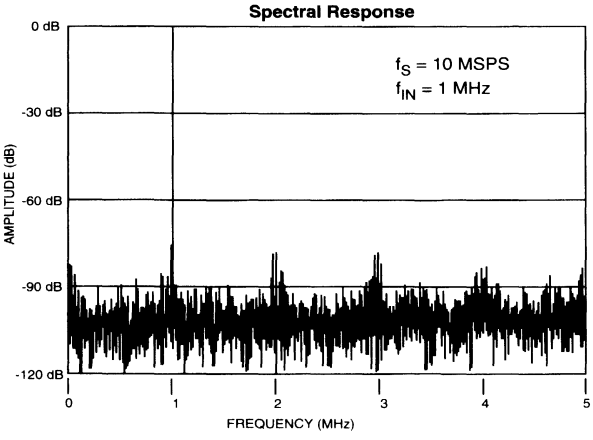
SNR, THD, SINAD vs Sample Rate



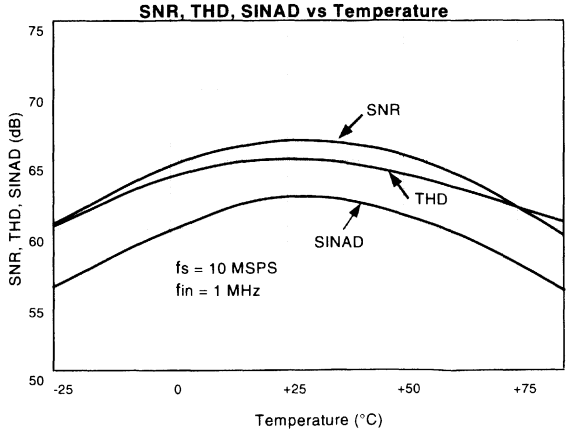
SINAD vs Input Frequency



SPT7920
Spectral Response



SNR, THD, SINAD vs Temperature



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TYPICAL INTERFACE CIRCUIT

The SPT7920 requires few external components to achieve the stated operation and performance. Figure 2 shows the typical interface requirements when using the SPT7920 in normal circuit operation. The following section provides a description of the pin functions and outlines critical performance criteria to consider for achieving the optimal device performance.

POWER SUPPLIES AND GROUNDING

The SPT7920 requires -5.2 V and +5 V analog supply voltages. The +5 V supply is common to analog VCC and digital DVCC. A ferrite bead in series with each supply line is intended to reduce the transient noise injected into the analog VCC. These beads should be connected as closely as possible to the device. The connection between the beads and the SPT7920 should not be shared with any other device. Each power supply pin should be bypassed as closely as possible to the device. Use 0.1 µF for VEE and VCC, and 0.01 µF for DVCC (chip caps are preferred).

AGND and DGND are the two grounds available on the SPT7920. These two internal grounds are isolated on the device. The use of ground planes is recommended to achieve optimum device performance. DGND is needed for the DVCC return path (40 mA typical) and for the return path for all digital output logic interfaces. AGND and DGND should be separated from each other and connected together only at the device through a ferrite bead.

A Schottky or hot carrier diode connected between AGND and VEE is required. The use of separate power supplies between VCC and DVCC is not recommended due to potential power supply sequencing latch-up conditions. Using the recommended interface circuit shown in figure 2 will provide optimum device performance for the SPT7920.

VOLTAGE REFERENCE

The SPT7920 requires the use of two voltage references: V_{FT} and V_{FB}. V_{FT} is the force for the top of the voltage reference ladder (+2.5 V typ), V_{FB} (-2.5 V typ) is the force for the bottom of the voltage reference ladder. Both voltages are applied across an internal reference ladder resistance of 900 ohms. The +2.5 V voltage source for reference VFT must be current limited to 20 mA maximum if a different driving circuit is used in place of the recommended reference circuit shown in figures 2 and 3. In addition, there are five reference ladder taps (V_{ST}, V_{RT1}, V_{RT2}, V_{RT3}, and V_{SB}). V_{ST} is the sense for the top of the reference ladder (+2.0 V), V_{RT2} is the midpoint of the ladder (0.0 V typ) and V_{SB} is the sense for the bottom of the reference ladder (-2.0 V). V_{RT1} and V_{RT3} are quarter point ladder taps (+1.0 and -1.0 V typical, respectively). The voltages seen at V_{ST} and V_{SB} are the true full scale input voltages of the device when V_{FT} and V_{FB} are driven to the recommended voltages (+2.5 V and -2.5 V typical respectively). V_{ST} and V_{SB} should be used to monitor the actual full scale input voltage of the device. V_{RT1}, V_{RT2} and V_{RT3} should not be driven to the expected ideal values as is commonly done with standard flash converters. When not being used, a decoupling capacitor of .01 uF connected to AGND from each tap is recommended to minimize high frequency noise injection.

Figure 2 - Typical Interface Circuit

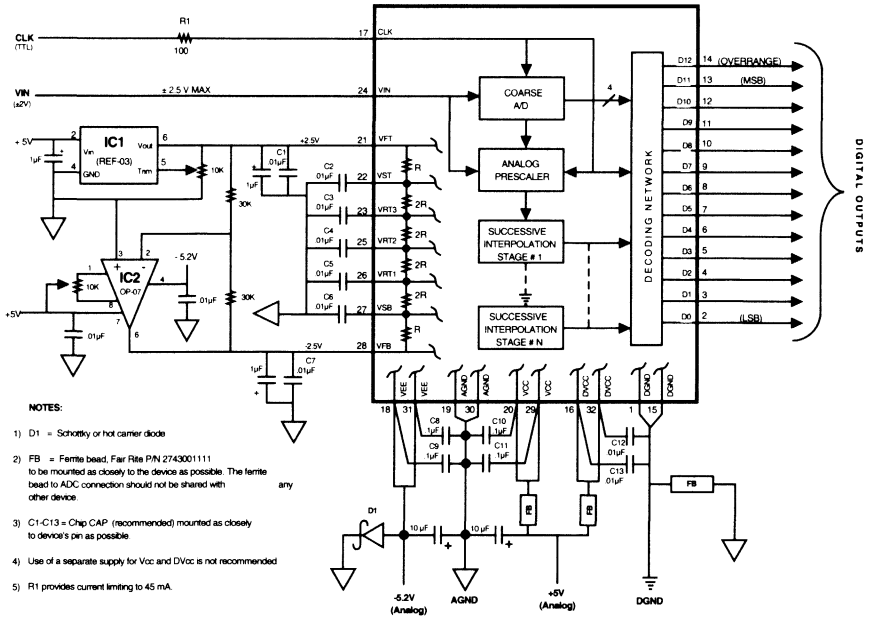
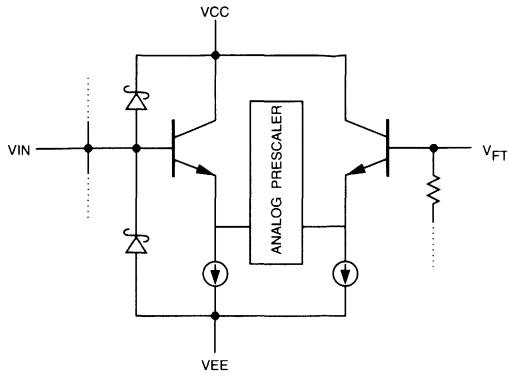


Figure 3 - Analog Equivalent Input Circuit



The analog input range will scale proportionally with respect to the reference voltage if a different input range is required. The maximum scaling factor for device operation is ± 20% of the recommended reference voltages of V_{FT} and V_{FB}. However, because the device is laser trimmed to optimize performance with ± 2.5 V references, the accuracy of the device will degrade if operated beyond a ± 2% range.

An example of a recommended reference driver circuit is shown in figure 2. IC1 is REF-03, the +2.5 V reference with a tolerance of 0.6% or +/- 0.015 V. The potentiometer R1 is 10k ohms and supports a minimum adjustable range of up to 150 mV. IC2 is recommended to be an OP-07 or equivalent device. R2 and R3 must be matched to within 0.1% with good TC tracking to maintain a 0.3 LSB matching between V_{FT} and V_{FB}. If 0.1% matching is not met, then potentiometer R4 can be used to adjust the V_{FB} voltage to the desired level. R1 and R4 should be adjusted such that V_{ST} and V_{SB} are exactly +2.0 V and -2.0 V respectively.

The following errors are defined:
+FS error = top of ladder offset voltage = $\Delta(+FS - V_{ST})$
-FS error = bottom of ladder offset voltage = $\Delta(-FS - V_{SB})$

Where the +FS (full scale) input voltage is defined as the output 1 LSB above the transition of 1—10 and 1—11 and the -FS input voltage is defined as the output 1 LSB below the transition of 0—00 and 0—01.

ANALOG INPUT

V_{IN} is the analog input. The full scale input range will be 80% of the reference voltage or ±2 volts with V_{FB}=-2.5 V and V_{FT}=+2.5 V.

The drive requirements for the analog inputs are minimal when compared to conventional Flash converters due to the SPT7920's extremely low input capacitance of only 5 pF and very high input impedance of 300 kΩ. For example, for an input signal of ± 2 V p-p with an input frequency of 10 MHz, the peak output current required for the driving circuit is only 628 µA.

CLOCK INPUT

The SPT7920 is driven from a single-ended TTL input (CLK). For optimal noise performance, the clock input slew rate should be a minimum of 6 ns. Because of this, the use of *fast* logic is recommended. The clock input duty cycle should be 50% where possible, but performance will not be degraded if kept within the range of 40-60%. However, in any case the clock pulse width (tpwH) must be kept at 300 ns maximum to ensure proper operation of the internal track and hold amplifier (see timing diagram). The analog input signal is latched on the rising edge of the CLK.

The clock input must be driven from fast TTL logic ($V_{IH} \leq 4.5$ V, $T_{RISE} < 6$ ns). In the event the clock is driven from a high current source, use a 100 Ω resistor in series to current limit to approximately 45 mA.

DIGITAL OUTPUTS

The format of the output data (D0-D11) is straight binary. (See table 2.) The outputs are latched on the rising edge of CLK with a propagation delay of 14 ns (typ). There is a one clock cycle latency between CLK and the valid output data. (See timing diagram.)

Table 2 - Output Data Information

ANALOG INPUT	OVERRANGE D12	OUTPUT CODE D11-DO
>+2.0 V + 1/2 LSB	1	1111 1111 1111
+2.0 V -1 LSB	O	1111 1111 111Ø
0.0 V	O	ØØØØ ØØØØ ØØØØ
-2.0 V +1 LSB	O	OOOO OOOO OOOØ
<2.0 V	O	OOOO OOOO OOOO

(Ø indicates the flickering bit between logic 0 and 1).

The rise times and fall times of the digital outputs are not symmetrical. The propagation delay of the rise time is typically 14 ns and the fall time is typically 6 ns. (See figure 4.) The nonsymmetrical rise and fall times create approximately 8 ns of invalid data.

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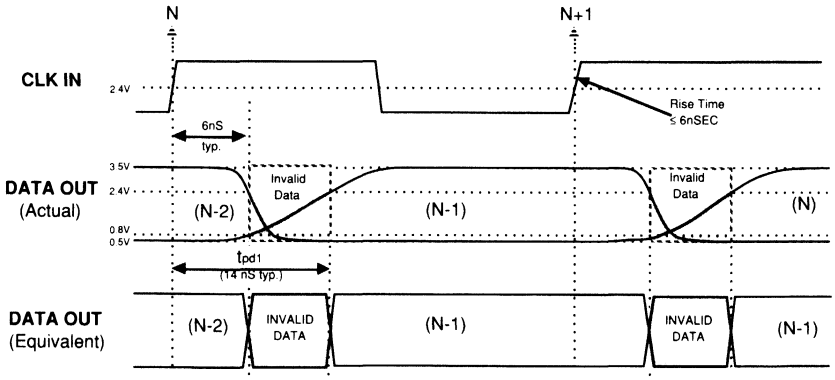
Figure 4 - Digital Output Characteristics



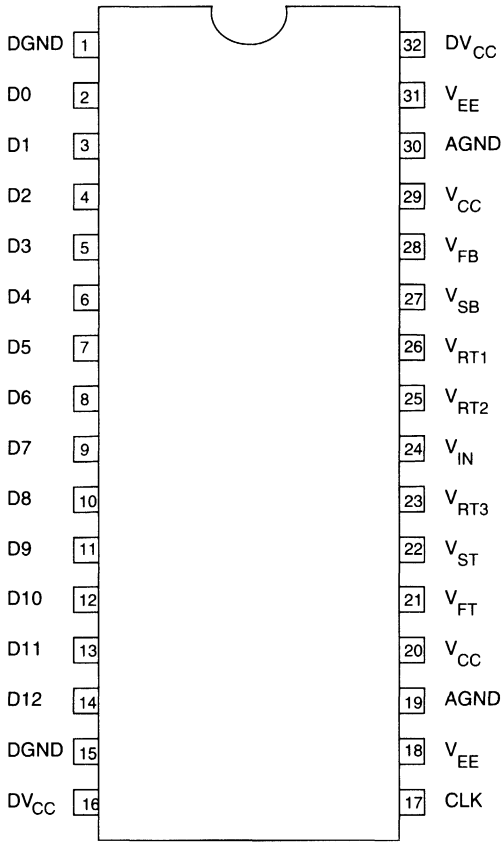
OVERRANGE OUTPUT

The OVERRANGE OUTPUT (D12) is an indication that the analog input signal has exceeded the full scale input voltage by 1 LSB. When this condition occurs, the outputs will switch to logic 1s. All other data outputs are unaffected by this operation. This feature makes it possible to include the SPT7920 into higher resolution systems.

EVALUATION BOARD

The EB7920 Evaluation Board is available to aid designers in demonstrating the full performance of the SPT7920. This board includes a reference circuit, clock driver circuit, output data latches and an on-board reconstruction of the digital data. An application note (AN7920) describing the operation of this board as well as information on the testing of the SPT7920 is also available. Contact the factory for price and availability.

PIN ASSIGNMENT



PIN FUNCTIONS

NAME	FUNCTION
DGND	Digital Ground
AGND	Analog Ground
D0-D11	TTL Outputs (D0=LSB)
D12	TTL Output Overrange
CLK	Clock Input
V_{EE}	-5.2 V Supply
V_{CC}	+5.0 V supply
V_{RT1}-V_{RT3}	Voltage Reference Taps
V_{IN}	Analog Input
DV_{CC}	Digital +5.0 V Supply (TTL Outputs)
V_{FT}	Force for Top of Reference Ladder
V_{ST}	Sense for Top of Reference Ladder
V_{FB}	Force for Bottom of Reference Ladder
V_{SB}	Sense for Bottom of Reference Ladder

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LEADERSHIP IN DATA CONVERSION AND SIGNAL PROCESSING

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SIGNAL PROCESSING TECHNOLOGIES

SPT7922

12-BIT, 30 MSPS, TTL, A/D CONVERTER

FEATURES

- Monolithic
- 12-Bit 30 MSPS Converter
- 64 dB SNR @ 3.58 MHz Input
- On-Chip Track/Hold
- Bipolar ±2.0 V Analog Input
- Low Power (1.1 W Typical)
- 5 pF input Capacitance
- TTL Outputs

APPLICATIONS

- Radar Receivers
- Professional Video
- Instrumentation
- Medical Imaging
- Electronic Warfare
- Digital Communications
- Digital Spectrum Analyzers
- Electro-optics

GENERAL DESCRIPTION

The SPT7922 A/D converter is the industry's first 12-bit monolithic A-to-D converter capable of sample rates of greater than 30 MSPS. On board input buffer and track/hold function assures excellent dynamic performance without the need for external components. Drive requirement problems are minimized with an input capacitance of only 5 pF.

Logic inputs and outputs are TTL. An overrange output signal is provided to indicate overflow conditions. Output data format is straight binary. Power dissipation is very low at only 1.1 watts with power supply voltages of +5.0 and -5.2 volts. The SPT7922 also provides a wide input voltage range of ±2.0 volts.

The SPT7922 is available in a small 32-lead ceramic sidebrazed DIP package. A commercial temperature range of 0 to +70 °C is currently offered. A surface-mount package, die, military temperature, and /883 processed units will be available in the near future. Consult the factory for availability.

BLOCK DIAGRAM

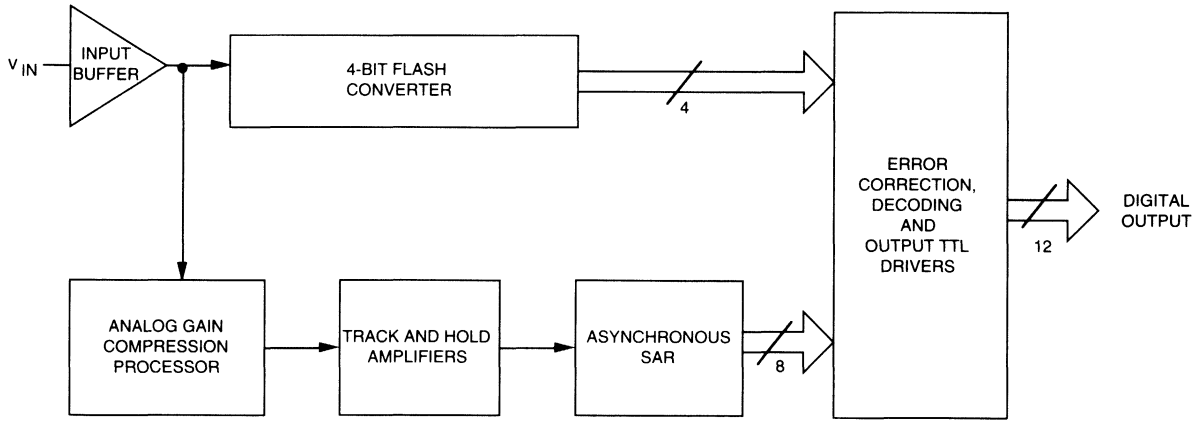

Figure 1A: Timing Diagram

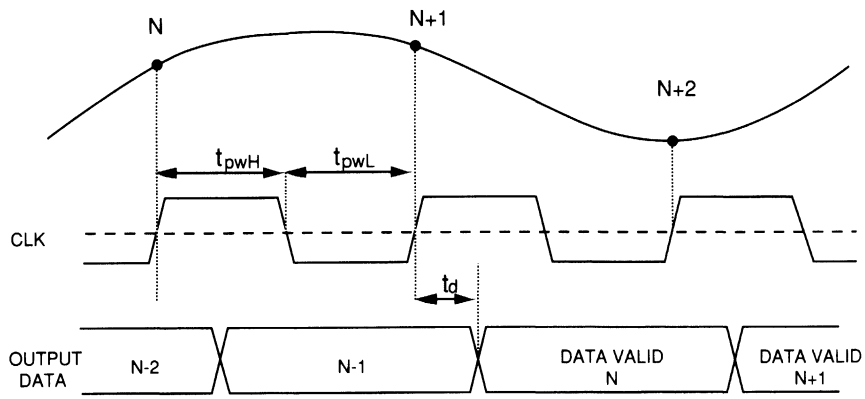

Figure 1B: Single Event Clock

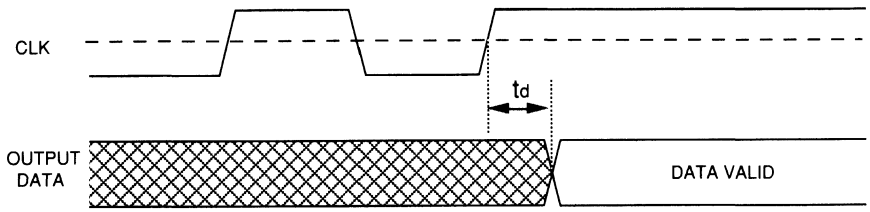

Table 1 - Timing Parameters

PARAMETERS	DESCRIPTION	MIN	TYP	MAX	UNITS
t_d	CLK to Data Valid Prop Delay	-	14	18	ns
t_{pwH}	CLK High Pulse Width	15	-	300	ns
t_{pwL}	CLK Low Pulse Width	15	-	-	ns

TEST LEVEL CODES

All electrical characteristics are subject to the following conditions:

All parameters having min/max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality Assurance inspection. Any blank section in the data column indicates that the specification is not tested at the specified condition.

Unless otherwise noted, all tests are pulsed tests; therefore, $T_J = T_C = T_A$.

TEST LEVEL	TEST PROCEDURE
I	100% production tested at the specified temperature.
II	100% production tested at T_A=25 °C, and sample tested at the specified temperatures.
III	QA sample tested only at the specified temperatures.
IV	Parameter is guaranteed (but not tested) by design and characterization data.
V	Parameter is a typical value for information purposes only.
VI	100% production tested at T_A = 25 °C. Parameter is guaranteed over specified temperature range.

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SPECIFICATION DEFINITIONS

APERTURE DELAY

Aperture delay represents the point in time, relative to the rising edge of the CLOCK input, that the analog input is sampled.

APERTURE JITTER

The variations in aperture delay for successive samples.

DIFFERENTIAL GAIN (DG)

A signal consisting of a sine wave superimposed on various DC levels is applied to the input. Differential gain is the maximum variation in the sampled sine wave amplitudes at these DC levels.

DIFFERENTIAL PHASE (DP)

A signal consisting of a sine wave superimposed on various DC levels that is applied to the input. Differential phase is the maximum variation in the sampled sine wave phases at these DC levels.

EFFECTIVE NUMBER OF BITS (ENOB)

SINAD = 6.02N + 1.76, where N is equal to the effective number of bits.

$$N = \frac{SINAD - 1.76}{6.02}$$

+/- FULL-SCALE ERROR (GAIN ERROR)

Difference between measured full scale response [(+Fs) - (-Fs)] and the theoretical response (+4 V -2 LSBs) where the +FS (full scale) input voltage is defined as the output transition between 1-10 and 1-11 and the -FS input voltage is defined as the output transition between 0-00 and 0-01.

INPUT BANDWIDTH

Small signal (50 mV) bandwidth (3 dB) of analog input stage.

DIFFERENTIAL NONLINEARITY (DNL)

Error in the width of each code from its theoretical value. (Theoretical = $V_{FS}/2^N$)

INTEGRAL NONLINEARITY (INL)

Linearity error refers to the deviation of each individual code (normalized) from a straight line drawn from -Fs through +Fs. The deviation is measured from the edge of each particular code to the true straight line.

OUTPUT DELAY

Time between the clock's triggering edge and output data valid.

OVERVOLTAGE RECOVERY TIME

The time required for the ADC to recover to full accuracy after an analog input signal 125% of full scale is reduced to 50% of the full-scale value.

SIGNAL-TO-NOISE RATIO (SNR)

The ratio of the fundamental sinusoid power to the total noise power. Harmonics are excluded.

SIGNAL-TO-NOISE AND DISTORTION (SINAD)

The ratio of the fundamental sinusoid power to the total noise and distortion power.

TOTAL HARMONIC DISTORTION (THD)

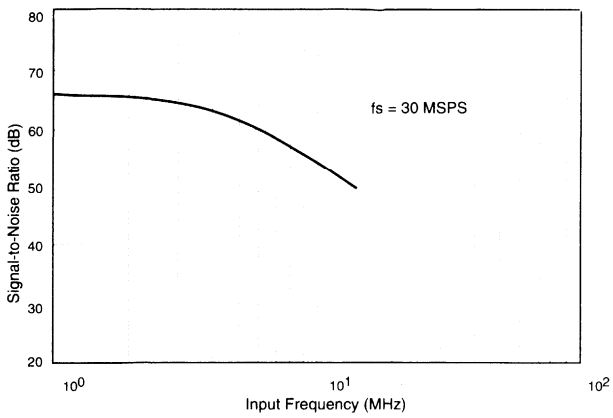
The ratio of the total power of the first 64 harmonics to the power of the measured sinusoidal signal.

SPURIOUS FREE DYNAMIC RANGE (SFDR)

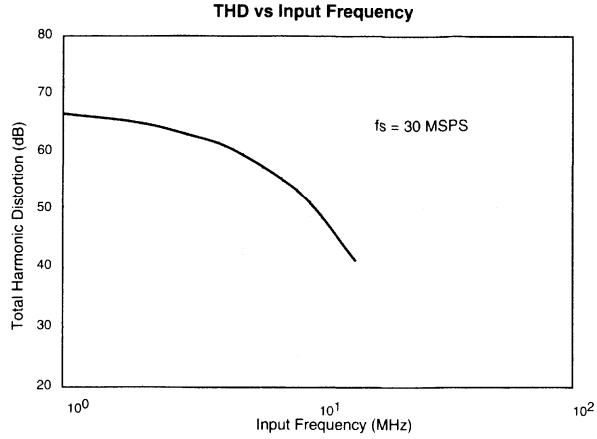
The ratio of the fundamental sinusoidal amplitude to the single largest harmonic or spurious signal.

PERFORMANCE CHARACTERISTICS

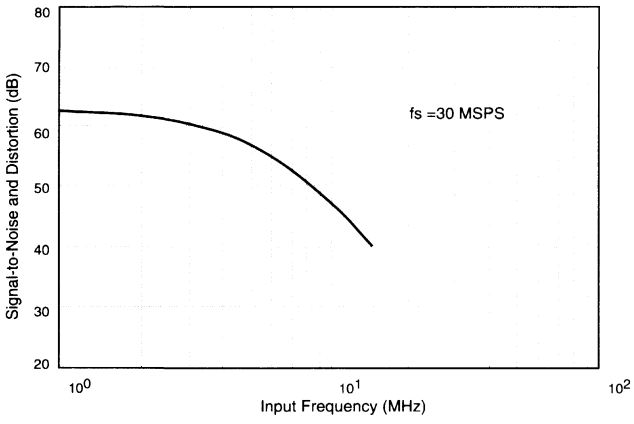
SNR vs Input Frequency



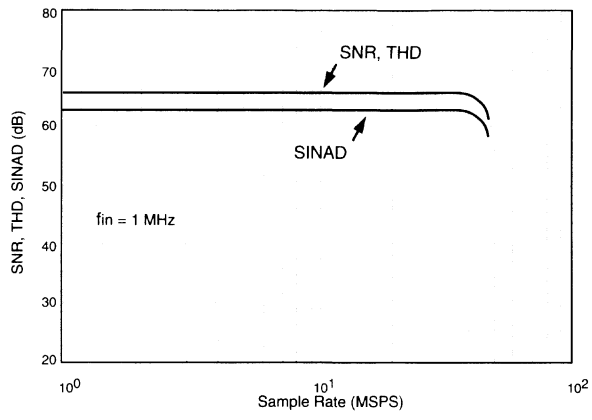
THD vs Input Frequency



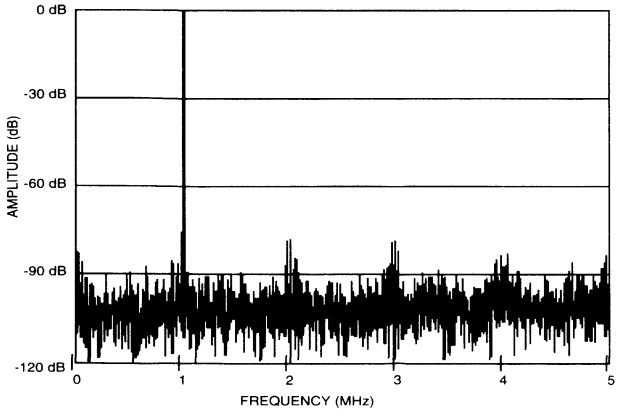
SINAD vs Input Frequency



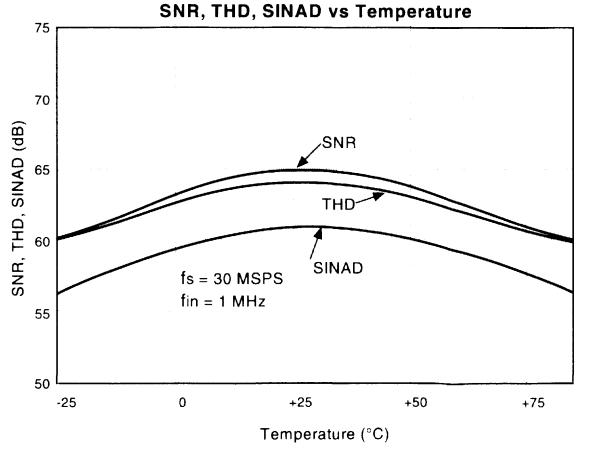
SNR, THD, SINAD vs Sample Rate



SPT7922
Spectral Response



SNR, THD, SINAD vs Temperature



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TYPICAL INTERFACE CIRCUIT

The SPT7922 requires few external components to achieve the stated operation and performance. Figure 2 shows the typical interface requirements when using the SPT7922 in normal circuit operation. The following section provides a description of the pin functions and outlines critical performance criteria to consider for achieving the optimal device performance.

POWER SUPPLIES AND GROUNDING

The SPT7922 requires -5.2 V and +5 V analog supply voltages. The +5 V supply is common to analog VCC and digital DVCC. A ferrite bead in series with each supply line is intended to reduce the transient noise injected into the analog VCC. These beads should be connected as closely as possible to the device. The connection between the beads and the SPT7922 should not be shared with any other device. Each power supply pin should be bypassed as closely as possible to the device. Use 0.1 µF for VEE and VCC, and 0.01 µF for DVCC (chip caps are preferred).

AGND and DGND are the two grounds available on the SPT7922. These two internal grounds are isolated on the device. The use of ground planes is recommended to achieve optimum device performance. DGND is needed for the DVCC return path (40 mA typical) and for the return path for all digital output logic interfaces. AGND and DGND should be separated from each other and connected together only at the device through a ferrite bead.

A Schottky or hot carrier diode connected between AGND and VEE is required. The use of separate power supplies between VCC and DVCC is not recommended due to potential power supply sequencing latch-up conditions. Using the recommended interface circuit shown in figure 2 will provide optimum device performance for the SPT7922.

VOLTAGE REFERENCE

The SPT7922 requires the use of two voltage references: V_{FT} and V_{FB}. V_{FT} is the force for the top of the voltage reference ladder (+2.5 V typ), V_{FB} (-2.5 V typ) is the force for the bottom of the voltage reference ladder. Both voltages are applied across an internal reference ladder resistance of 900 ohms. The +2.5 V voltage source for reference VFT must be current limited to 20 mA maximum if a different driving circuit is used in place of the recommended reference circuit shown in figures 2 and 3. In addition, there are five reference ladder taps (V_{ST}, V_{RT1}, V_{RT2}, V_{RT3}, and V_{SB}). V_{ST} is the sense for the top of the reference ladder (+2.0 V), V_{RT2} is the midpoint of the ladder (0.0 V typ) and V_{SB} is the sense for the bottom of the reference ladder (-2.0 V). V_{RT1} and V_{RT3} are quarter point ladder taps (+1.0 and -1.0 V typical, respectively). The voltages seen at V_{ST} and V_{SB} are the true full scale input voltages of the device when V_{FT} and V_{FB} are driven to the recommended voltages (+2.5 V and -2.5 V typical respectively). V_{ST} and V_{SB} should be used to monitor the actual full scale input voltage of the device. V_{RT1}, V_{RT2} and V_{RT3} should not be driven to the expected ideal values as is commonly done with standard flash converters. When not being used, a decoupling capacitor of .01 uF connected to AGND from each tap is recommended to minimize high frequency noise injection.

Figure 2 - Typical Interface Circuit

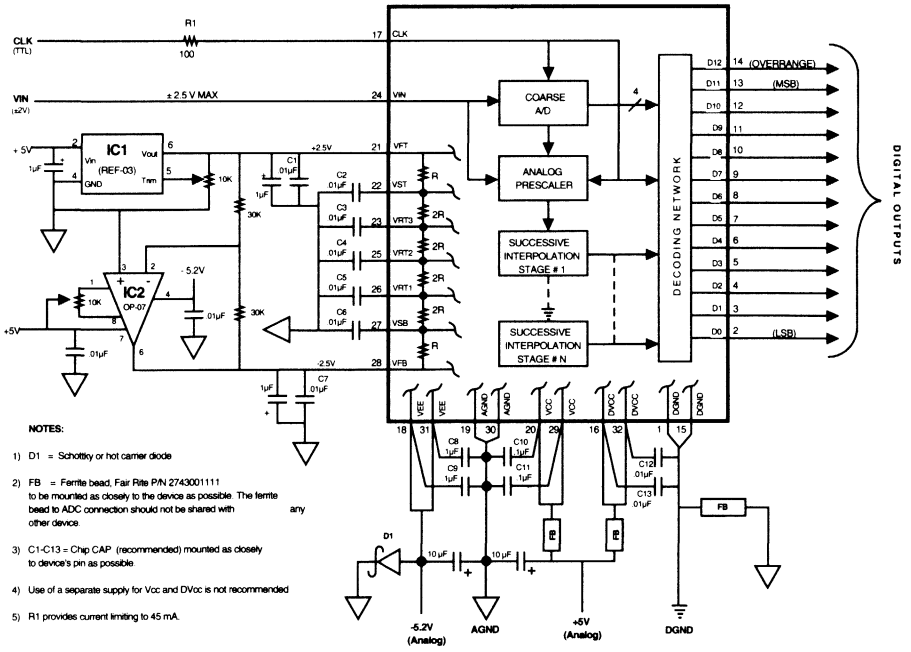
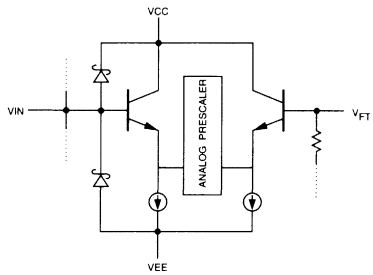


Figure 3 - Analog Equivalent Input Circuit



The analog input range will scale proportionally with respect to the reference voltage if a different input range is required. The maximum scaling factor for device operation is ± 20% of the recommended reference voltages of V_{FT} and V_{FB}. However, because the device is laser trimmed to optimize performance with ± 2.5 V references, the accuracy of the device will degrade if operated beyond a ± 2% range.

An example of a recommended reference driver circuit is shown in figure 2. IC1 is REF-03, the +2.5 V reference with a tolerance of 0.6% or +/- 0.015 V. The potentiometer R1 is 10k ohms and supports a minimum adjustable range of up to 150 mV. IC2 is recommended to be an OP-07 or equivalent device. R2 and R3 must be matched to within 0.1% with good TC tracking to maintain a 0.3 LSB matching between V_{FT} and V_{FB}. If 0.1% matching is not met, then potentiometer R4 can be used to adjust the V_{FB} voltage to the desired level. R1 and R4 should be adjusted such that V_{ST} and V_{SB} are exactly +2.0 V and -2.0V respectively.

The following errors are defined:
+FS error = top of ladder offset voltage = Δ(+FS -V_{ST})
-FS error = bottom of ladder offset voltage = Δ(-FS -V_{SB})

Where the +FS (full scale) input voltage is defined as the output 1 LSB above the transition of 1—10 and 1—11 and the -FS input voltage is defined as the output 1 LSB below the transition of 0—00 and 0—01.

ANALOG INPUT

V_{IN} is the analog input. The full scale input range will be 80% of the reference voltage or ±2 volts with V_{FB}=-2.5 V and V_{FT}=+2.5 V.

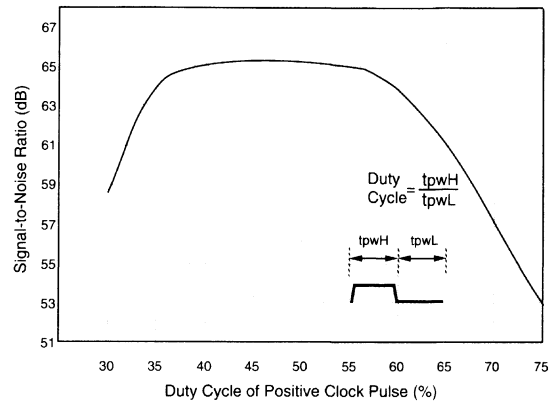
The drive requirements for the analog inputs are minimal when compared to conventional Flash converters due to the SPT7922's extremely low input capacitance of only 5 pF and very high input impedance of 300 kΩ. For example, for an input signal of ± 2 V p-p with an input frequency of 10 MHz, the peak output current required for the driving circuit is only 628 µA.

CLOCK INPUT

The SPT7922 is driven from a single-ended TTL input (CLK). The CLK pulse width (tpwH) must be kept between 15 ns and 300 ns to ensure proper operation of the internal track-and-hold amplifier. (See timing diagram.) When operating the SPT7922 at sampling rates above 3 MSPS, it is recommended that the clock input duty cycle be kept at 50% to optimize performance. (See figure 4.) The analog input signal is latched on the rising edge of the CLK.

The clock input must be driven from fast TTL logic (V_{IH} ≤4.5 V, T_{RISE} <6 ns). In the event the clock is driven from a high current source, use a 100 Ω resistor in series to current limit to approximately 45 mA.

Figure 4 - SNR vs Clock Duty Cycle



DIGITAL OUTPUTS

The format of the output data (D0-D11) is straight binary. (See table 2.) The outputs are latched on the rising edge of CLK with a propagation delay of 14 ns (typ). There is a one clock cycle latency between CLK and the valid output data. (See timing diagram.)

Table 2 - Output Data Information

ANALOG INPUT	OVERRANGE D12	OUTPUT CODE D11-DO
>+2.0 V + 1/2 LSB	1	1111 1111 1111
+2.0 V -1 LSB	O	1111 1111 111Ø
0.0 V	O	ØØØØ ØØØØ ØØØØ
-2.0 V +1 LSB	O	OOOO OOOO OOOØ
<2.0 V	O	OOOO OOOO OOOO

(Ø indicates the flickering bit between logic 0 and 1).

The rise times and fall times of the digital outputs are not symmetrical. The propagation delay of the rise time is typically 14 ns and the fall time is typically 6 ns. (See figure 5.) The nonsymmetrical rise and fall times create approximately 8 ns of invalid data.

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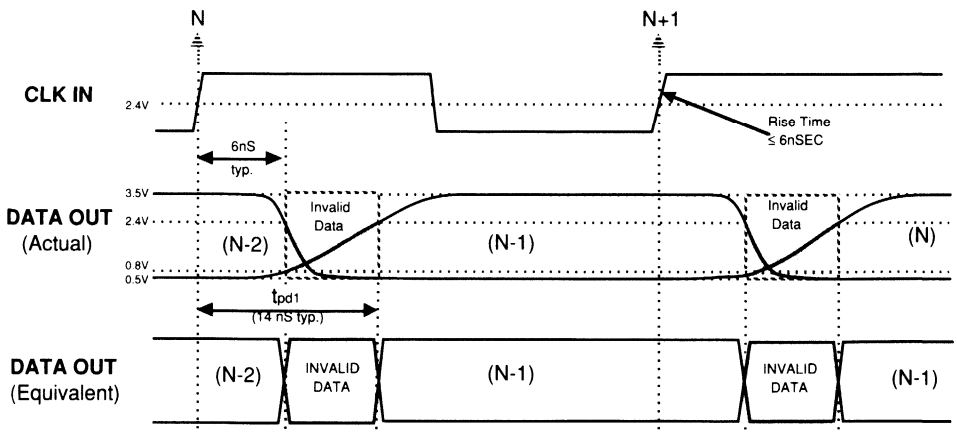
Figure 5 - Digital Output Characteristics



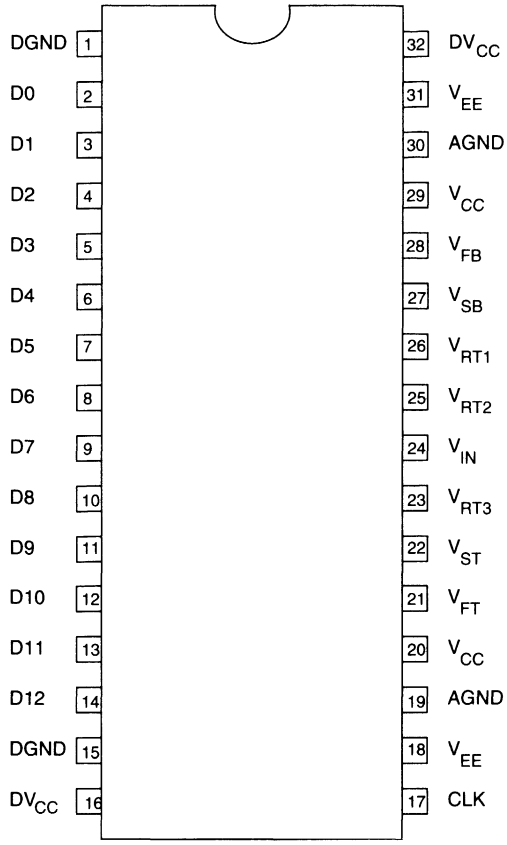
OVERRANGE OUTPUT

The OVERRANGE OUTPUT (D12) is an indication that the analog input signal has exceeded the full scale input voltage by 1 LSB. When this condition occurs, the outputs will switch to logic 1s. All other data outputs are unaffected by this operation. This feature makes it possible to include the SPT7922 into higher resolution systems.

EVALUATION BOARD

The EB7922 Evaluation Board is available to aid designers in demonstrating the full performance of the SPT7922. This board includes a reference circuit, clock driver circuit, output data latches and an on-board reconstruction of the digital data. An application note (AN7922) describing the operation of this board as well as information on the testing of the SPT7922 is also available. Contact the factory for price and availability.

PIN ASSIGNMENT



PIN FUNCTIONS

NAME	FUNCTION
DGND	Digital Ground
AGND	Analog Ground
D0-D11	TTL Outputs (D0=LSB)
D12	TTL Output Overrange
CLK	Clock Input
V_{EE}	-5.2 V Supply
V_{CC}	+5.0 V supply
V_{RT1}-V_{RT3}	Voltage Reference Taps
V_{IN}	Analog Input
DV_{CC}	Digital +5.0 V Supply (TTL Outputs)
V_{FT}	Force for Top of Reference Ladder
V_{ST}	Sense for Top of Reference Ladder
V_{FB}	Force for Bottom of Reference Ladder
V_{SB}	Sense for Bottom of Reference Ladder

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LEADERSHIP IN DATA CONVERSION AND SIGNAL PROCESSING

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SIGNAL PROCESSING TECHNOLOGIES

SPT8100

18-BIT STEREO ADC

ADVANCED INFORMATION

3

FEATURES

- 18-Bit Resolution
- 5th Order Delta-Sigma Modulator
- One Stage FIR Filter
  Passband Ripple: ±0.0005 dB
  Stopband Attenuation: 115 dB
- 64X Oversampling
- Adjustable System Sampling Rates
  Including 32 kHz, 44.1 kHz, and 48 kHz
- 2s Complement Output
- On-Chip Power Down Function
- Single +5 V Supply

APPLICATIONS

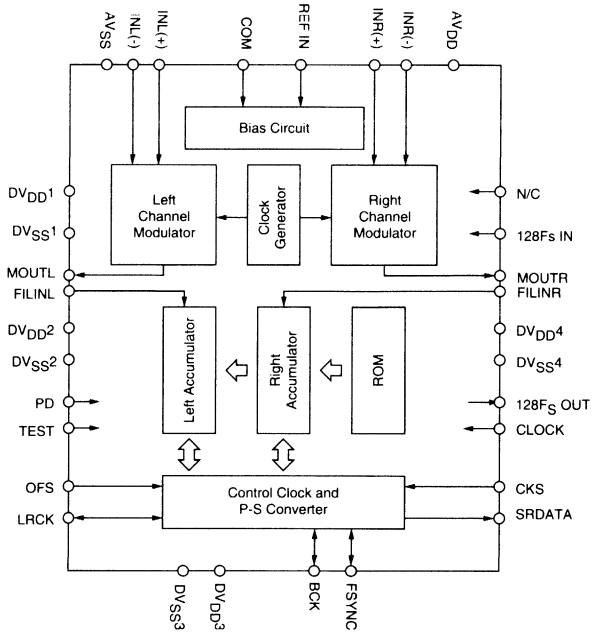
- Professional Audio Digital Tape Recorders
- Digital Audio Editors
- Digital Mixing
- Direct-to-Disc Recorders

GENERAL DESCRIPTION

The SPT8100 is a CMOS, two-channel delta-sigma A/D converter for digital audio applications. It performs a 64X oversampling and has a 5th order modulator for quantization noise reduction. It also eliminates noise outside the baseband by a FIR filter which has ±0.0005 dB passband ripple and 115 dB stopband attenuation characteristics. The digital filter outputs 18-bit resolution by decimating the interpolated signal from the modulator.

The SPT8100 operates from a single +5 V power supply and is available in a 32L plastic DIP package guaranteed over the commercial temperature range of 0 to 70 °C.

BLOCK DIAGRAM

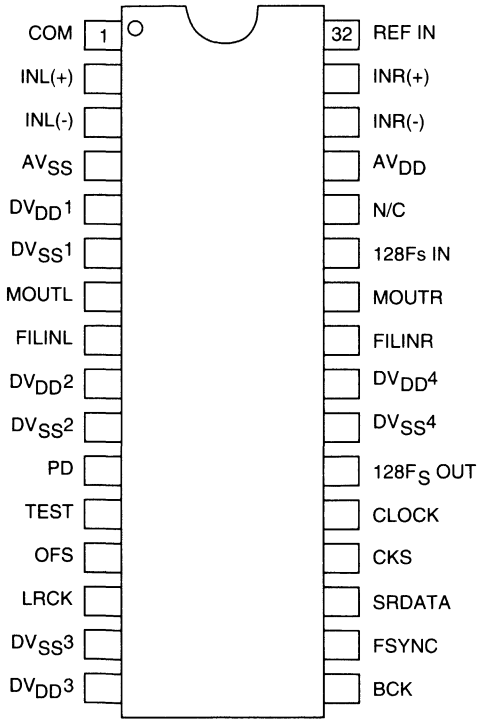


ELECTRICAL SPECIFICATIONS

T_A=25 °C, V_{DD}=5.0 V, V_{SS}=0 V, Clock=12.288 MHz, unless otherwise specified.

PARAMETERS	TEST CONDITIONS	TEST LEVEL	MIN	TYP	MAX	UNITS
Resolution			18			Bits
Dynamic Range				90		dB
Signal-to-Noise				87		dB
Total Harmonic Distortion					.0015	%
Crosstalk				100		dB
Power Supply Current				100		mA
Power Down Current				100		µA

PIN ASSIGNMENTS



PIN FUNCTIONS

COM	Analog Ground
	2.5 V Level from Analog Negative Power Supply
INL(+)	Left Channel Analog Positive Input
INL(-)	Left Channel Analog Negative Input
AV_{SS}	Analog Negative Power Supplies
DV_{DD}1-4	Digital Positive Power Supplies
DV_{SS}1-4	Digital Negative Power Supplies
MOUTL	Test Pin for Left Channel Modulator
	(Open in Normal Position)
FILINL	Test Pin for Left Channel Filter
	(H or L in Normal Position)
PD	Power Down (When High, Power-Down Mode)
TEST	Test Pin (Open in Normal Operation)
OFS	Output Format Select
LRCK	LR Clock
BCK	Bit Clock
FSYNC	Frame Synchronization Clock
SRDATA	Serial Data Output
CKS	Master Clock Select
	(When High: 384 Fs, When low: 256 Fs)
CLOCK	Master Clock
$128F_S$ OUT	128 Fs Clock Output
	(Can Be Connected to 128 Fs IN)
FILINR	Test Pin for Right Channel Filter
	(H or L in Normal Position)
MOUTR	Test Pin for Right Channel Modulator
	(Open in Normal Position)
$128F_S$ IN	128 Fs Clock Input
N/C	No Connect
AV_{DD}	Analog Positive Power Supply
INR(-)	Right Channel Analog Negative Input
INR(+)	Right Channel Analog Positive Input
REF IN	Reference Voltage Input (Should be COM + 1.25 V)

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Section 4 Digital-to-Analog Converters

HDAC7542A	12-Bit, 500 ns, BiCMOS	4-5
HDAC7543A	12-Bit, 500 ns, BiCMOS	4-15
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HDAC52160	16-Bit, 150 ns	4-65
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SPT
SIGNAL PROCESSING TECHNOLOGIES

HDAC7542A

CMOS, 12-BIT MICROPROCESSOR BUFFERED DAC

FEATURES

- Improved Version of the AD7542
- Maximum Gain Error <1/2 LSB (A/G Grade)
- 500 ns Settling Time
- 12-Bit Linearity Over Temperature
- Microprocessor Compatible I/O
- Low Gain Drift (<3 ppm/°C)
- 4-Quadrant Multiplication

APPLICATIONS

- µP Controlled Gain Circuits
- µP Controlled Function Generation
- Bus Structured Instruments
- µP Based Control Systems
- µP Attenuator Control

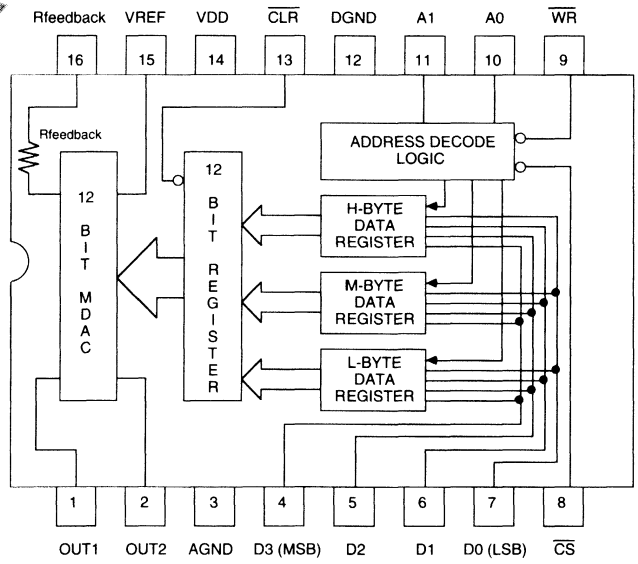
GENERAL DESCRIPTION

The HDAC7542A is a monolithic, low cost, multiplying 12-bit digital-to-analog converter (DAC) designed for direct microprocessor interface. It is compatible with the industry standard 7542 but has significant performance improvements in speed and gain accuracy. The HDAC7542A is fabricated in a three-micron, polysilicon gate CEMOS process and operates from a single +5 V (maximum) supply. Excellent linearity and gain accuracy are achieved through the use of laser-trimmed thin film resistors. Latch-up immunity is ensured by the use of an epi process base. This eliminates the need for external Schottky clamping diodes for latch-up protection.

The data bits for selecting the DAC output are written into the HDAC7542A via a direct connection to the parallel bus of a microprocessor. Data bytes are written as 3, 4-bit groups or nibbles into the data registers on the chip. This input bits are double buffered on chip. Updating the analog output is controlled via the paralled bus by writing to the chip. A clear pin ($\overline{CLR}$) allows for resetting the output to all zeros under power-up or system reset conditions. All address decoding for writing to the chip registers is handled on the chip.

The HDAC7542's direct parallel bus interconnect makes it an excellent choice for microprocessor-based instruments and industrial or process controllers utilizing microprocessors.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Beyond which damage may occur)[1] 25 °C

Supply Voltages
V_{DD} to GND ..... +7 V
AGND to GND ..... -0.3 to V_{DD}
Input Voltages
$V_{Rfeedback}$ to GND ..... ±25 V
Digital Input Voltage to GND ..... 0.3 to V_{DD}
Outputs
V_{OUT1} or V_{OUT2} to GND ..... -0.3 V to V_{DD}

Temperature
Operating Temperature, ambient ..... -55 to +125 °C
junction ..... +150 °C
Lead Temperature, (soldering 10 seconds) ..... +300 °C
Storage Temperature ..... -65 to +150 °C
Power Dissipation (Any Package) to +75 °C 450mW
(Derates above +75 °C by 6 mW/°C)

Note 1: Operation at any Absolute Maximum Rating is not implied. See Operating Conditions for proper nominal appliied conditions in typical applications.

ELECTRICAL SPECIFICATIONS

$T_A=T_{MIN}$ to T_{MAX}, V_{DD}=+5 V; V_{REF}=+10 V, OUT1=OUT2=0 V, AGND=DGND, unless otherwise specified.

TEST PARAMETERS	TEST CONDITIONS	TEST LEVEL	HDAC7542AA/G MIN	HDAC7542AA/G NOM	HDAC7542AA/G MAX	HDAC7542AA MIN	HDAC7542AA NOM	HDAC7542AA MAX	HDAC7542AB MIN	HDAC7542AB NOM	HDAC7542AB MAX	UNITS
DC ELECTRICAL CHARACTERISTICS												
Resolution		I		12			12			12		Bits
Relative Accuracy		I	-.5	±.25	+.5	-.5		+.5	-1		+1	LSB
Differential Nonlinearity	Guaranteed 12-Bit Monotonic	I	-1		+1	-1		+1	-1		+1	LSB
Gain Error	25 °C	I	-.5		+.5	-2		+2	-3		+3	LSB
Using Internal $R_{feedback}$	Tmin - Tmax	I	-1.5		+1.5	-3		+3	-4		+4	LSB
Gain Temperature Coefficient		IV		0.3	3		0.3	3		0.3	3	ppm/°C
Output Leakage OUT1[4] and OUT2	25 °C	I	-1		+1	-1		+1	-1		+1	nA
	0-70 °C/-25 to +85 °C	I	-10		+10	-10		+10	-10		+10	nA
	-55 to +125 °C	I	-50		+50	-50		+50	-50		+50	nA
	All Digital Inputs at 0 V											
Reference Input Resistance	Pin 19 to GND											
	+25 °C	IV	7	12.5	18	7	12.5	18	7	12.5	18	kΩ
	Temp. Coefficient	IV		-180			-180			-180		ppm/°C
DIGITAL INPUTS												
V_{IH} (High Input Voltage)		I	2.0			2.0			2.0			V
V_{IL} (Low Input Voltage)		I			0.8			0.8			0.8	V
I_{IN} (Input Currents I_{IH}, I_{IL})		I			±1			±1			±1	µA
C_{IN} (Input Capacitance)	VIN=0 Volts	IV			5			5			5	pF

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ELECTRICAL SPECIFICATIONS

$T_A=T_{MIN}$ to T_{MAX}, V_{DD}=+5 V; V_{REF}=+10 V, OUT1=0 V, AGND=DGND, unless otherwise specified.

TEST PARAMETERS	TEST CONDITIONS	TEST LEVEL	HDAC7542AA/G MIN	HDAC7542AA/G NOM	HDAC7542AA/G MAX	HDAC7542AA MIN	HDAC7542AA NOM	HDAC7542AA MAX	HDAC7542AB MIN	HDAC7542AB NOM	HDAC7542AB MAX	UNITS
I_{DD}	Logic Inputs at V_{IL} or V_{IH}	I			2.5			2.5			2.5	mA
AC ELECTRICAL CHARACTERISTICS												
Multiplying Feedthrough Error	V_{REF} to V_{OUT} V_{REF}=±10 V 10 kHz Sinewave	IV		0.3	0.5		0.3	0.5		0.3	0.5	mV(p-p)
Output Current Settling Time[1,3]		IV		0.5	1.0		0.5	1.0		0.5	1.0	µsec
Capacitance OUT1,2	Digital Inputs=V_{IH}	IV			75			75			75	pF
Capacitance OUT1,2	Digital Inputs=V_{IL}	IV			30			30			30	pF
SWITCHING CHARACTRISTICS												
t_{WR} (WRITE Pulse Width)		I	40			40			40			nsec
t_{AWH} (Address-to-WRITE hold time)		I	0			0			0			nsec
t_{CWH} (Chip select-to-WRITE hold Time)		I	0			0			0			nsec
t_{CLR} (Clear pulse Width)		I	40			40			40			nsec
INPUT BYTE REGISTER LOADING												
t_{CWS} (Chip select-to-WRITE Setup Time)		I	0			0			0			nsec
t_{AWS} (Address Valid-to-WRITE Setup Time)		I	40			40			40			nsec
t_{DS} (Data Setup Time)		I	20			20			20			nsec
t_{DH} (Data Hold Time)		I	20			20			20			nsec
INTERNAL DAC REGISTER LOADING												
t_{CWS} (Chip Select-to-WRITE Setup Time)		I	0			0			0			nsec
t_{AWS} (Address Valid-to-WRITE Setup Time)		I	40			40			40			nsec

Note 1: OUT1 load: 100 Ω + 13 pF

Note 2: Digital inputs change from 0 V to V_{DD} or V_{DD} to 0 V

Note 3: Measured from falling edge of $\overline{WR}$.

Note 4: Digital inputs $\overline{WR}$ and $\overline{CS}$ at 0 V.

TEST LEVEL CODES

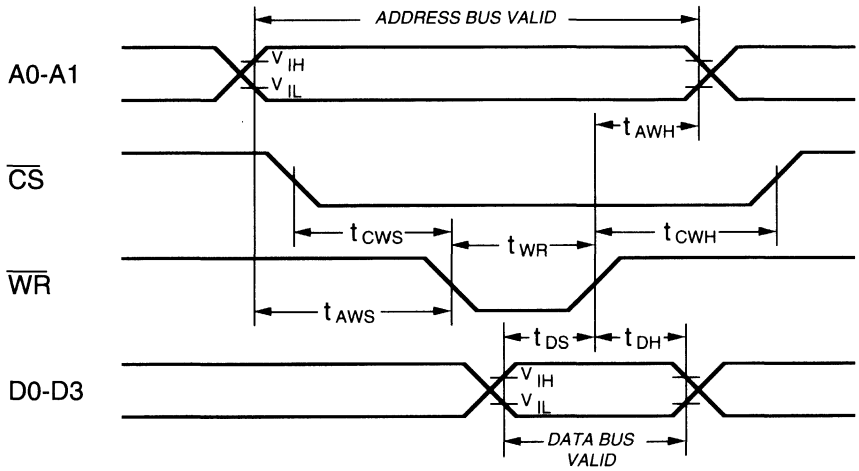
All electrical characteristics are subject to the following conditions:

All parameters having min/max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality Assurance inspection. Any blank section in the data column indicates that the specification is not tested at the specified condition.

Unless otherwise noted, all tests are pulsed tests; therefore, $T_J = T_C = T_A$.

TEST LEVEL	TEST PROCEDURE
I	100% production tested at the specified temperature.
II	100% production tested at T_A=25 °C, and sample tested at the specified temperatures.
III	QA sample tested only at the specified temperatures.
IV	Parameter is guaranteed (but not tested) by design and characterization data.
V	Parameter is a typical value for information purposes only.
VI	100% production tested at T_A = 25 °C. Parameter is guaranteed over specified temperature range.

Figure 1 - Write Cycle Timing Diagram



TERMINOLOGY

RELATIVE ACCURACY

Relative accuracy or endpoint nonlinearity is a measure of the maximum deviation from a straight line passing through the endpoints of the DAC transfer function. It is measured after adjusting for zero and full scale and is expressed in percentage of full scale range or (sub)multiples of 1 LSB.

DIFFERENTIAL NONLINEARITY

Differential nonlinearity is the difference between the measured change and the ideal 1 LSB change between any two adjacent codes. A specified differential nonlinearity of 1 LSB (max) over the operating temperature range ensures monotonicity.

GAIN ERROR

Gain error or full-scale error is a measure of the output error between an ideal DAC and the actual device output. For the HDAC7542A ideal full-scale output is -(4095)/(4096)•(V_{REF}). Gain error is adjustable to zero using external trims as shown in figures 6 and 7, and Table II.

OUTPUT LEAKAGE CURRENT

Current which appears at OUT1 with the DAC loaded to all 0s, or OUT2 with the DAC loaded to all 1s.

MULTIPLYING FEEDTHROUGH ERROR

AC error due to capacitive feedthrough from the V_{REF} terminal to OUT1 with the DAC loaded to all 0s.

OUTPUT CURRENT SETTLING TIME

Time required for the output of the DAC to settle to within 1/2 LSB for a given digital input stimulus, i.e., 0 to Full Scale.

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CIRCUIT DESCRIPTION

As shown in the block diagram, the HDAC7542A consists of a 12 bit multiplying DAC and data input logic. The data input logic consists of three 4-bit input data registers (H, M and L-Byte) and a 12-bit DAC register. The DAC register is loaded from the three input registers. Content of the DAC register controls the DAC's analog output level. Data entry is further described in the Interface Logic section.

Figure 2A shows a simplified version of the 12-bit multiplying DAC circuitry. Note that the HDAC7542A uses a modified R-2R ladder technique that provides for superior linearity over similar devices which use the basic R-2R ladder.

A basic R-2R ladder portion is used within the HDAC7542A for the nine least-significant bits (bits 0-8). This ladder portion successively divides the remaining VREF input to produce a binary weighted nine-stage current division. In other words, in moving from left to right, each 2R resistor leg has half the current flow of the previous leg. Double-pole switches within each leg are controlled by the respective input data bit. The switches route the bit-weighted current of the leg to either analog ground (pin OUT2) or to the output (pin OUT1). OUT1 is a virtual ground by means of the external active circuitry. Hence, with every switch in either position, the R-2R ladder resistive integrity is maintained. Input resistance of pin VREF is kept constant.

Modification of the basic R-2R ladder structure occurs in the three most-significant bits. Here, the switches of seven equally weighted current dividers are controlled by bits 9-11 via a logic decoder. Although more complex, this method provides increased accuracy. Application of the HDAC7542A is identical to similar devices that use an un-modified R-2R ladder network.

The DAC output current is converted to a voltage by the feedback resistance composed of the external resistor shown in Figure 2A in series with internal resistor $R_{feedback}$. The operational amplifier provides a buffered VOUT, and in combination with the feedback resistance maintains OUT1 at virtual ground. The transfer function of Figure 2B shows the relationship of VOUT for an equivalent R-2R resistor network, shown in the same figure. A more detailed explanation of the circuit operation and performance aspects is found in the following Equivalent Circuit Analysis section.

Figure 2A - Simplified Circuit Desription

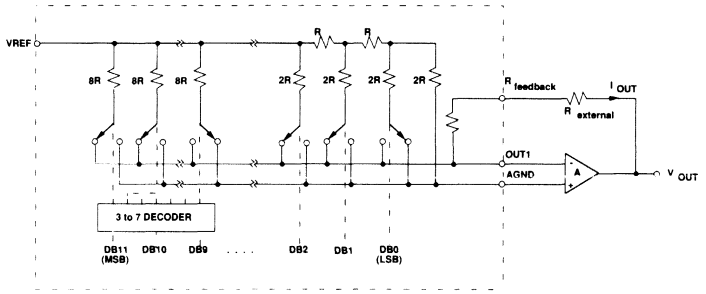
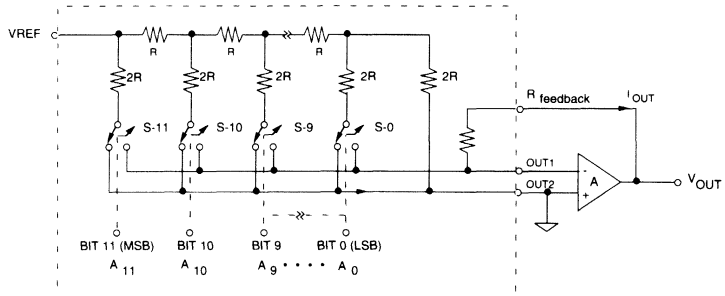


Figure 2B - Equivalent R-2R Resistor Network



The transfer function for the HDAC7542A connected in the multiplying mode as shown in Figure 2B is:

$$V_{OUT} = -V_{REF} \times \left(\frac{A_{11}}{2^1} + \frac{A_{10}}{2^2} + \bullet \bullet \bullet + \frac{A_0}{2^{12}} \right)$$ in which A_x assumes a value of 1 for a HIGH bit and 0 for a Low bit.

EQUIVALENT CIRCUIT ANALYSIS

The equivalent output circuit of the HDAC7542A is the key to understanding offset, linearity and settling time. Figures 3 and 4 illustrate these effects. In Figure 3, the equivalent unipolar operation is illustrated with an external op-amp and all switches LOW to route all current to OUT2. OUT2 is internally connected to AGND in packaged versions of the HDAC7542A. The current from OUT2 is composed of (4095/4096)-th's of the input current at pin V_{REF} plus parasitic leakage currents of the switches. These leakage currents are due to both junction and surface leakage on the MOS switches. 1/4096-th of the input current passes to the ground through the ladder terminal 2R resistor. OUT1 DC current is due only to switch leakage.

Figure 4 shows the same equivalent circuit when all switches are HIGH thereby routing all current to OUT1. The conditions are symmetrical in this case to figure 3.

The main effect of switch leakages in either case is an offset voltage from the DAC when used in voltage output mode as shown in figures 3 and 4.

Figure 3 - HDAC7542A DAC Equivalent Circuit All Digital Inputs Low

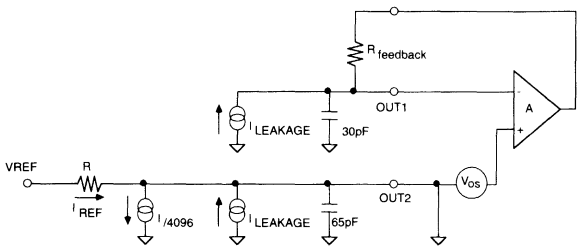
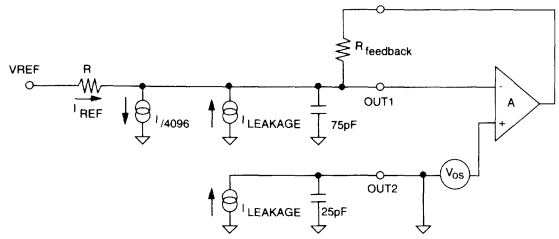


Figure 4 - HDAC7542A DAC Equivalent Circuit All Digital Inputs High



The output resistance seen at the input terminals of the op-amp varies with the code chosen. Between figures 3 and 4, resistance at each op-amp input can change from 10k Ohms to an open for extremes in code. This causes the gain of the offsets (due to either leakage currents of the DAC or op-amp offset) to be code dependent. For example, the gain of offsets of the op-amp under these extreme cases is given below:

Offset gain=1 + $R_{feedback}$/RDAC

With all code bits LOW:
RDAC >> $R_{feedback}$; offset gain=1

With all code bits HIGH:
RDAC= $R_{feedback}$; offset gain=2

Thus, the offset is not amplified by a constant gain over the range of code input. This variation in offset gain is seen as a nonlinearity in the voltage output over the full scale output. The magnitude of nonlinearity is the difference in the gains at code extremes times the offset voltage. In this DAC, this nonlinearity is equal to the offset itself. Thus, the total offset voltage of the op-amp plus leakage induced offset of the DAC and op-amp must be kept to less than 1 LSB to prevent degradation to the DAC linearity performance.

The dynamic output impedance of OUT1 and OUT2 is composed of the DAC switch capacitances to ground. OUT2 has the capacitance of the OFF switches while OUT1 has switch capacitance for ON switches.

The capacitance on OUT1 creates a feedback pole in the voltage output operation mode (figures 3 and 4). Instability of the output amplifier can occur due to the presence of this pole. This pole's instability effect is typically compensated by the use of a feedback capacitor - C1 (figures 6 and 7). Although all R-2R DAC's have the need for this type of compensation, the HDAC7542A maintains faster settling times when used in the voltage output mode. This is due to the lower output capacitance of the HDAC7542A.

The choice of compensation capacitor is bounded by three limits:

- C1 along with $R_{feedback}$ determines the settling time of the output voltage from the op-amp; therefore C1 should be as small as possible for minimum settling time.
- The pole defined by C1 and $R_{feedback}$ should be smaller than secondary poles in the op-amp: as a rule of thumb, about one half of the op-amp's gain-bandwidth.
- Settling time is proportional to $\sqrt{C_{OUT\,1} + C1}$.

For an OP-27 used as an output op-amp with 8 MHz gain-bandwidth, the choice of C1 is:

$(2 \bullet \pi \bullet C1 \bullet R_{feedback})^{-1}$= 4 MHz or C1= 3 pf

$\bullet R_{feedback}$ = 12.5 kΩ

Fast settling time with small amounts of ringing are obtained when the small values of C1 (given by the criteria above) are as close as possible to the DAC output capacitance. The HDAC7542A 's low output capacitance comes much closer to fulfilling this goal than most other 7542 compatible DAC's. Thus, faster, more well controlled settling is seen with the HDAC7542A.

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Table I - Input Logic Truth Table

HDAC7542A CONTROL INPUTS					HDAC7542A OPERATION
A1	A0	$\overline{CS}$	$\overline{WR}$	$\overline{CLR}$	
X	X	X	X	0	RESETS DAC REGISTER TO 0000 0000 0000 (1)
X	X	1	X	1	NO OPERATION, DEVICE NOT SELECTED
0	0	0	↑	1	LOAD L-BYTE DATA REGISTER WITH DATA AT D0-D3
0	1	0	↑	1	LOAD M-BYTE DATA REGISTER WITH DATA AT D0-D3
1	0	0	↑	1	LOAD H-BYTE DATA REGISTER WITH DATA AT D0-D3
1	1	0	⊓	1	LOAD DAC REGISTER WITH L, M, H-BYTE REG. DATA

NOTE (1) :
CLR = 0 ASYNCHRONOUSLY RESETS DAC REGISTER TO 0000 0000 0000 BUT HAS NO EFFECT ON INPUT REGISTERS.

0 = LOGIC LOW
1 = LOGIC HIGH
X = DON'T CARE
↑ = POSITIVE EDGE TRIGGERED
⊓ = LEVEL TRIGGERED

INTERFACE LOGIC

Data is loaded into the HDAC7542A in three 4-bit bytes through data pins D0, D1, D2, and D3. Address pins A0 and A1 select the loading of internal byte register H (high byte), M (middle Byte) or L (low byte). Address pins A0 and A1 also allow the selection of the internal 12-bit DAC register, which is loaded by the H, M and L register simultaneously. Data in the internal DAC register determines the DAC analog output value. Table 1 above provides the complete input logic truth table.

Write timing, as shown in the Write Cycle Timing Diagram, is similar to data loading of a RAM device. Note that pin $\overline{WR}$ is used to both load the input byte registers and the internal DAC register. The $\overline{CLR}$ pin, when momentarily brought to logic 0, resets the internal DAC register to 0000 0000 0000. This feature is useful for system initialization since the DAC output is set to a known condition.

UNIPOLAR BINARY OPERATION - 2 QUADRANT MULTIPLICATION

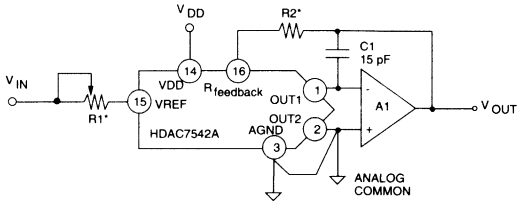
Figure 6 illustrates the use of the HDAC7542A in a unipolar (or 2 quadrant multiplication) mode. The V_{REF} is applied from pin 15 to ground voltage or an input current can be applied to pin 15. Positive or negative voltages/current can be applied. The input is multiplied by (-1) times the DAC code scaling.

R1 can be used to provide full scale output trimming capability. The adjustment is made by selecting code 1111 1111 1111 and changing R1 for (4095/4096) of the V_{REF} voltage out. If the source of V_{REF} is adjustable, V_{REF} could be directly adjusted for full scale calibration. (See Table III.)

The output capacitance of OUT1 must be compensated as described in Equivalent Circuit Analysis by the use of C1 in the feedback path. This cancels the feedback pole caused by OUT1's capacitance.

The op-amp used with the HDAC7542 should be selected for low offset voltage and low bias currents to reduce offset and linearity errors as described in Equivalent Circuit Analysis. The op-amp's bias currents appear as errors in the same fashion as the DAC's leakage currents. The op-amp offset voltage should be less than approximately 10% of an LSB (of the output full scale voltage). This is due to the offset effect which is code dependent and contributes to the nonlinearity in proportion to its size with respect to full scale output voltage.

Figure 6 - Unipolar Binary Operation



* REFER TO TABLE II

BIPOLAR OPERATION - 4 QUADRANT MULTIPLICATION

The use of the HDAC7542A in a bipolar (or 4 quadrant multiplication) mode is illustrated in figure 7. The V_{REF} is applied from pin 15 to ground voltage or an input current can be applied to pin 15. Positive or negative voltages/current can be applied. The output is either +1 or -1 times the code scaling of the DAC. The polarity is selected by the MSB of the DAC input code.

Amplifier A1's output is subtracted from 1/2 the value of V_{REF} to produce a maximum output which is half of V_{REF} in either polarity (see Table IV for the exact scaling). The MSB of the DAC selects the polarity of the output.

Full scale calibration of the output can be made by adjusting R5 or the V_{REF} source itself. Calibration of the zero output at code 1000 0000 0000 is made by adjusting R1. It is key that R3, R4 and R5 track each other for the stability of the summation made at A2. Failure of these resistors to track will result in both gain and offset drift over temperature even though calibration is done at room temperature.

As with unipolar operation, C1 is needed to compensate the OUT1 capacitance. A1 must be selected for low offset voltage and bias current to minimize nonlinearity and offset errors.

Table II - Recommended Trim Resistor Values vs Grades

	TRIM RESISTOR	
	"A" grades	"B" grades
R1	20Ω	100Ω
R2	6.8Ω	33Ω

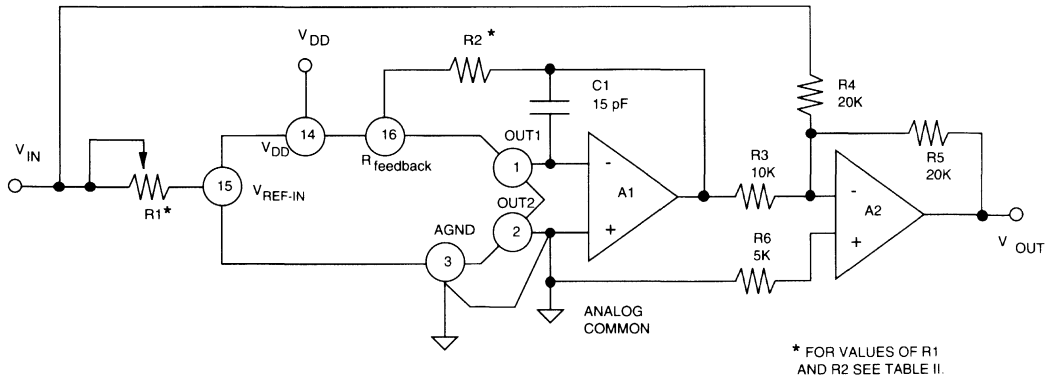
Table III - Unipolar Binary Code Table for Circuit of Figure 4

BINARY NUMBER IN DAC MSB		LSB	ANALOG OUTPUT, V_{OUT}
1111	1111	1111	$-V_{IN}\left(\frac{4095}{4096}\right)$
1000	0000	0000	$-V_{IN}\left(\frac{2048}{4096}\right) = -1/2\ V_{IN}$
0000	0000	0001	$-V_{IN}\left(\frac{1}{4096}\right)$
0000	0000	0000	0 Volts

Table IV- Bipolar Binary Code Table for Circuit of Figure 5

BINARY NUMBER IN DAC MSB		LSB	ANALOG OUTPUT, V_{OUT}
1111	1111	1111	$+V_{IN}\left(\frac{2047}{2048}\right)$
1000	0000	0001	$+V_{IN}\left(\frac{1}{2048}\right)$
1000	0000	0000	0V
0111	1111	1111	$-V_{IN}\left(\frac{1}{2048}\right)$
0000	0000	0000	$-V_{IN}\left(\frac{2048}{2048}\right)$

Figure 7 - Bipolar Operation



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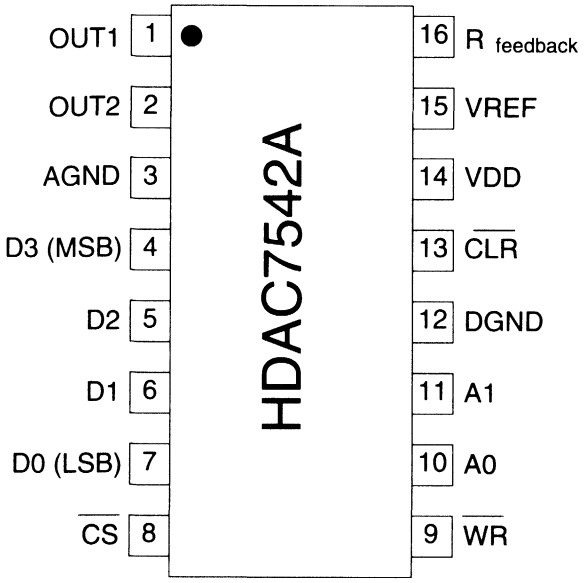
PIN ASSIGNMENT HDAC7542A



PIN FUNCTIONS HDAC7542A

NAME	FUNCTION
OUT1	Analog Current Output 1
OUT2	Analog Current Output 2
AGND	Analog Ground
D3	Data Bus Input 3 (MSB)
D2	Data Bus Input 2
D1	Data Bus Input 1
D0	Data Bus Input 0 (LSB)
$\overline{CS}$	Chip Select Input
$\overline{WR}$	Data Write Input
A0	Address Bus Input 0
A1	Address Bus Input 1
DGND	Digital Ground
$\overline{CLR}$	Clear Input for DAC Reg
VDD	Positive Power Supply
VREF	Reference Input Voltage
$R_{feedback}$	Internal Feedback Resistor

LEADERSHIP IN DATA CONVERSION AND SIGNAL PROCESSING

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SIGNAL PROCESSING TECHNOLOGIES

HDAC7543A

CMOS, 12-BIT SERIAL INPUT BUFFERED MULTIPLYING DAC

FEATURES

- Improved Version of the AD7543
- Max Gain Error <1/2 LSB (A/G Grade)
- 500 ns Settling Time
- 12-Bit Linearity Over Temperature
- Low Gain Drift (<3 ppm/°C)
- Serial Data Load With Flexible Strobe Conditions
- Four Quadrant Multiplication

APPLICATIONS

- Proportional Controllers Requiring Serial Isolation or Remote Location
- Industrial and Process Controllers

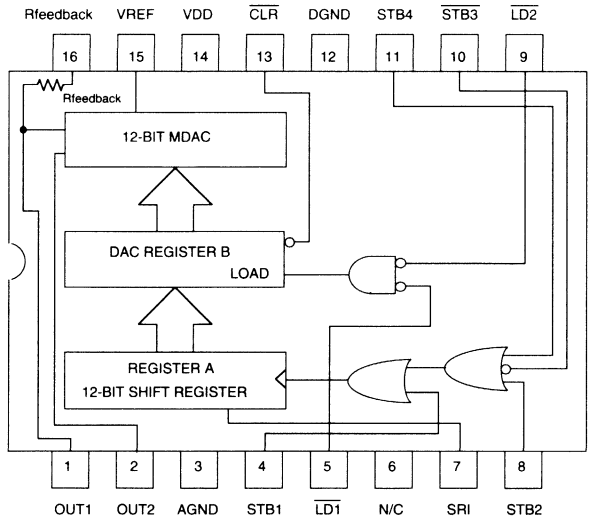
GENERAL DESCRIPTION

The HDAC7543A is a monolithic, low cost, multiplying 12-bit digital-to-analog converter (DAC) designed for serial digital input. It is compatible with the industry standard AD7543 but has significant performance improvements in speed and gain accuracy. The HDAC7543A is fabricated in a three-micron polysilicon gate BEMOS process and operates from a single +5 V (maximum) supply. Excellent linearity and gain accuracy are achieved through the use of laser-trimmed thin film resistors. Latch-up immunity is ensured by the use of an epi process base. This eliminates the need for external Schottky clamping diodes for latch-up protection.

The data bits for selecting the DAC output are written into the HDAC7543A via a serial data port prior to latching them into the output register. The input bits are double buffered on-chip. The serial bus control pins provide a great deal of flexibility in providing the serial input strobe conditions for the data transfer. A clear pin ($\overline{CLR}$) allows for resetting the output to all zeros under power up or system reset conditions.

The HDAC7543A's direct serial data interconnect makes it an excellent choice for industrial or process controllers which require electrical isolation or remote location. The serial bus minimizes the number of control lines which would require isolation devices or line drivers in these types of applications.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Beyond which damage may occur)[1] 25 °C

Supply Voltages
V_{DD} to GND ..... +7 V
AGND to GND ..... -0.3 to V_{DD}
Input Voltages
$V_{Rfeedback}$ to GND ..... ±25 V
Digital Input Voltage to GND ..... 0.3 to V_{DD}
Outputs
V_{out1} or V_{out2} to GND ..... -0.3 V to V_{DD}

Temperature
Operating Temperature, ambient ..... -55 to +125 °C
junction ..... +150 °C
Lead Temperature, (soldering 10 seconds) ..... +300 °C
Storage Temperature ..... -65 to +150 °C
Power Dissipation (Any Package) to +75 °C 450mW
(Derates above +75 °C by 6 mW/°C)

Note 1: Operation at any Absolute Maximum Rating is not implied. See Operating Conditions for proper nominal appliied conditions in typical applications.

ELECTRICAL SPECIFICATIONS

$T_A=T_{MIN}$ to T_{MAX}, V_{DD}=+5 V; V_{REF}=+10 V, OUT1=OUT2=0 V, AGND=DGND, unless otherwise specified.

TEST PARAMETERS	TEST CONDITIONS	TEST LEVEL	HDAC7543AA/G MIN	HDAC7543AA/G NOM	HDAC7543AA/G MAX	HDAC7543AA MIN	HDAC7543AA NOM	HDAC7543AA MAX	HDAC7543AB MIN	HDAC7543AB NOM	HDAC7543AB MAX	UNITS
DC ELECTRICAL CHARACTERISTICS												
Resolution		I		12			12			12		Bits
Relative Accuracy		I	-0.5	±0.25	+0.5	-0.5		+0.5	-1		+1	LSB
Differential Nonlinearity	Guaranteed 12-Bit Monotonic	I	-1		+1	-1		+1	-1		+1	LSB
Gain Error	25 °C	I	-.5		+.5	-2		+2	-3		+3	LSB
Using Internal $R_{feedback}$	Tmin - Tmax	I	-1.5		+1.5	-3		+3	-4		+4	LSB
Gain Temperature Coefficient		IV		0.3	3		0.3	3		0.3	3	ppm/°C
Output Leakage OUT1[4] and OUT2	25 °C	I	-1		+1	-1		+1	-1		+1	nA
	0-70 °C/-25 to +85 °C	I	-10		+10	-10		+10	-10		+10	nA
	-55 to +125 °C	I	-50		+50	-50		+50	-50		+50	nA
	All Digital Inputs at 0 V											
Reference Input Resistance	Pin 15 to GND											
	+25 °C	IV	7	12.5	18	7	12.5	18	7	12.5	18	kΩ
	Temp. Coefficient	IV		-180			-180			-180		ppm/°C
DIGITAL INPUTS												
V_{IH} (High Input Voltage)		I	2			2			2			V
V_{IL} (Low Input Voltage)		I			0.8			0.8			0.8	V
I_{IN} (Input Currents I_{IH}, I_{IL})		I			±1			±1			±1	µA
C_{IN} (Input Capacitance)	VIN=0 Volts	IV			5			5			5	pF

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ELECTRICAL SPECIFICATIONS

$T_A=T_{MIN}$ to T_{MAX}, V_{DD}=+5 V; V_{REF}=+10 V, OUT1=OUT2=0 V, AGND=DGND, unless otherwise specified.

TEST PARAMETERS	TEST CONDITIONS	TEST LEVEL	HDAC7543AA/G MIN	HDAC7543AA/G NOM	HDAC7543AA/G MAX	HDAC7543AA MIN	HDAC7543AA NOM	HDAC7543AA MAX	HDAC7543AB MIN	HDAC7543AB NOM	HDAC7543AB MAX	UNITS
AC ELECTRICAL CHARACTERISTICS												
Multiplying Feedthrough Error	V_{REF} to V_{OUT} V_{REF}=±10 V 10 kHz Sinewave	IV		0.3	0.5		0.3	0.5		0.3	0.5	mV(p-p)
Output Current Settling Time[1,3]		IV		0.5	1.0		0.5	1.0		0.5	1.0	µsec
Capacitance OUT1	Digital Inputs=V_{IH} $\overline{WR}$=$\overline{CS}$=0 V	IV			75			75			75	pF
Capacitance OUT2	Digital Inputs=V_{IL} $\overline{WR}$=$\overline{CS}$=0 V	IV			30			30			30	pF
Power Supply Rejection Ratio	+25 °C	I			.005			.005			.005	%
	Over Temperature	I			.01			.01			.01	%
Serial Input (t_{DS1})	STB1 Strobed	I	50			50			50			nsec
to Strobe (t_{DS2})	STB2 Strobed	I	20			20			20			nsec
Setup Time (t_{DS3})	$\overline{STB3}$ Strobed	I	0			0			0			nsec
(t_{DS4})	STB4 Strobed	I	0			0			0			nsec
Serial Input (t_{DH1})	STB1 Strobed	I	30			30			30			nsec
to Strobe (t_{DH2})	STB2 Strobed	I	60			60			60			nsec
Hold Time (t_{DH3})	$\overline{STB3}$ Strobed	I	80			80			80			nsec
(t_{DH4})	STB4 Strobed	I	80			80			80			nsec
t_{SRI} (SRI Data Pulse Width)		I	80			80			80			nsec
t_{STB1} (STB1 Pulse Width)		I	40			40			40			nsec
t_{STB2} (STB2 Pulse Width)		I	40			40			40			nsec
t_{STB3} ($\overline{STB3}$ Pulse Width)		I	40			40			40			nsec
t_{STB4} (STB4 Pulse Width)		I	40			40			40			nsec
$t_{LD1,LD2}$ (Load Pulse Width)		I	120			120			120			nsec
t_{ASB} (Min. Time Between Strobing LSB into Register A and Loading Register B		IV	0			0			0			nsec
t_{CLR} ($\overline{CLR}$ Pulse Width)		I	100			100			100			nsec

Note 1: OUT1 load: 100 Ω + 13 pF.
Note 2: Digital inputs change from 0 V to V_{DD} or V_{DD} to 0 V.
Note 3: Measured from falling edge of $\overline{WR}$.
Note 4: Digital inputs $\overline{WR}$ and $\overline{CS}$ at 0 V.
Note 5: Measured from falling edge of $\overline{WR}$ to 90% of final output value.

TEST LEVEL CODES

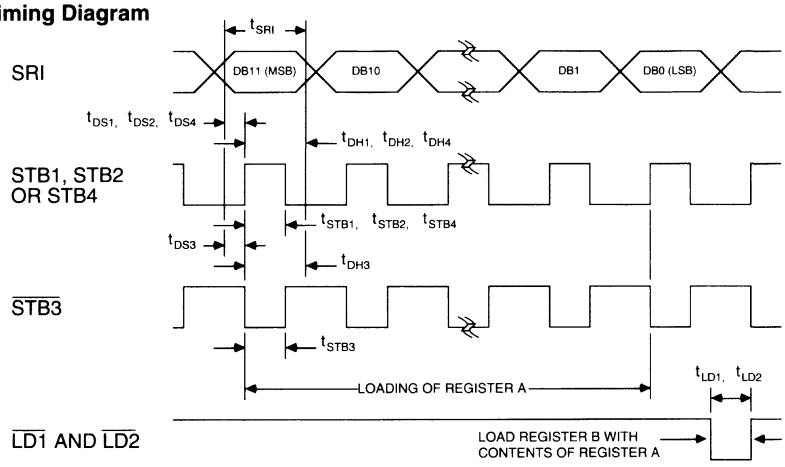
All electrical characteristics are subject to the following conditions:

All parameters having min/max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality Assurance inspection. Any blank section in the data column indicates that the specification is not tested at the specified condition.

Unless otherwise noted, all tests are pulsed tests; therefore, $T_J = T_C = T_A$.

TEST LEVEL	TEST PROCEDURE
I	100% production tested at the specified temperature.
II	100% production tested at T_A=25 °C, and sample tested at the specified temperatures.
III	QA sample tested only at the specified temperatures.
IV	Parameter is guaranteed (but not tested) by design and characterization data.
V	Parameter is a typical value for information purposes only.
VI	100% production tested at T_A = 25 °C. Parameter is guaranteed over specified temperature range.

Figure 1 - Logic Timing Diagram



TERMINOLOGY

RELATIVE ACCURACY

Relative accuracy or endpoint nonlinearity is a measure of the maximum deviation from a straight line passing through the endpoints of the DAC transfer function. It is measured after adjusting for zero and full scale and is expressed in percentage of full scale range or (sub)multiples of 1 LSB.

DIFFERENTIAL NONLINEARITY

Differential nonlinearity is the difference between the measured change and the ideal 1 LSB change between any two adjacent codes. A specified differential nonlinearity of 1 LSB (max) over the operating temperature range ensures monotonicity.

MULTIPLYING FEEDTHROUGH ERROR

AC error due to capacitive feedthrough from the V_{REF} terminal to OUT1 with the DAC loaded to all 0s.

GAIN ERROR

Gain error or full-scale error is a measure of the output error between an ideal DAC and the actual device output. For the HDAC7543A ideal full-scale output is $-(4095)/(4096)\bullet(V_{REF})$. Gain error is adjustable to zero using external trims as shown in figures 6 and 7.

OUTPUT LEAKAGE CURRENT

Current which appears at OUT1 with the DAC loaded to all 0s, or OUT2 with the DAC loaded to all 1s.

OUTPUT CURRENT SETTLING TIME

Time required for the output of the DAC to settle to within 1/2 LSB for a given digital input stimulus, i.e., 0 to Full Scale.

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CIRCUIT DESCRIPTION

As shown in the block diagram, the HDAC7543A consists of a 12 bit multiplying DAC and data input logic. The data input logic consists of a serial input data register (register A) and a parallel DAC register (register B). Register A loads register B with a 12-bit parallel data work. The content of register B controls the DAC's output. Data entry is further described in the Interface Logic section.

Figure 2A shows a simplified version of the 12-bit multiplying DAC circuitry. Note that the HDAC7543A uses a modified R-2R ladder technique that provides for superior linearity over similar devices which use the basic R-2R ladder.

A basic R-2R ladder portion is used within the HDAC7543A for the nine least-significant bits (bits 0-8). This ladder portion successively divides the remaining VREF input to produce a binary weighted nine-stage current division. In other words, in moving from left to right, each 2R resistor leg has half the current flow of the previous leg. Double-pole switches within each leg are controlled by the respective input data bit. The switches route the bit-weighted current of the leg to either analog ground or to the output (pin OUT1). OUT1 is a virtual ground by means of the external active circuitry. Hence, with every switch in either position, the R-2R ladder resistive integrity is maintained. Input resistance of pin VREF is kept constant.

Modification of the basic R-2R ladder structure occurs in the three most-significant bits. Here, the switches of seven equally weighted current dividers are controlled by bits 9-11 via a logic decoder. Although more complex, this method provides increased accuracy. Application of the HDAC7543A is identical to similar devices that use an un-modified R-2R ladder network.

The DAC output current is converted to a voltage by the feedback resistance composed of the external resistor shown in Figure 2A in series with internal resistor $R_{feedback}$. The operational amplifier provides a buffered VOUT, and in combination with the feedback resistance maintains OUT1 at virtual ground. The transfer function of Figure 2B shows the relationship of VOUT for an equivalent R-2R resistor network, shown in the same figure. A more detailed explanation of the circuit operation and performance aspects is found in the following Equivalent Circuit Analysis section.

Figure 2A - Simplified Circuit Description

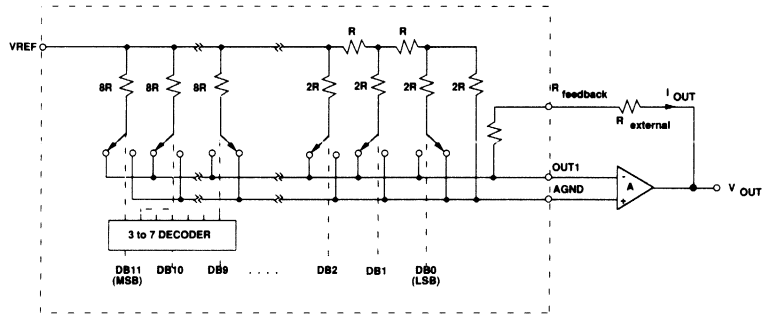
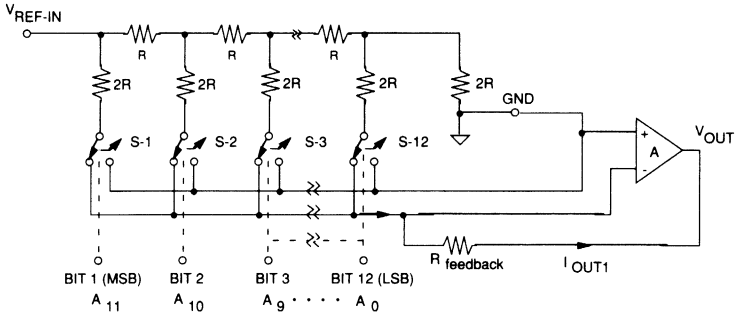


Figure 2B - Equivalent R-2R Network



The transfer function for the HDAC7543A connected in the multiplying mode as shown in figure 2B is:

$$V_O = -V_{REF} \times \left(\frac{A_{11}}{2^1} + \frac{A_{10}}{2^2} + \frac{A_9}{2^3} \cdots \frac{A_0}{2^{12}} \right)$$ in which A_x assumes a value of 1 for a HIGH bit and 0 for a Low bit.

EQUIVALENT CIRCUIT ANALYSIS

The equivalent output circuit of the HDAC7543A is the key to understanding offset, linearity and settling time. Figures 3 and 4 illustrate these effects.

In figure 3, the equivalent unipolar operation is illustrated with an external op-amp and all switches LOW to route all current to OUT2. OUT2 is internally connected to AGND in packaged versions of the HDAC7543A. The current from OUT2 is composed of (4095/4096)-th's of the input current at pin V_{REF} plus parasitic leakage currents of the switches. These leakage currents are due to both junction and surface leakage on the MOS switches. 1/4096-th of the input current passes to the ground through the ladder terminal 2R resistor. OUT1 DC current is due only to switch leakage.

Figure 4 shows the same equivalent circuit when all switches are HIGH thereby routing all current to OUT1. The conditions are symmetrical in this case to figure 3.

The main effect of switch leakages in either case is an offset voltage from the DAC when used in voltage output mode as shown in figures 3 and 4.

Figure 3 - HDAC7543A DAC Equivalent Circuit All Digital Inputs Low

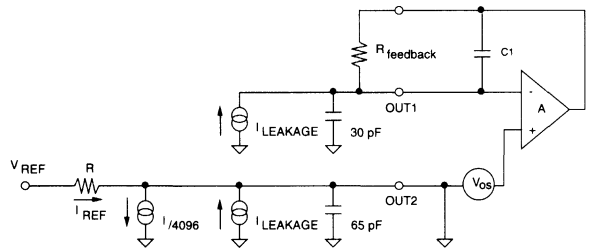
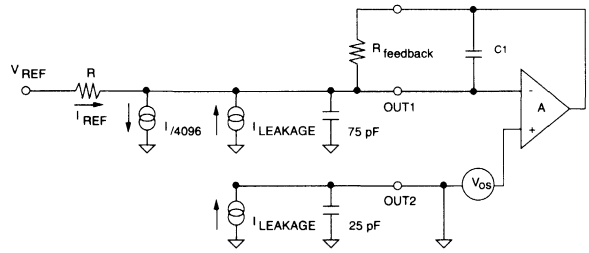


Figure 4 - HDAC7543A DAC Equivalent Circuit All Digital Inputs High



The output resistance seen at the input terminals of the op-amp varies with the code chosen. Between figures 3 and 4, resistance at each op-amp input can change from 10k Ohms to an open for extremes in code. This causes the gain of the offsets (due to either leakage currents of the DAC or op-amp offset) to be code dependent. For example, the gain of offsets of the op-amp under these extreme cases is given below:

Offset gain=1 + $R_{feedback}$/RDAC

With all code bits LOW:
RDAC >> $R_{feedback}$; offset gain=1

With all code bits HIGH:
RDAC= $R_{feedback}$; offset gain=2

Thus, the offset is not amplified by a constant gain over the range of code input. This variation in offset gain is seen as a nonlinearity in the voltage output over the full scale output. The magnitude of nonlinearity is the difference in the gains at code extremes times the offset voltage. In this DAC, this nonlinearity is equal to the offset itself. Thus, the total offset voltage of the op-amp plus leakage induced offset of the DAC and op-amp must be kept to less than 1 LSB to prevent degradation to the DAC linearity performance.

The dynamic output impedance of OUT1 and OUT2 is composed of the DAC switch capacitances to ground. OUT2 has the capacitance of the OFF switches while OUT1 has switch capacitance for ON switches.

The capacitance on OUT1 creates a feedback pole in the voltage output operation mode (figures 3 and 4). Instability of the output amplifier can occur due to the presence of this pole. This pole's instability effect is typically compensated by the use of a feedback capacitor - C1 (figures 6 and 7). Although all R-2R DAC's have the need for this type of compensation, the HDAC7543A maintains faster settling times when used in the voltage output mode. This is due to the lower output capacitance of the HDAC7543A.

The choice of compensation capacitor is bounded by three limits:

- C1 along with $R_{feedback}$ determines the settling time of the output voltage from the op-amp; therefore C1 should be as small as possible for minimum settling time.
- The pole defined by C1 and $R_{feedback}$ should be smaller than secondary poles in the op-amp: as a rule of thumb, about one half of the op-amp's gain-bandwidth.
- Settling time is proportional to $\sqrt{C_{OUT\,1} + C1}$.

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For an OP-27 used as an output op-amp with 8 MHz gain-bandwidth, the choice of C1 is:

$(2 \bullet \pi \bullet C1 \bullet R_{feedback})^{-1} = 4$ MHz or C1= 3 pf

$\bullet R_{feedback} = 12.5\ k\Omega$

Fast settling time with small amounts of ringing are obtained when the small values of C1 (given by the criteria above) are as close as possible to the DAC output capacitance. The HDAC7543A 's low output capacitance comes much closer to fulfilling this goal than most other 7543 compatible DAC's. Thus, faster, more well controlled settling is seen with the HDAC7543A.

Table 1 - Input Logic Truth Table

REGISTER A CONTROL INPUTS				REGISTER B CONTROL INPUTS			HDAC7543A OPERATION
STB4	$\overline{STB3}$	STB2	STB1	$\overline{CLR}$	$\overline{LD2}$	$\overline{LD1}$	
0	1	0	↑	X	X	X	DATA APPEARING AT SRI IS STROBED INTO REGISTER A (MSB FIRST)
0	1	↑	0	X	X	X	
0	↓	0	0	X	X	X	
↑	1	0	0	X	X	X	
1	X	X	X				NO OPERATION OF REGISTER A
X	0	X	X				
X	X	1	X				
X	X	X	1				
				0	X	X	SET REG. B TO 0000 0000 0000 (1)
				1	1	X	NO OPERATION OF REGISTER B
				1	X	1	
				1	0	0	LOAD REG. B WITH CONTENTS OF REG. A

NOTE (1) :
CLR = 0 ASYNCHRONOUSLY RESETS REGISTER B TO 0000 0000 0000 BUT HAS NO EFFECT ON REGISTER A.

0 = LOGIC LOW
1 = LOGIC HIGH
X = DON'T CARE
↑ = POSITIVE EDGE
↓ = NEGATIVE EDGE

INTERFACE LOGIC

Data is loaded into the HDAC7543A serially through pin SRI. The serial data is clocked into register A with either pin STB1, STB2 or STB4 at the rising clock edge or with pin $\overline{STB3}$ at the falling clock edge. When register A has been loaded with the 12 data bits, the data is transferred to register B by bringing both pin $\overline{LD1}$ and $\overline{LD2}$ momentarily low. Refer to the Logic Timing Diagram for loading sequence.

When pin $\overline{CLR}$ is momentarily brought to logic 0, register B is reset to 0000 0000 0000. This feature is useful for system initialization since the DAC output is set to a known condition.

UNIPOLAR BINARY OPERATION - 2 QUADRANT MULTIPLICATION

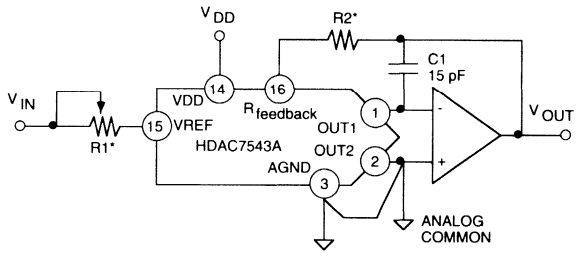
Figure 6 illustrates the use of the HDAC7543A in a unipolar (or 2 quadrant multiplication) mode. The V_{REF} is applied from pin 15 to ground voltage or an input current can be applied to pin 15. Positive or negative voltages/current can be applied. The input is multiplied by (-1) times the DAC code scaling.

R1 can be used to provide full scale output trimming capability. The adjustment is made by selecting code 1111 1111 1111 and changing R1 for (4095/4096) of the V_{REF} voltage out. If the source of V_{REF} is adjustable, V_{REF} could be directly adjusted for full scale calibration. (See Table III.)

The output capacitance of OUT1 must be compensated as described in Equivalent Circuit Analysis by the use of C1 in the feedback path. This cancels the feedback pole caused by OUT1's capacitance.

The op-amp used with the HDAC7543A should be selected for low offset voltage and low bias currents to reduce offset and linearity errors as described in Equivalent Circuit Analysis. The op-amp's bias currents appear as errors in the same fashion as the DAC's leakage currents. The op-amp offset voltage should be less than approximately 10% of an LSB (of the output full scale voltage). This is due to the offset effect which is code dependent and contributes to the nonlinearity in proportion to its size with respect to full scale output voltage.

Figure 6 - Unipolar Binary Operation



*REFER TO TABLE II

BIPOLAR OPERATION - 4 QUADRANT MULTIPLICATION

The use of the HDAC7543A in a bipolar (or 4 quadrant multiplication) mode is illustrated in figure 7. The V_{REF} is applied from pin 15 to ground voltage or an input current can be applied to pin 15. Positive or negative voltages/current can be applied. The output is either +1 or -1 times the code scaling of the DAC. The polarity is selected by the MSB of the DAC input code.

Amplifier A1's output is subtracted from 1/2 the value of V_{REF} to produce a maximum output which is half of V_{REF} in either polarity (see Table IV for the exact scaling). The MSB of the DAC selects the polarity of the output.

Full scale calibration of the output can be made by adjusting R5 or the V_{REF} source itself. Calibration of the zero output at code 1000 0000 0000 is made by adjusting R1. It is key that R3, R4 and R5 track each other for the stability of the summation made at A2. Failure of these resistors to track will result in both gain and offset drift over temperature even though calibration is done at room temperature.

As with unipolar operation, C1 is needed to compensate the OUT1 capacitance. A1 must be selected for low offset voltage and bias current to minimize nonlinearity and offset errors.

Table II - Recommended Trim Resistor Values vs Grades

	TRIM RESISTOR	
	"A" grades	"B" grades
R1	20Ω	100Ω
R2	6.8Ω	33Ω

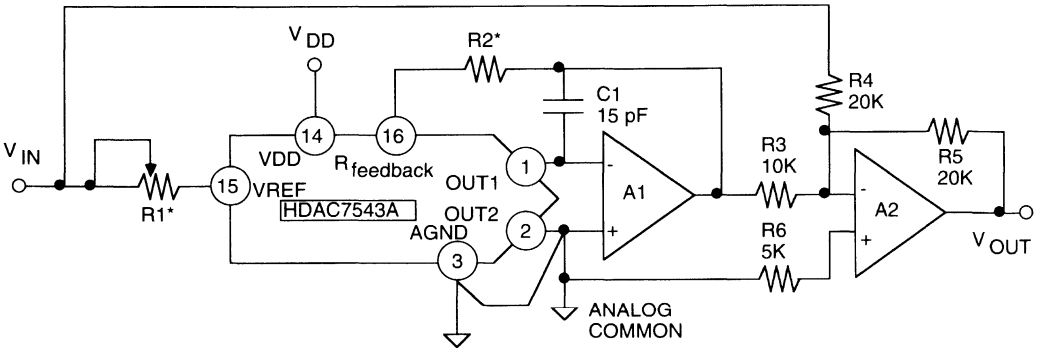
Table III - Unipolar Binary Code Table for Circuit of Figure 4

BINARY NUMBER IN DAC MSB		LSB	ANALOG OUTPUT, V_{OUT}
1111	1111	1111	$-V_{IN}\left(\frac{4095}{4096}\right)$
1000	0000	0000	$-V_{IN}\left(\frac{2048}{4096}\right) = -1/2\ V_{IN}$
0000	0000	0001	$-V_{IN}\left(\frac{1}{4096}\right)$
0000	0000	0000	0 Volts

Table IV - Bipolar Binary Code Table for Circuit of Figure 5

BINARY NUMBER IN DAC MSB		LSB	ANALOG OUTPUT, V_{OUT}
1111	1111	1111	$+V_{IN}\left(\frac{2047}{2048}\right)$
1000	0000	0001	$+V_{IN}\left(\frac{1}{2048}\right)$
1000	0000	0000	0V
0111	1111	1111	$-V_{IN}\left(\frac{1}{2048}\right)$
0000	0000	0000	$-V_{IN}\left(\frac{2048}{2048}\right)$

Figure 7 - Bipolar Operation



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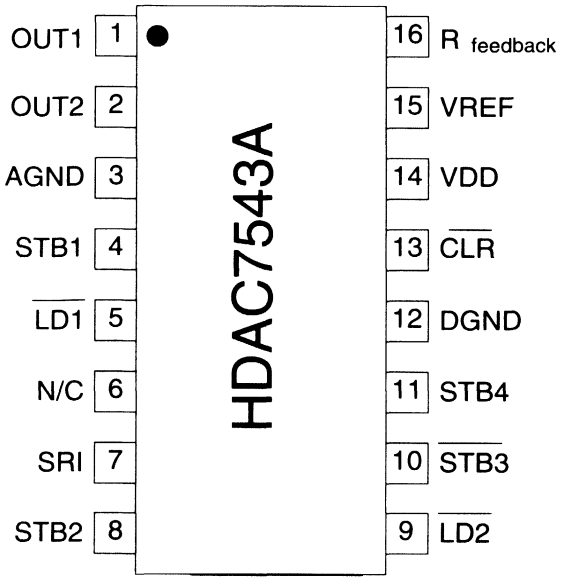
PIN ASSIGNMENT HDAC7543A



PIN FUNCTIONS HDAC7543A

NAME	FUNCTION
OUT1	Analog Current Output 1
OUT2	Analog Current Output 2
AGND	Analog Ground
STB1	Strobe Input 1 for Reg A
$\overline{LD1}$	Load Input 1 for Reg B
N/C	No Connection
SRI	Serial Data Input
STB2	Strobe Input 2 for Reg A
$\overline{LD2}$	Load Input 2 for Reg B
STB3	Strobe Input 3 for Reg A
STB4	Strobe Input 4 for Reg A
DGND	Digital Ground
$\overline{CLR}$	Clear Input for Reg B
VDD	Positive Power Supply
VREF	Reference Input Voltage
$R_{feedback}$	Internal Feedback Resistor

LEADERSHIP IN DATA CONVERSION AND SIGNAL PROCESSING

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SPT
SIGNAL PROCESSING TECHNOLOGIES

HDAC10180

8-BIT, HIGH SPEED D/A CONVERTER

4

FEATURES

- 275 MWPS Conversion Rate - A Version
- 165 MWPS Conversion Rate - B Version
- Compatible with TDC1018 with Improved Performance
- RS-323-A Compatible
- Complete Video Controls: Sync, Blank, Bright and Reference White (Force High)
- 10 kHz, 100 kΩ ECL Compatible
- Single Power Supply
- Registered Data and Video Controls
- Differential Current Outputs

APPLICATIONS

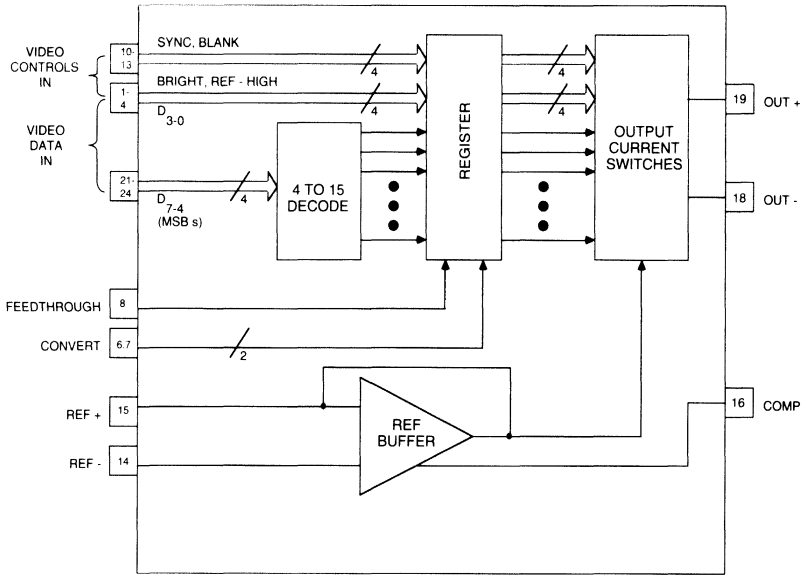
- High Resolution Color or Monochrome Raster Graphics Displays
- Medical Electronics: CAT, PET, MR Imaging Displays
- CAD/CAE Workstations
- Solids Modeling
- General Purpose High-Speed D/A Conversion
- Digital Synthesizers
- Automated Test Equipment
- Digital Transmitters/Modulators

GENERAL DESCRIPTION

The HDAC10180 is a monolithic 8-bit digital-to-analog converter capable of accepting video data at a 165 or 275 MWPS rate. Complete with video controls (Sync, Blank, Reference White, [Force High] Bright), the HDAC10180 directly drives doubly-terminated 50 or 75 Ohm loads to standard composite video levels. Standard set-up level is 7.5 IRE. The HDAC10180 is pin-compatible with the TDC1018, with improved performance, and two can be used with the HDAC10181. The HDAC10180 contains data and control input registers, video control logic, reference buffer, and current switches in a 24-lead CERDIP package.

A standard military drawing is available as DESC drawing 5962-91748.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATING (Beyond which damage may occur)[1]

Supply Voltages

V_{EED} (measured to V_{CCD}) ..... -7.0 to 0.5 V
V_{EEA} (measured to V_{CCA}) ..... -7.0 to 0.5 V
V_{CCA} (measured to V_{CCD}) ..... -0.5 to 0.5 V

Input Voltages

CONV, Data, and Controls ..... V_{EED} to 0.5 V
(measured to V_{CCD})

REF + (measured to V_{CCA}) ..... V_{EEA} to 0.5 V
REF - (measured to V_{CCA}) ..... V_{EEA} to 0.5 V

Temperature

Operating, ambient ..... -55 to + 125 °C
junction ..... + 175 °C
Lead, Soldering (10 seconds) ..... + 300 °C
Storage ..... -60 to + 150 °C

Note: 1. Operation at any Absolute Maximum Ratings is not implied. See Electrical Specifications for proper nominal applied conditions in typical applications.

ELECTRICAL SPECIFICATIONS

$V_{CCD} = V_{CCA}$ =ground, $V_{EEA} = V_{EED}$ = -5.2 V ±0.3 V, $T_A = T_{MIN}$ to T_{MAX}, C_C = 0 pF, I_{SET} = 1.105 mA

PARAMETERS	TEST CONDITIONS	TEST LEVEL	MIN	TYP	MAX	UNITS
DC ELECTRICAL CHARACTERISTICS						
Integral Linearity Error	1.0 mA<I_{SET}<1.3 mA	I	-.37 -.95		+.37 +.95	% Full Scale LSB
Differential Linearity Error	1.0 mA<I_{SET}<1.3 mA	I	-0.2 -0.5		+0.2 +0.5	% Full Scale LSB
Gain Error		I	-6.5		+6.5	% Full Scale
Gain Error Tempco		V		150		PPM/°C
Input Capacitance, REF +, REF -		V		5		pF
Compliance Voltage, + Output		I	-1.2		1.5	V
Compliance Voltage, - Output		I	-1.2		1.5	V
Equivalent Output Resistance		I	20			K Ohm
Output Capacitance		V		12		pF
Maximum Current, + Output		IV	45			mA
Maximum Current, - Output		IV	45			mA
Output Offset Current		I			0.5	LSB
Input Voltage, Logic HIGH		I	-1.0			V
Input Voltage, Logic LOW		I			-1.5	V
Convert Voltage, Common Mode Range		I	-0.5		-2.5	V
Convert Voltage, Differential		IV	0.4		1.2	V
Input Current, Logic LOW, Data and Controls		I			120	µA
Input Current, Logic HIGH, Data and Controls		I		10	120	µA
Input Current, Convert		I		2	60	µA

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ELECTRICAL SPECIFICATIONS

V_{CCD} = V_{CCA} =ground, V_{EEA} = V_{EED} = -5.2 V ±0.3 V, T_A =T_{MIN} to T_{MAX}, C_C = 0 pF, I_{SET} = 1.105 mA

PARAMETERS	TEST CONDITIONS	LEVEL	MIN	TYP	MAX	UNITS
DC ELECTRICAL CHARACTERISTICS						
Input Capacitance, Data and Controls		V		3.0		pF
Power Supply Sensitivity		I	-120		+120	µA/V
Supply Current		I		175	220	mA
DYNAMIC CHARACTERISTICS (R_L = 37.5 Ohms, C_L = 5 pF, T_A = 25 °C, I_{SET} = 1.105 mA)						
Maximum Conversion Rate	B Grade A Grade	III III	165 275			MWPS MWPS
Rise Time	10% to 90% G.S. $T_A = T_{MIN}$ to T_{MAX}	III IV			1.6 2.0	ns ns
Rise Time	10% to 90% G.S. R_L = 25 Ohms	IV		1.0		ns
Current Settling Time, Clocked Mode	To 0.2%	IV		7.0		ns
Current Settling Time, Clocked Mode	To 0.8%	IV		5.5		ns
Current Settling Time, Clocked Mode	To 0.2% R_L = 25 Ω	IV		4.5		ns
Clock to Output Delay, Clocked Mode	 $T_A = T_{MIN}$ to T_{MAX}	III IV			4.0 4.5	ns ns
Data and Output Delay, Transparent Mode		III IV			6.0 6.0	ns ns
Convert Pulse Width, (LOW or HIGH)	B Grade A Grade	III III	3.0 1.8			ns ns
Glitch Energy	Area = 1/2 VT	V		10		pV-s
Reference Bandwidth, -3 dB		V		1.0		MHz
Set-up Time, Data and Controls	 $T_A = T_{MIN}$ to T_{MAX}	III IV	1.3 1.3	1.8 1.8	2.0 2.0	ns ns
Hold Time, Data and Controls	 $T_A = T_{MIN}$ to T_{MAX}	III IV	0.5 0.5			ns ns
Slew Rate	20% to 80% G.S. $T_A = T_{MIN}$ to T_{MAX}	III IV	390 325			V/µS V/µS
Clock Feedthrough	 $T_A = T_{MIN}$ to T_{MAX}	III IV			-48 -48	dB dB

TEST LEVEL CODES

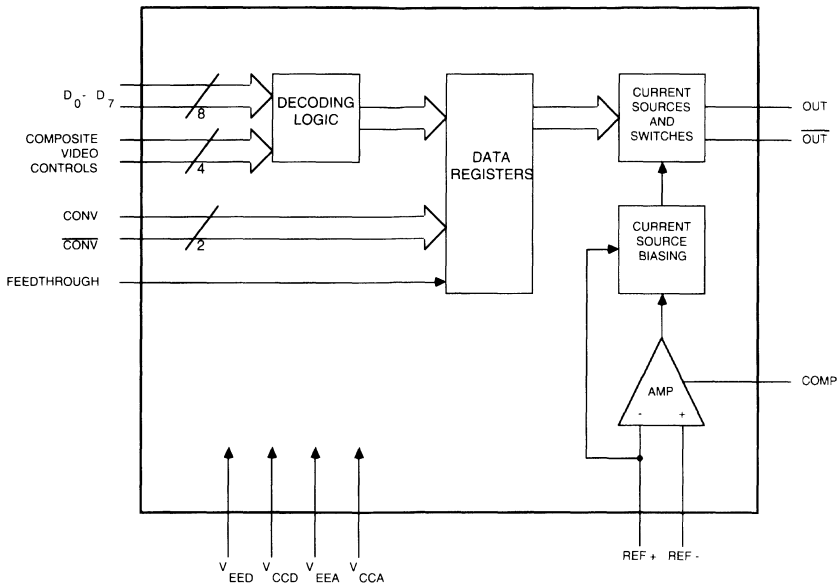
All electrical characteristics are subject to the following conditions:

All parameters having min/max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality Assurance inspection. Any blank section in the data column indicates that the specification is not tested at the specified condition.

Unless otherwise noted, all tests are pulsed tests, therefore $T_j = T_C = T_A$.

TEST LEVEL	TEST PROCEDURE
I	100% production tested at the specified temperature.
II	100% production tested at T_A = 25°C, and sample tested at the specified temperatures.
III	QA sample tested only at the specified temperatures.
IV	Parameter is guaranteed (but not tested) by design and characterization data.
V	Parameter is a typical value for information purposes only.

FUNCTIONAL DIAGRAM



APPLICATION INFORMATION

The HDAC10180 is a high speed video Digital-to-Analog converter capable of up to 275 MWPS conversion rates. This makes the device suitable for driving 1500 X 1800 pixel displays at 70 to 90 Hz update rates.

The HDAC10180 is separated into different conversion rate categories as shown in Table I.

The HDAC10180 has 10 KH and 100K ECL logic level compatible video controls and data inputs. The complementary analog output currents produced by the devices are proportional to the product of the digital control and data inputs in conjunction with the analog reference current. The HDAC10180 is segmented so that the four MSBs of the input data are separated into a parallel "thermometer" code. From here, fifteen current sinks, which are identical, are driven to fabricate sixteen coarse output levels. The remaining four LSBs drive four binary weighted current switches.

The MSB currents are then summed with the LSBs, which provide a one-sixteenth of full scale contribution, to provide the 256 distinct analog output levels.

The video control inputs drive weighted current sinks which are added to the output current to produce composite video output levels. These controls, Sync, Blank, Reference White (Force High), and Bright are needed in video applications.

Another feature that similar video D/A converters do not have is the Feedthrough Control. This pin allows registered or unregistered operation between the video control inputs and data. In the registered mode, the composite functions are latched to the pixel data to prevent screen-edge distortions generally found on unregistered VIDEO DACs.

Table I - The HDAC10180 Family and Speed Designations

PART NUMBER	UPDATE	COMMENTS
HDAC10180A	275 MWPS	Suitable for 1200 X 1500 to 1500 X 1800 displays at 60 to 90 Hz update rate.
HDAC10180B	165 MWPS	Suitable for 1024 X 1280 to 1200 X 1500 displays at 60 to 90 Hz update rate.

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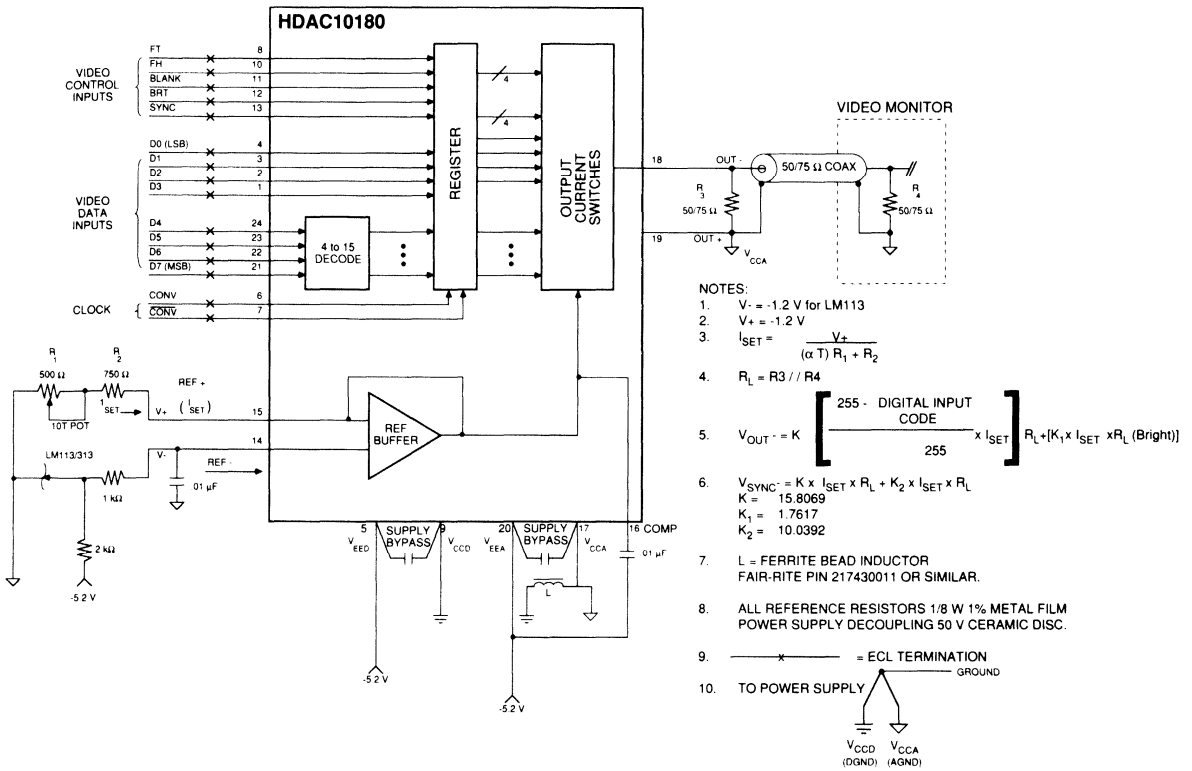
Figure 1 - Typical Interface Circuit



TYPICAL INTERFACE CIRCUIT

GENERAL

A typical interface circuit using the HDAC10180 in a color raster application is shown in Figure 1. The HDAC10180 requires few external components and is extremely easy to use. The very high operating speeds of the HDAC10180 requires good circuit layout, decoupling of supplies, and proper design of transmission lines. The following are several considerations that should be noted to achieve best performance.

INPUT CONSIDERATIONS

Video input data and controls may be directly connected to the HDAC10180. Note that all ECL inputs are terminated as close to the device as possible to reduce ringing, crosstalk and reflections. A convenient and commonly used microstrip impedance is about 130 Ohms, which is easily terminated using a 330 Ohm resistor to V_{EE} and a 220 Ohm resistor to Ground. This arrangement gives a Thevenin equivalent termination of 130 Ohms to -2 Volts without the need for a -2 Volt supply. Standard SIP (Single Inline Package) 220/330 resistor networks are available for this purpose.

It is recommended that stripline or microstrip techniques be used for all ECL interface. Printed circuit wiring of known impedance over a solid ground plane is recommended. The ground plane should be constructed such that analog and digital ground currents are isolated as much as possible. The HDAC10180 provides separate digital and analog ground connections to simplify ground layout.

OUTPUT CONSIDERATIONS

The analog outputs are designed to directly drive a dual 50 or 75 Ohm load transmission system as shown. The source impedances of the HDAC10180 outputs are high impedance current sinks. The load impedance (R_L) must be 25 or 37.5 Ohms to attain standard RS-343-A video levels. Any deviation from this impedance will affect the resulting video output levels proportionally. As with the data interface, it is important that the analog transmission lines have matched impedance throughout, including connectors and transitions between printed wiring and coaxial cable. The combination of matched source termination resistor R_S and load terminator R_L minimizes reflections of both forward and reverse traveling waves in the analog transmission system. The return path for analog output current is V_{CCA} which is connected to the source termination resistor R_S.

POWER CONSIDERATIONS

The HDAC10180 operates from a single standard -5.2 Volt supply. Proper bypassing of the supplies will augment the HDAC10180's inherent supply noise rejection characteristics. As shown in Figure 1, a large tantalum capacitor in parallel with smaller ceramic capacitors is recommended for best performance. The small-valued capacitors should be connected as close to the device package as possible, whereas the tantalum capacitor may be placed up to a few inches away.

The HDAC10180 operates with separate analog (V_{EEA}) and digital (V_{EED}) power supplies to establish high noise immunity. Both supplies can eventually be connected to the same power source, but they should be individually decoupled as mentioned previously. The digital supply has a separate ground return which is V_{CCD}. The analog supply return is V_{CCA}. All power and ground pins must be connected in any application. If a +5 V power source is required, the ground pins V_{CCD} and V_{CCA} become the positive supply pins while V_{EED} and V_{EEA} become the ground returns. The relative polarities of the other voltages on inputs and outputs must be maintained.

REFERENCE CONSIDERATIONS

The HDAC10180 has two reference inputs: REF - and REF +. Both pins are connected to the inverting and noninverting inputs of an internal amplifier that serves as a reference buffer amplifier.

The output of the buffer amplifier is the reference for the current sinks. The amplifier feedback loop is connected around one of the current sinks to achieve better accuracy. (See Figure 7.)

Since the analog output currents are proportional to the digital input data and the reference current (I_{SET}), the full-scale output may be adjusted by varying the reference current. I_{SET} is controlled through the REF + input on the HDAC10180. A method and equations to set I_{SET} is shown in Figure 1. The HDAC10180 uses an external negative voltage reference. The external reference must be stable to achieve a satisfactory output and the REF - pin should be driven through a resistor to minimize offsets caused by bias current. The value for I_{SET} can be varied with the 500 Ohm trimmer to change the full scale output. A double 50 Ohm load (25 Ohm) can be driven if I_{SET} is increased 50% more than ISET for doubly terminated 75 Ohm video applications.

COMPENSATION

The HDAC10180 provides an external compensation input (COMP) for the reference buffer amplifier. In order to use this pin correctly, a capacitor (C_C) should be connected between COMP and V_{EEA} as shown in Figure 1. Keep the lead lengths as short as possible. If the reference is to be kept as a constant, the C_C should be large (.01 µF). The value of C_C determines the bandwidth of the amplifier. If modulation of the reference is required, smaller values of C_C can be used to get up to a 1 MHz bandwidth.

DATA INPUTS AND VIDEO CONTROLS

The HDAC10180 has standard single-ended data inputs. The inputs are registered to produce the lowest differential data propagation delay (skew) to minimize glitching. There are also four video control inputs to generate composite video outputs. These are Sync, Blank, Bright and Reference White or Force High. Also provided is the Feedthrough control as mentioned earlier. The controls and data inputs are all 10 KH and 100K ECL compatible. In addition, all have internal pulldown resistors to leave them at a logic low so the pins are inactive when not used. This is useful if the devices are applied as standard DACs without the need for video controls or if less than 8-bits are used.

The HDAC10180 is usually configured in the synchronous mode. In this mode, the controls and data are synchronized to prevent pixel dropout. This reduces screen-edge distortions and provides the lowest output noise while maintaining the highest conversion rate. By leaving the Feedthrough (FT) control open (low), each rising edge of the convert (CONV) clock latches decoded data and control values into a D-type internal register. The registered data is then converted into the appropriate analog output by the switched current sinks. When FT is tied high, the control inputs and data are not registered. The analog output asynchronously tracks the input data and video controls. Feedthrough itself is asynchronous and usually used as a DC control.

The controls and data have to be present at the input pins for a set-up time of t_s before, and a hold time of t_h after the rising edge of the clock (CONV) in order to be synchronously registered. The set-up and hold times are not important in the asynchronous mode. The minimum pulse widths high (t_{PWH}) and low (t_{PWL}) as well as settling time become the limiting factors (see Figure 2).

Figure 2 - Timing Diagram

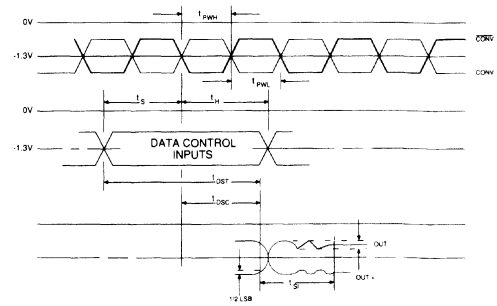


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Table II - Video Control Operation (Output values for Set-up = 10 IRE and 75 Ohm standard load)

Sync	Blank	Ref White	Bright	Data Input	Out - (mA)	Out - (V)	Out - (IRE)	Description
1	X	X	X	X	28.57	-1.071	-40	Sync Level
0	1	X	X	X	20.83	-0.781	0	Blank Level
0	0	1	1	X	0.00	0.000	110	Enhanced High Level
0	0	1	0	X	1.95	-0.073	100	Normal High Level
0	0	0	0	000...	19.40	-0.728	7.5	Normal Low Level
0	0	0	0	111...	1.95	-0.073	100	Normal High Level
0	0	0	1	000...	17.44	-0.654	17.5	Enhanced Low Level
0	0	0	1	111...	0.00	0.000	110	Enhanced High Level

The video controls produce the output levels needed for horizontal blanking, frame synchronization, etc., to be compatible with video system standards as described in RS-343-A. Table II shows the video control effects on the analog output. Internal logic governs Blank, Sync and Force High so that they override the data inputs as needed in video applications. Sync overrides both the data and other controls to produce full negative video output (Figure 8).

Reference white video level output is provided by Force High, which drives the internal digital data to full scale output or 100 IRE units. Bright gives an additional 10% of full scale value to the output level. This function can be used in graphic displays for highlighting menus, cursors or warning messages. Again, if the devices are used in non-video applications, the video controls can be left open.

CONVERT CLOCK

For best performance, the clock should be ECL driven, differentially, by utilizing CONV and $\overline{\text{CONV}}$ (Figure 3). By driving the clock this way, clock noise and power supply/output intermodulation will be minimized. The rising edge of the clock synchronizes the data and control inputs to the HDAC10180. Since the actual switching threshold of $\overline{\text{CONV}}$ is determined by CONV, the clock can be driven single-ended by connecting a bias voltage to $\overline{\text{CONV}}$. The switching threshold of CONV is set by this bias voltage.

ANALOG OUTPUTS

The HDAC10180 has two analog outputs that are high impedance, complementary current sinks. The outputs vary in proportion to the input data, controls and reference current values so that the full scale output can be changed by setting I_{REF} as mentioned earlier.

In video applications, the outputs can drive a doubly terminated 50 or 75 Ohm load to standard video levels. In the standard configuration of Figure 4, the output voltage is the product of the output current and load impedance and is between 0 and -1.07 V. The OUT - output (Figure 8) will provide a video output waveform with the SYNC pulse bottom at the -1.07 V level. The OUT + is inverted with SYNC up.

Figure 3 - CONVert, CONVert Switching Levels

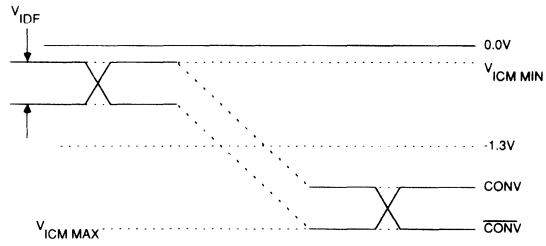


Figure 4A - Standard Load

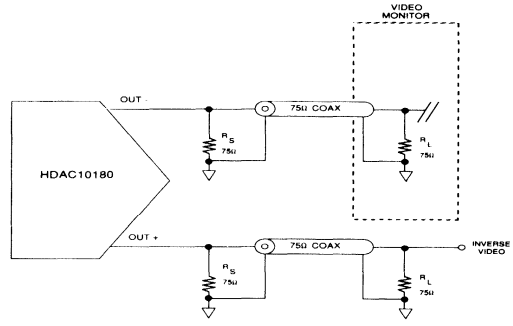
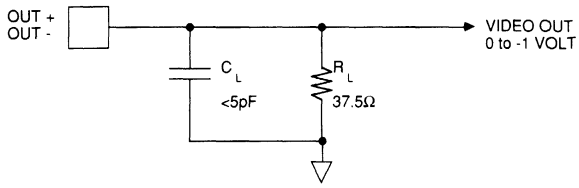


Figure 4B - Test Load



TYPICAL RGB GRAPHICS SYSTEM

In an RGB graphics system, the color displayed is determined by the combined intensities of the red, green and blue (RGB) D/A converter outputs. A change in gain or offset in any of the RGB outputs will affect the apparent hue displayed on the CRT screen.

Thus, it is very important that the outputs of the D/A converters track each other over a wide range of operating conditions. Since the D/A output is proportional to the product of the reference and digital input code, a common reference should be used to drive all three D/As in an RGB system to minimize RGB DAC-to-DAC mismatch. This may also eliminate the need for individual calibration of each DAC during production assembly.

The HDAC10181 contains an internal precision bandgap reference which completely eliminates the need for an external reference. The reference can supply up to 50 µA to an external load, such as two other DAC reference inputs. (See HDAC10181 Data Sheet).

The circuits shown in Figure 5 illustrate how a single HDAC10181 may be used as a master reference in a system with multiple DACs (such as RGB). The other DACs are simply slaved from the HDAC10181's reference output. The HDAC10180s shown are especially well-suited to be slaved to a 10181 for a better TC tracking from DAC-to-DAC, since they are essentially 10181s without the reference. The 10180 is pin-compatible with the TDC1018, which does not have an internal reference. Although either the TDC1018 or HDAC10180 may be slaved from an HDAC10181, the higher performance HDAC10180 and the above mentioned DAC-to-DAC TC tracking is the best choice for new designs.

No external reference is required for operation of the HDAC10181, as this function is provided internally. The internal reference is a bandgap type and is suitable for operation over extended temperature ranges. The HDAC10180 must use an external reference.

Figure 5 - Typical RGB Graphics System

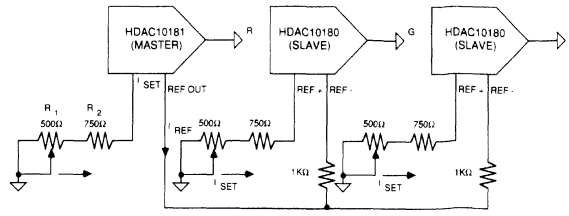


Figure 6 - Burn-In Circuit

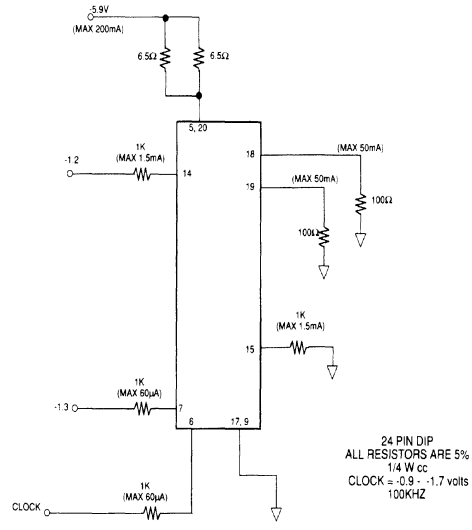


Figure 7 - DAC Output Circuit

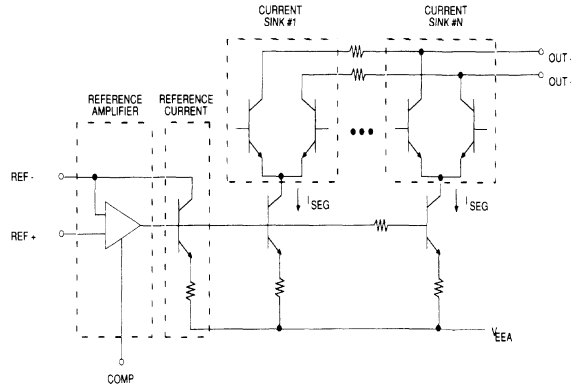


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Figure 8 - Video Output Waveform for Standard Load

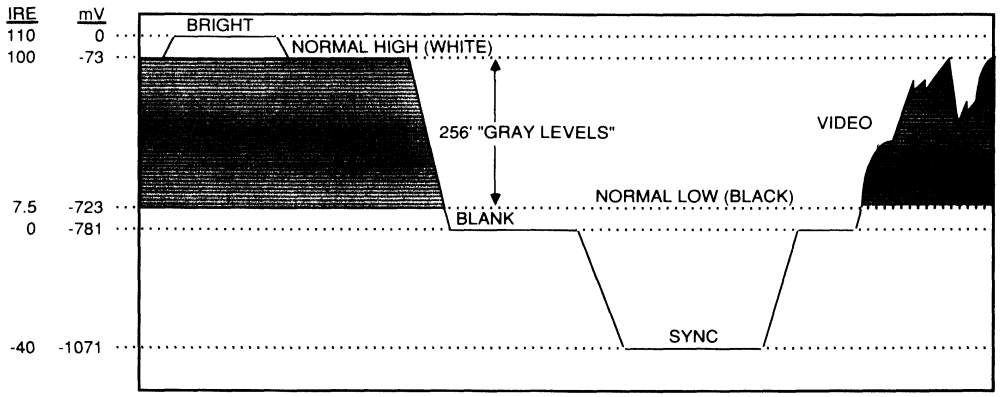
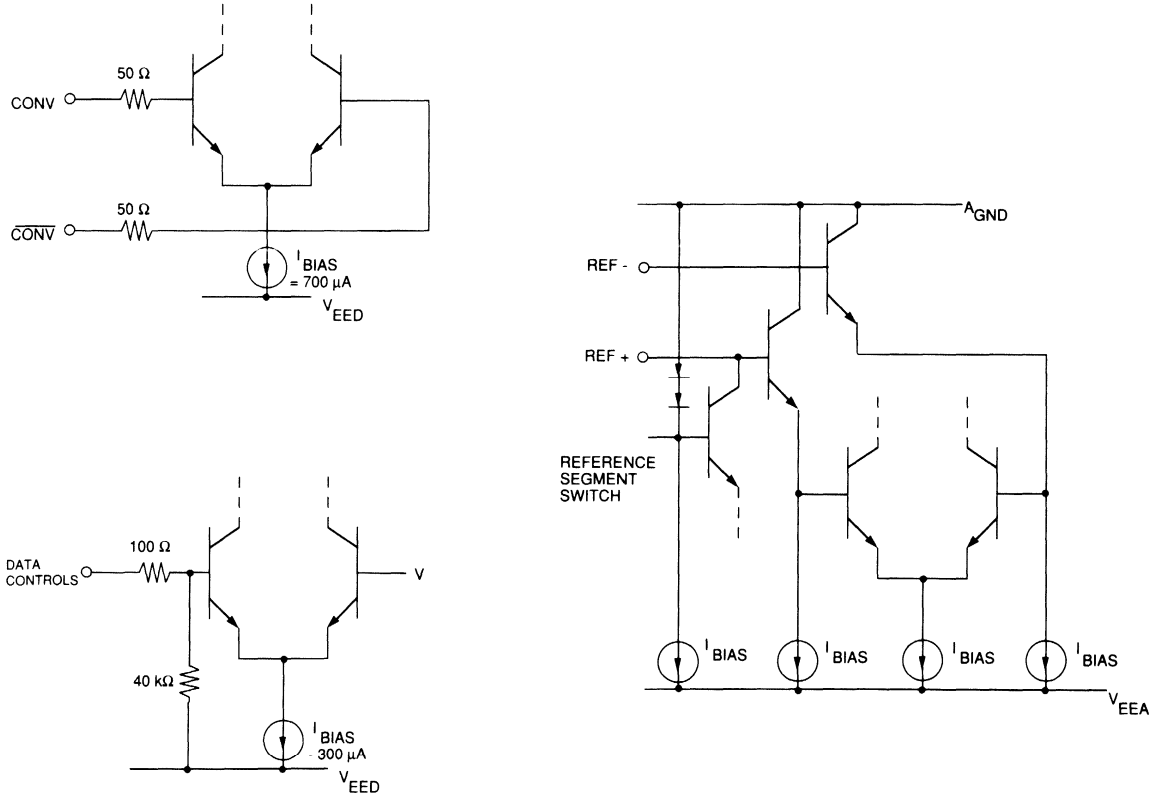
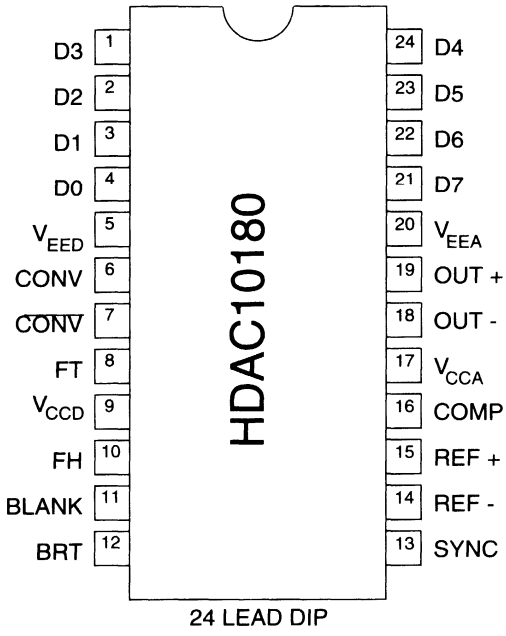


Figure 9 - Equivalent Input Circuits - Data, Clock, Controls and Reference



PIN ASSIGNMENTS



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PIN FUNCTIONS

NAME	FUNCTION
$\overline{D3}$	Data Bit 3
$\overline{D2}$	Data Bit 2
$\overline{D1}$	Data Bit 1
$\overline{D0}$	Data Bit 0 (LSB)
$\overline{V_{EED}}$	Digital Negative Supply
$\overline{CONV}$	Convert Clock Input
$\overline{\overline{CONV}}$	Convert Clock Input Complement
$\overline{FT}$	Register Feedthrough Control
$\overline{V_{CCD}}$	Digital Positive Supply
$\overline{FH}$	Data Force High Control
$\overline{BLANK}$	Video Blank Input
$\overline{BRT}$	Video Bright Input
$\overline{SYNC}$	Video SYNC Input
$\overline{REF -}$	Reference Current - Input
$\overline{REF +}$	Reference Current + Input
$\overline{COMP}$	Compensation Input
$\overline{V_{CCA}}$	Analog Positive Supply
$\overline{OUT -}$	Output Current Negative
$\overline{OUT +}$	Output Current Positive
$\overline{V_{EEA}}$	Analog Negative Supply
$\overline{D7}$	Data Bit 7 (MSB)
$\overline{D6}$	Data Bit 6
$\overline{D5}$	Data Bit 5
$\overline{D4}$	Data Bit 4

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LEADERSHIP IN DATA CONVERSION AND SIGNAL PROCESSING

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SIGNAL PROCESSING TECHNOLOGIES

HDAC10181

8-BIT, HIGH SPEED D/A CONVERTER

FEATURES

- 275 MWPS Conversion Rate - A Version
- 165 MWPS Conversion Rate - B Version
- RS-323-A Compatible
- Complete Video Controls: Sync, Blank, Bright and Reference White (Force High)
- 10 KH, 100 kΩ ECL Compatible
- Single Power Supply
- Registered Data and Video Controls
- Differential Current Outputs
- Stable On-Chip Bandgap Reference

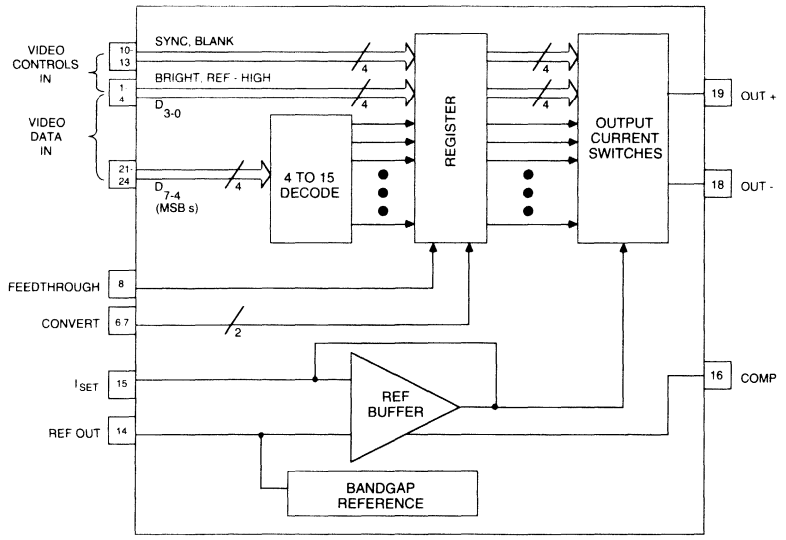
APPLICATIONS

- High Resolution Color or Monochrome Raster Graphics Displays
- Medical Electronics: CAT, PET, MR Imaging Displays
- CAD/CAE Workstations
- Solids Modeling
- General Purpose High-Speed D/A Conversion
- Digital Synthesizers
- Automated Test Equipment
- Digital Transmitters/Modulators

GENERAL DESCRIPTION

The HDAC10181 is a monolithic 8-bit digital-to-analog converter capable of accepting video data at a 165 or 275 MWPS rate. Complete with video controls (Sync, Blank, Reference White, [Force High] Bright), the HDAC10181 directly drives doubly-terminated 50 or 75 Ohm loads to standard composite video levels. Standard set-up level is 7.5 IRE. The HDAC10181 includes an internal precision bandgap reference which can drive two HDAC10180s in an RGB graphics system. The HDAC10181 contains data and control input registers, video control logic, reference buffer, and current switches in 24 Lead CERDIP package.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATING (Beyond which the useful life will be impaired)[1]

Supply Voltages

V_{EED} (measured to V_{CCD}) ..... -7.0 to 0.5 V
V_{EEA} (measured to V_{CCA}) ..... -7.0 to 0.5 V
V_{CCA} (measured to V_{CCD}) ..... -0.5 to 0.5 V

Input Voltages

CONV, Data, and Controls ..... V_{EED} to 0.5 V
(measured to V_{CCD})

I_{SET} (measured to V_{CCA}) ..... V_{EEA} to 0.5 V
REF OUT (measured to V_{CCA}) ..... V_{EEA} to 0.5 V

Temperature

Operating, ambient ..... -55 to + 125 °C
junction ..... + 175 °C
Lead, Soldering (10 seconds) ..... + 300 °C
Storage ..... -60 to + 150 °C

Note: 1. Operation at any Absolute Maximum Ratings is not implied. See Electrical Specifications for proper nominal applied conditions in typical applications.

ELECTRICAL SPECIFICATIONS

$V_{CCD} = V_{CCA}$ = ground, $V_{EEA} = V_{EED}$ = -5.2 V ±0.3 V, $T_A = T_{MIN}$ to T_{MAX}, C_C = 0 pF, I_{SET} = 1.105 mA

PARAMETERS	TEST CONDITIONS	TEST LEVEL	MIN	TYP	MAX	UNITS
DC ELECTRICAL CHARACTERISTICS						
Integral Linearity Error	1.0 mA<I_{SET}<1.3 mA	I	-.37 -.95		+.37 +.95	% Full Scale LSB
Differential Linearity Error	1.0 mA<I_{SET}<1.3 mA	I	-0.2 -0.5		+0.2 +0.5	% Full Scale LSB
Gain Error		I	-19		+19	% Full Scale
Gain Error Tempco		V		250		PPM/°C
Input Capacitance, I_{SET}, REF OUT		V		5		pF
Compliance Voltage, + Output		I	-1.2		1.5	V
Compliance Voltage, - Output		I	-1.2		1.5	V
Equivalent Output Resistance		I	20			K Ohm
Output Capacitance		V		12		pF
Maximum Current, + Output		IV	45			mA
Maximum Current, - Output		IV	45			mA
Output Offset Current		I			0.5	LSB
Input Voltage, Logic HIGH		I	-1.0			V
Input Voltage, Logic LOW		I			-1.5	V
Convert Voltage, Common Mode Range		I	-0.5		-2.5	V
Convert Voltage, Differential		IV	0.4		1.2	V
Input Current, Logic LOW, Data and Controls		I			120	µA
Input Current, Logic HIGH, Data and Controls		I		10	120	µA
Input Current, Convert		I		2	60	µA

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ELECTRICAL SPECIFICATIONS

$V_{CCD} = V_{CCA}$ = ground, $V_{EEA} = V_{EED}$ = -5.2 V ±0.3 V, $T_A = T_{MIN}$ to T_{MAX}, C_C = 0 pF, I_{SET} = 1.105 mA

PARAMETERS	TEST CONDITIONS	LEVEL	MIN	TYP	MAX	UNITS
DC ELECTRICAL CHARACTERISTICS						
Input Capacitance, Data and Controls		V		3		pF
Power Supply Sensitivity		I	-120		+120	µA/V
Supply Current		I		175	220	mA
DYNAMIC CHARACTERISTICS (R_L = 37.5 Ohms, C_L = 5 pF, T_A = 25 °C, I_{SET} = 1.105 mA)						
Maximum Conversion Rate	B Grade A Grade	III III	165 275			MWPS
Rise Time	10% to 90% G.S.	III			1.6	ns
Rise Time	10% to 90% G.S. R_L = 25 Ohms	IV		1.0		ns
Current Settling Time, Clocked Mode	To 0.2%	IV		7		ns
Current Settling Time, Clocked Mode	To 0.8%	IV		5.5		ns
Current Settling Time, Clocked Mode	To 0.2% R_L = 25 Ω	IV		4.5		ns
Clock to Output Delay, Clocked Mode		III			4	ns
Data and Output Delay, Transparent Mode		III			6	ns
Convert Pulse Width, LOW	B Grade A Grade	III III	3.0 1.8			ns
Glitch Energy	Area = 1/2 VT	V		10		pV-s
Convert Pulse Width, HIGH	B Grade A Grade	III III	3.0 1.8			ns ns
Reference Bandwidth, -3 dB		V		1		MHz
Set-up Time, Data and Controls		III	1.3	1.8	2	ns
Hold Time, Data and Controls		III	0.5			ns
Slew Rate	20% to 80% G.S.	III	400			V/µS
Clock Feedthrough		III			-48	dB

TEST LEVEL CODES

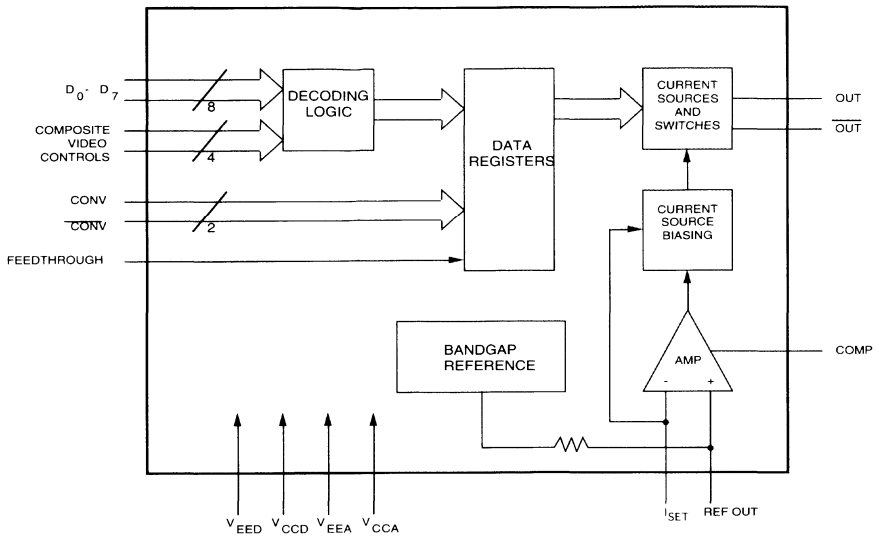
All electrical characteristics are subject to the following conditions:

All parameters having Min./Max. specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality Assurance inspection. Any blank section in the data column indicates that the specification is not tested at the specified condition.

Unless otherwise noted, all tests are pulsed tests, therefore $T_j = T_C = T_A$.

TEST LEVEL	TEST PROCEDURE
I	100% production tested at the specified temperature.
II	100% production tested at T_A = 25 °C, and sample tested at the specified temperatures.
III	QA sample tested only at the specified temperatures.
IV	Parameter is guaranteed (but not tested) by design and characterization data.
V	Parameter is a typical value for information purposes only.

FUNCTIONAL DIAGRAM



APPLICATION INFORMATION

The HDAC10181 is a high speed video Digital-to-Analog converter capable of up to 275 MWPS conversion rates. This makes the devices suitable for driving 1500 X 1800 pixel displays at 70 to 90 Hz update rates.

The HDAC10181 is separated into different conversion rate categories as shown in Table I.

The HDAC10181 has 10 KH and 100K ECL logic level compatible video control and data inputs. The complementary analog output currents produced by the devices are proportional to the product of the digital control and data inputs in conjunction with the analog reference current. The HDAC10181 is segmented so that the four MSBs of the input data are separated into a parallel "thermometer" code. From here, fifteen current sinks, which are identical, are driven to fabricate sixteen coarse output levels. The remaining four LSBs drive four binary weighted current switches. MSB currents are then summed with the LSBs, which provide a one-sixteenth of full scale contribution, to provide the 256 distinct analog output levels.

The video control inputs drive weighted current sinks which are added to the output current to produce composite video output levels. These controls, Sync, Blank, Reference White (Force High), and Bright are needed in video applications.

Another feature that similar video D/A converters do not have is the Feedthrough Control. This pin allows registered or unregistered operation between the video control inputs and data. In the registered mode, the composite functions are latched to the pixel data to prevent screen-edge distortions generally found on unregistered VIDEO DACs.

Table I - The HDAC10181 Family and Speed Designations

PART NUMBER	UPDATE	COMMENTS
HDAC10181A	275 MWPS	Suitable for 1200 X 1500 to 1500 X 1800 displays at 60 to 90 Hz update rate.
HDAC10181B	165 MWPS	Suitable for 1024 X 1280 to 1200 X 1500 displays at 60 to 90 Hz update rate.

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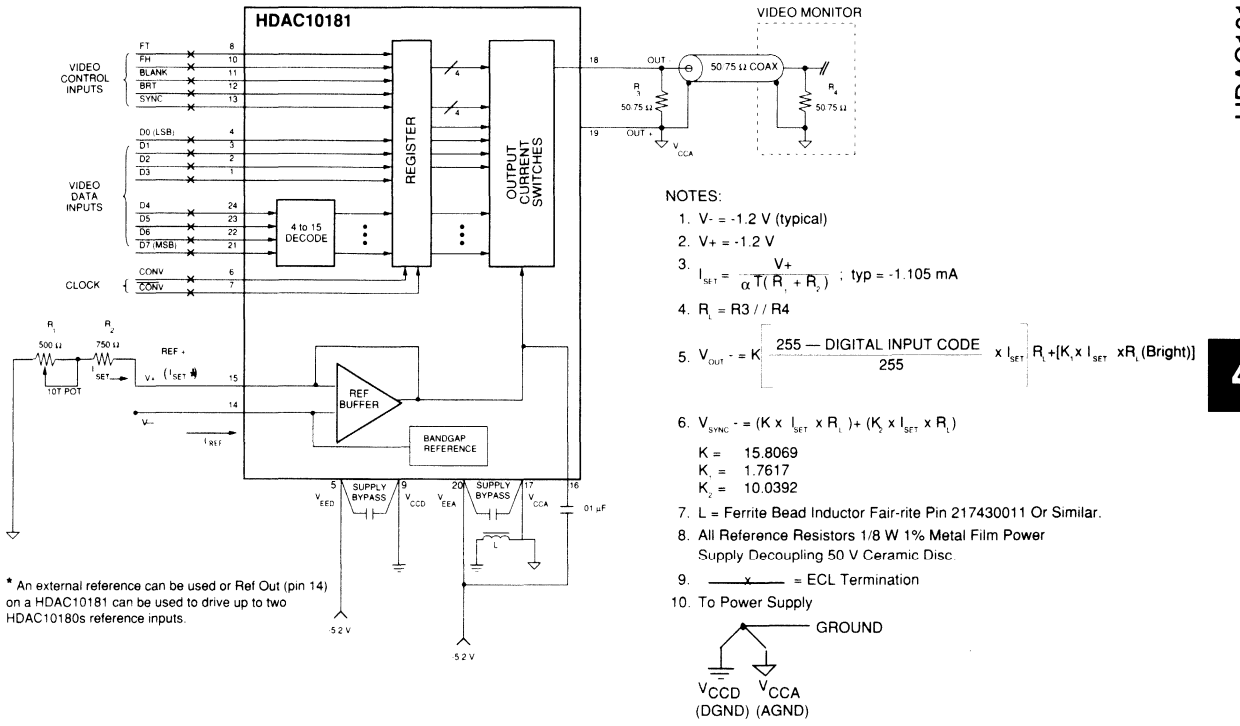
Figure 1 - Typical Interface Circuit



NOTES:

1. V- = -1.2 V (typical)
2. V+ = -1.2 V
3. $I_{SET} = \frac{V+}{\alpha T(R_1 + R_2)}$; typ = -1.105 mA
4. R_L = R3 // R4
5. $V_{OUT} - = K\left[\frac{255 - \text{DIGITAL INPUT CODE}}{255} \times I_{SET} \times R_L + [K_1 \times I_{SET} \times R_L(\text{Bright})]\right]$
6. $V_{SYNC} - = (K \times I_{SET} \times R_L) + (K_2 \times I_{SET} \times R_L)$

   K = 15.8069
   K_1 = 1.7617
   K_2 = 10.0392
7. L = Ferrite Bead Inductor Fair-rite Pin 217430011 Or Similar.
8. All Reference Resistors 1/8 W 1% Metal Film Power Supply Decoupling 50 V Ceramic Disc
9. —x— = ECL Termination
10. To Power Supply

TYPICAL INTERFACE CIRCUIT

GENERAL

A typical interface circuit using the HDAC10181 in a color raster application is shown in Figure 1. The HDAC10181 requires few external components and is extremely easy to use. The very high operating speeds of the HDAC10181 requires good circuit layout, decoupling of supplies, and proper design of transmission lines. The following are several considerations that should be noted to achieve best performance.

INPUT CONSIDERATIONS

Video input data and controls may be directly connected to the HDAC10181. Note that all ECL inputs are terminated as close to the device as possible to reduce ringing, crosstalk and reflections. A convenient and commonly used microstrip impedance is about 130 Ohms, which is easily terminated using a 330 Ohm resistor to V_{EE} and a 220 Ohm resistor to Ground. This arrangement gives a Thevenin equivalent termination of 130 Ohms to -2 Volts without the need for a -2 Volt supply. Standard SIP (Single Inline Package) 220/330 resistor networks are available for this purpose.

It is recommended that stripline or microstrip techniques be used for all ECL interface. Printed circuit wiring of known impedance over a solid ground plane is recommended. The ground plane should be constructed such that analog and digital ground currents are isolated as much as possible. The HDAC10181 provides separate digital and analog ground connections to simplify ground layout.

OUTPUT CONSIDERATIONS

The analog outputs are designed to directly drive a dual 50 or 75 Ohm load transmission system as shown. The source impedances of the HDAC10181 outputs are high impedance current sinks. The load impedance (R_L) must be 25 or 37.5 Ohms to attain standard RS-343-A video levels. Any deviation from this impedance will affect the resulting video output levels proportionally. As with the data interface, it is important that the analog transmission lines have matched impedance throughout, including connectors and transitions between printed wiring and coaxial cable. The combination of matched source termination resistor R_S and load terminator R_L minimizes reflections of both forward and reverse traveling waves in the analog transmission system. The return path for analog output current is V_{CCA} which is connected to the source termination resistor R_S.

POWER CONSIDERATIONS

The HDAC10181 operates from a single standard -5.2 Volt supply. Proper bypassing of the supplies will augment the HDAC10181 inherent supply noise rejection characteristics. As shown in Figure 1, a large tantalum capacitor in parallel with smaller ceramic capacitors is recommended for best performance. The small-valued capacitors should be connected as close to the device package as possible, whereas the tantalum capacitor may be placed up to a few inches away.

The HDAC10181 operates with separate analog (V_{EEA}) and digital (V_{EED}) power supplies to establish high noise immunity. Both supplies can eventually be connected to the same power source, but they should be individually decoupled as mentioned previously. The digital supply has a separate ground return which is V_{CCD}. The analog supply return is V_{CCA}. All power and ground pins must be connected in any application. If a +5 V power source is required, the ground pins V_{CCD} and V_{CCA} become the positive supply pins while V_{EED} and V_{EEA} become the ground returns. The relative polarities of the other voltages on inputs and outputs must be maintained.

REFERENCE CONSIDERATIONS

The HDAC10181 has one input (ISET) and one reference output (REF OUT). Both pins are connected to the inverting and noninverting inputs of an internal amplifier that serves as a reference buffer amplifier. The HDAC10181 has a bandgap reference connected internally to the inverting output of the buffer amplifier and the REF OUT.

The output of the buffer amplifier is the reference for the current sinks. The amplifier feedback loop is connected around one of the current sinks to achieve better accuracy. (See Figure 6.)

Since the analog output currents are proportional to the digital input data and the reference current (I_{SET}), the full-scale output may be adjusted by varying the reference current. I_{SET} is controlled through the I_{SET} input on the HDAC10181. A method and equations to set I_{SET} is shown in Figure 1. The HDAC10181 uses its own reference voltage for setting up I_{SET} as shown in Figure 1. The value for I_{SET} can be varied with the 500 Ohm trimmer to change the full scale output. A double 50 Ohm load (25 Ohm) can be driven if I_{SET} is increased 50% more than I_{SET} for doubly terminated 75 Ohm video applications.

COMPENSATION

The HDAC10181 provides an external compensation input (COMP) for the reference buffer amplifier. In order to use this pin correctly, a capacitor (C_C) should be connected between COMP and V_{EEA} as shown in Figure 1. Keep the lead lengths as short as possible. If the reference is to be kept as a constant, the C_C should be large (.01 µF). The value of C_C determines the bandwidth of the amplifier. If modulation of the reference is required, smaller values of C_C can be used to get up to a 1 MHz bandwidth.

DATA INPUTS AND VIDEO CONTROLS

The HDAC10181 has standard single-ended data inputs. The inputs are registered to produce the lowest differential data propagation delay (skew) to minimize glitching. There are also four video control inputs to generate composite video outputs. These are Sync, Blank, Bright and Reference White or Force High. Also provided is the Feedthrough control as mentioned earlier. The controls and data inputs are all 10 KH and 100K ECL compatible. In addition, all have internal pulldown resistors to leave them at a logic low so the pins are inactive when not used. This is useful if the devices are applied as standard DACs without the need for video controls or if less than 8-bits are used.

The HDAC10181 is usually configured in the synchronous mode. In this mode, the controls and data are synchronized to prevent pixel dropout. This reduces screen-edge distortions and provides the lowest output noise while maintaining the highest conversion rate. By leaving the Feedthrough (FT) control open (low), each rising edge of the convert (CONV) clock latches decoded data and control values into a D-type internal register. The registered data is then converted into the appropriate analog output by the switched current sinks. When FT is tied high, the control inputs and data are not registered. The analog output asynchronously tracks the input data and video controls. Feedthrough itself is asynchronous and usually used as a DC control.

The controls and data have to be present at the input pins for a set-up time of t_s before, and a hold time of t_h after the rising edge of the clock (CONV) in order to be synchronously registered. The set-up and hold times are not important in the asynchronous mode. The minimum pulse widths high (t_{PWH}) and low (t_{PWL}) as well as settling time become the limiting factors (see Figure 2).

Figure 2 - Timing Diagram

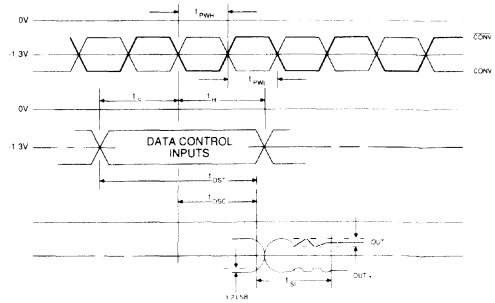


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Table II - Video Control Operation (Output values for Set-up = 10 IRE and 75 Ohm standard load)

Sync	Blank	Ref White	Bright	Data Input	Out - (mA)	Out - (V)	Out - (IRE)	Description
1	X	X	X	X	28.57	-1.071	-40	Sync Level
0	1	X	X	X	20.83	-0.781	0	Blank Level
0	0	1	1	X	0.00	0.000	110	Enhanced High Level
0	0	1	0	X	1.95	-0.073	100	Normal High Level
0	0	0	0	000...	19.40	-0.728	7.5	Normal Low Level
0	0	0	0	111...	1.95	-0.073	100	Normal High Level
0	0	0	1	000...	17.44	-0.654	17.5	Enhanced Low Level
0	0	0	1	111...	0.00	0.000	110	Enhanced High Level

The video controls produce the output levels needed for horizontal blanking, frame synchronization, etc., to be compatible with video system standards as described in RS-343-A. Table II shows the video control effects on the analog output. Internal logic governs Blank, Sync and Force High so that they override the data inputs as needed in video applications. Sync overrides both the data and other controls to produce full negative video output (Figure 8).

Reference white video level output is provided by Force High, which drives the internal digital data to full scale output or 100 IRE units. Bright gives an additional 10% of full scale value to the output level. This function can be used in graphic displays for highlighting menus, cursors or warning messages. Again, if the devices are used in non-video applications, the video controls can be left open.

CONVERT CLOCK

For best performance, the clock should be ECL drive, differentially, by utilizing CONV and $\overline{\text{CONV}}$ (Figure 3). By driving the clock this way, clock noise and power supply/output intermodulation will be minimized. The rising edge of the clock synchronizes the data and control inputs to the HDAC10181. Since the actual switching threshold of $\overline{\text{CONV}}$ is determined by CONV, the clock can be driven single-ended by connecting a bias voltage to $\overline{\text{CONV}}$. The switching threshold of CONV is set by this bias voltage.

ANALOG OUTPUTS

The HDAC10181 has two analog outputs that are high impedance, complementary current sinks. The outputs vary in proportion to the input data, controls and reference current values so that the full scales output can be changed by setting I_{REF} as mentioned earlier.

In video applications, the outputs can drive a doubly terminated 50 or 75 Ohm load to standard video levels. In the standard configuration of Figure 4, the output voltage is the product of the output current and load impedance and is between 0 and -1.07 V. The OUT - output (Figure 8) will provide a video output waveform with the SYNC pulse bottom at the -1.07 V level. The OUT + is inverted with SYNC up.

Figure 3 - CONVert, CONVert Switching Levels

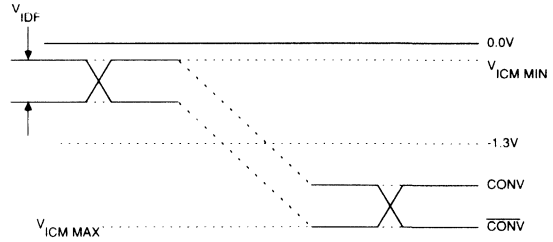


Figure 4A - Standard Load

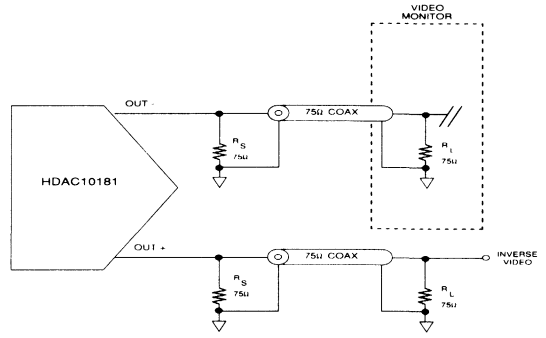
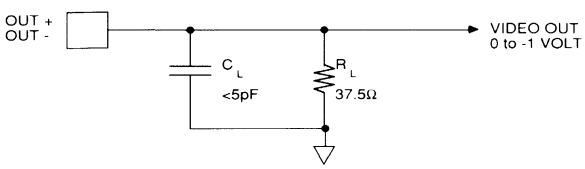


Figure 4B - Test Load



TYPICAL RGB GRAPHICS SYSTEM

In an RGB graphics system, the color displayed is determined by the combined intensities of the red, green and blue (RGB) D/A converter outputs. A change in gain or offset in any of the RGB outputs will affect the apparent hue displayed on the CRT screen.

Thus, it is very important that the outputs of the D/A converters track each other over a wide range of operating conditions. Since the D/A output is proportional to the product of the reference and digital input code, a common reference should be used to drive all three D/As in an RGB system to minimize RGB DAC-to-DAC mismatch. This may also eliminate the need for individual calibration of each DAC during production assembly.

The HDAC10181 contains an internal precision bandgap reference which completely eliminates the need for an external reference. The reference can supply up to 50 μA to an external load, such as two other DAC reference inputs.

The circuits shown in Figure 5 illustrate how a single HDAC10181 may be used as a master reference in a system with multiple DACs (such as RGB). The other DACs are simply slaved from the HDAC10181's reference output. The HDAC10180s shown are especially well-suited to be slaved to a 10181 for a better TC tracking from DAC-to-DAC, since they are essentially 10181s without the reference. The 10180 is pin-compatible with the TDC1018, which does not have an internal reference. Although either the TDC1018 or HDAC10180 may be slaved from an HDAC10181, the higher performance HDAC10180 and the above mentioned DAC-to-DAC TC tracking is the best choice for new designs. (See 10180 data sheet.)

No external reference is required for operation of the HDAC10181, as this function is provided internally. The internal reference is a bandgap type and is suitable for operation over extended temperature ranges. The HDAC10180 must use an external reference.

Figure 5 - Typical RGB Graphics System

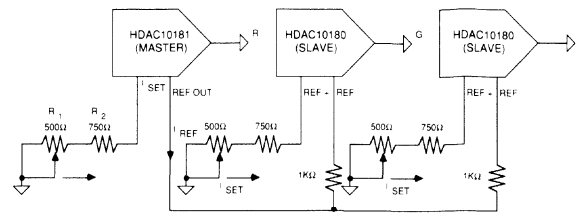


Figure 6 - Burn-In Circuit

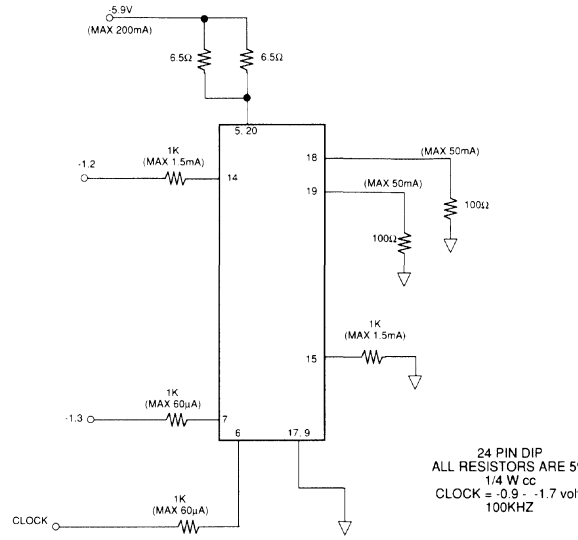


Figure 7 - DAC Output Circuit

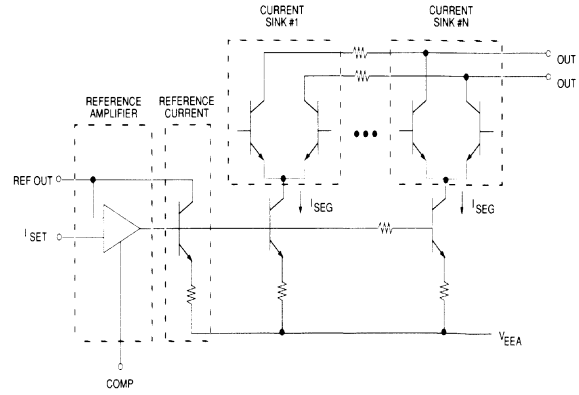


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Figure 8 - Video Output Waveform for Standard Load

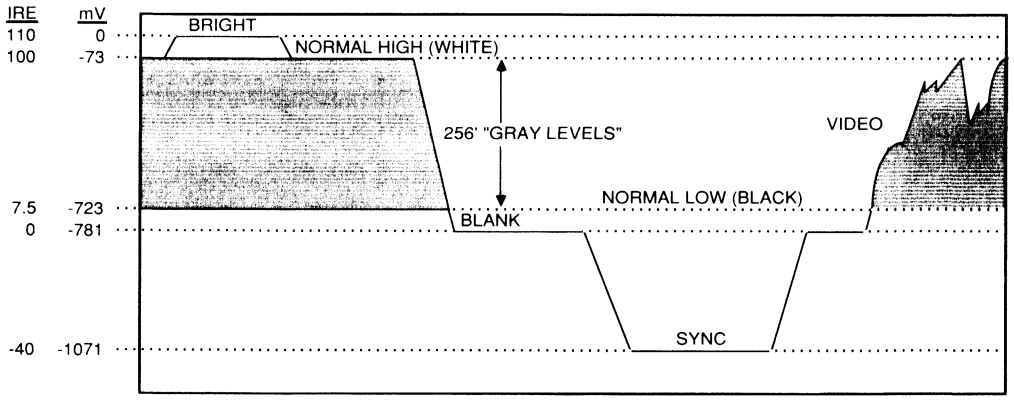
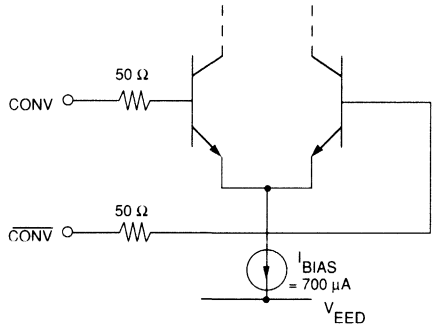
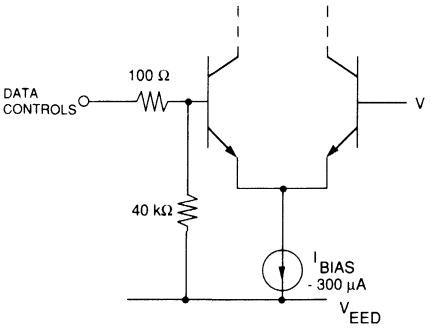
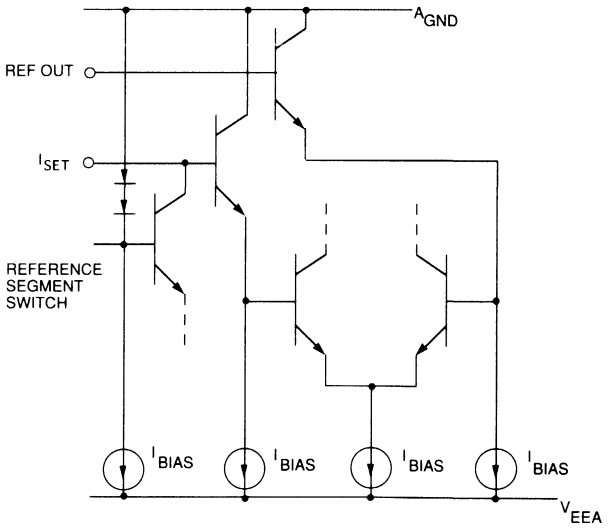


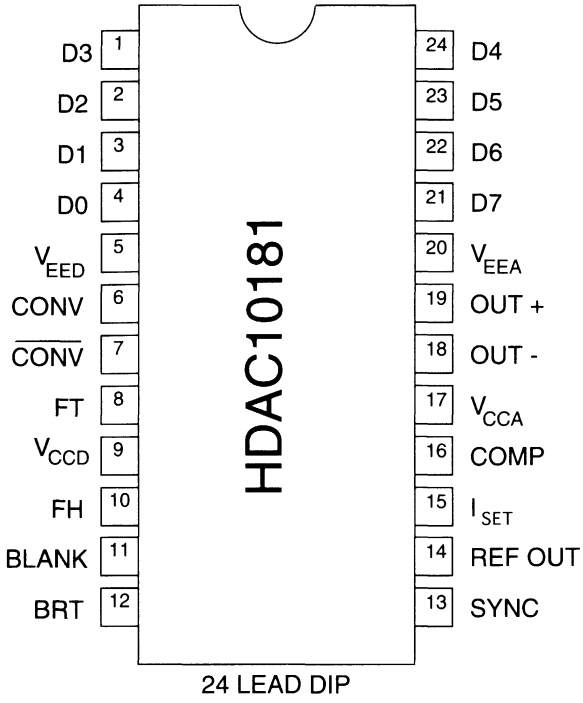
Figure 9 - Equivalent Input Circuits - Data, Clock, Controls and Reference







PIN ASSIGNMENTS



24 LEAD DIP

PIN FUNCTIONS

NAME	FUNCTION
$\overline{D3}$	Data Bit 3
$\overline{D2}$	Data Bit 2
$\overline{D1}$	Data Bit 1
$\overline{D0}$	Data Bit 0 (LSB)
$\overline{V_{EED}}$	Digital Negative Supply
$\overline{CONV}$	Convert Clock Input
$\overline{\overline{CONV}}$	Convert Clock Input Complement
$\overline{FT}$	Register Feedthrough Control
$\overline{V_{CCD}}$	Digital Positive Supply
$\overline{FH}$	Data Force High Control
$\overline{BLANK}$	Video Blank Input
$\overline{BRT}$	Video Bright Input
$\overline{SYNC}$	Video SYNC Input
$\overline{REF\ OUT}$	Reference Output
$\overline{I_{SET}}$	Reference Current + Input
$\overline{COMP}$	Compensation Input
$\overline{V_{CCA}}$	Analog Positive Supply
$\overline{OUT\ -}$	Output Current Negative
$\overline{OUT\ +}$	Output Current Positive
$\overline{V_{EEA}}$	Analog Negative Supply
$\overline{D7}$	Data Bit 7 (MSB)
$\overline{D6}$	Data Bit 6
$\overline{D5}$	Data Bit 5
$\overline{D4}$	Data Bit 4

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LEADERSHIP IN DATA CONVERSION AND SIGNAL PROCESSING

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SPT
SIGNAL PROCESSING TECHNOLOGIES

HDAC51400

8-BIT, ULTRAHIGH SPEED D/A CONVERTER

FEATURES

- 400 MWPS Nominal Conversion Rate
- RS-323-A Compatible
- Complete Video Controls: Sync, Blank, Bright and Reference White (Force High)
- 10 KH, 100K ECL Compatible
- Single Power Supply
- Registered Data and Video Controls
- Differential Current Outputs
- Stable On-Chip Bandgap Reference
- 50 and 75 Ohm Output Drive

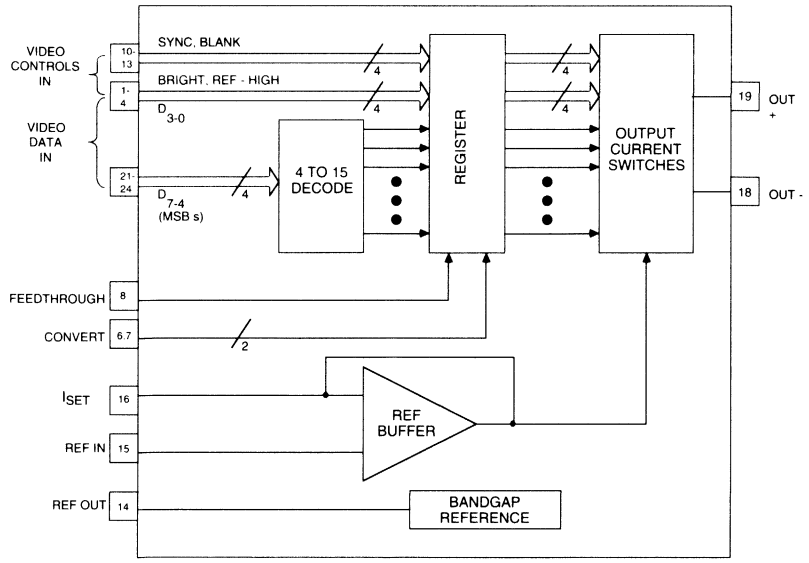
APPLICATIONS

- Raster Graphics
- High Resolution Color or Monochrome Displays to 2k x 2k Pixels
- Medical Electronics: CAT, PET, MR Imaging Displays
- CAD/CAE Workstations
- Solids Modeling
- General Purpose High-Speed D/A Conversion
- Digital Synthesizers
- Automated Test Equipment
- Digital Transmitters/Modulators

GENERAL DESCRIPTION

The HDAC51400 is a monolithic 8-bit digital-to-analog converter capable of accepting video data at a 400 MWPS. Complete with video controls (Sync, Blank, Reference White, [Force High] Bright), the HDAC51400 directly drives doubly-terminated 50 or 75 Ohm loads to standard composite video levels. Standard set-up level is 7.5 IRE. The HDAC51400 includes an internal precision bandgap reference which can drive two other HDAC51400s in an RGB graphics system. The HDAC51400 contains data and control input registers, video control logic, reference buffer, and current switches in a 24 Lead CERDIP package.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATING (Beyond which the useful life will be impaired)[1]

Supply Voltages

V_{EED} (measured to V_{CCD}) ..... -7.0 to 0.5 V
V_{EEA} (measured to V_{CCA}) ..... -7.0 to 0.5 V
V_{CCA} (measured to V_{CCD}) ..... -0.5 to 0.5 V

Input Voltages

CONV, Data, and Controls (measured to V_{CCD}) ..... V_{EED} to 0.5 V

REF+ (measured to V_{CCA}) ..... V_{EEA} to 0.5 V
REF– (measured to V_{CCA}) ..... V_{EEA} to 0.5 V

Temperature

Operating, ambient ..... -55 to + 125 °C
junction ..... + 175 °C
Lead, Soldering (10 seconds) ..... + 300 °C
Storage ..... -60 to + 150 °C

Note: 1. Operation at any Absolute Maximum Ratings is not implied. See Electrical Specifications for proper nominal applied conditions in typical applications.

ELECTRICAL SPECIFICATIONS

V_{CCD}=V_{CCA} = ground, V_{EEA} = V_{EED} = -5.2 V ±0.3 V, T_A = T_{MIN} to T_{MAX}, C_C = 0 pF, I_{SET} = 1.105 mA

PARAMETERS	TEST CONDITIONS	TEST LEVEL	MIN	TYP	MAX	UNITS
DC ELECTRICAL CHARACTERISTICS						
Integral Linearity Error	1.0 mA<I_{SET}<1.3 mA	I	-.37 -.95		+.37 +.95	% Full Scale LSB
Differential Linearity Error	1.0 mA<I_{SET}<1.3 mA	I	-0.2 -0.5		+0.2 +0.5	% Full Scale LSB
Gain Error		I	-6.5		+6.5	% Full Scale
Gain Error Tempco		IV		150		PPM/°C
Bandgap Tempco		IV		100		PPM/°C
Input Capacitance, I_{SET}, REF OUT		V		5		pF
Compliance Voltage, + Output		I	-1.2		1.5	V
Compliance Voltage, - Output		I	-1.2		1.5	V
Equivalent Output Resistance		I	20			kΩ
Output Capacitance		V		9		pF
Maximum Current, + Output		IV	45			mA
Maximum Current, - Output		IV	45			mA
Output Offset Current		I			0.5	LSB
Input Voltage, Logic HIGH		I	-1.0			V
Input Voltage, Logic LOW		I			-1.5	V
Convert Voltage, Common Mode Range		I	-0.5		-2.5	V
Convert Voltage, Differential		IV	0.4		1.2	V
Input Current, Logic LOW, Data and Controls		I			120	µA
Input Current, Logic HIGH, Data and Controls		I		10	120	µA
Input Current, Convert		I		2	60	µA
Reference Voltage Measured to V_{CCA}		IV		-1.2		V
Reference Output Current		I	-50			µA

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ELECTRICAL SPECIFICATIONS

V_{CCD}=V_{CCA} = ground, V_{EEA}

PARAMETERS	TEST CONDITIONS	LEVEL	MIN	TYP	MAX	UNITS
DC ELECTRICAL CHARACTERISTICS						
Input Capacitance, Data and Controls		V		3		pF
Power Supply Sensitivity		I	-120		+120	µA/V
Supply Current		I		175	220	mA
DYNAMIC CHARACTERISTICS (R_L = 37.5 Ohms, C_L = 5 pF, T_A=+25 °C, I_{SET}=1.105 mA)						
Maximum Conversion Rate		IV	385	400		MWPS
Rise Time	10% to 90% G.S.	IV			900	ps
Rise Time	10% to 90% G.S. R_L = 25 Ohms	IV			600	ps
Current Settling Time, Clocked Mode	To 0.2% G.S.	IV		4		ns
Current Settling Time, Clocked Mode	To 0.2% R_L = 25 Ω	IV		3		ns
Clock to Output Delay, Clocked Mode		III			4	ns
Data and Output Delay, Transparent Mode		III			6	ns
Convert Pulse Width, LOW		IV		1.25		ns
Glitch Energy	Area = 1/2 VT	V		10		pV-s
Convert Pulse Width, HIGH		III		1.25		ns
Reference Bandwidth, -3 dB		V		1.25		MHz
Set-up Time, Data and Controls		III		1		ns
Hold Time, Data and Controls		III	0.	-200		ps
Slew Rate	20% to 80% G.S.	V		700		V/µS
Clock Feedthrough		III			-48	dB

TEST LEVEL CODES

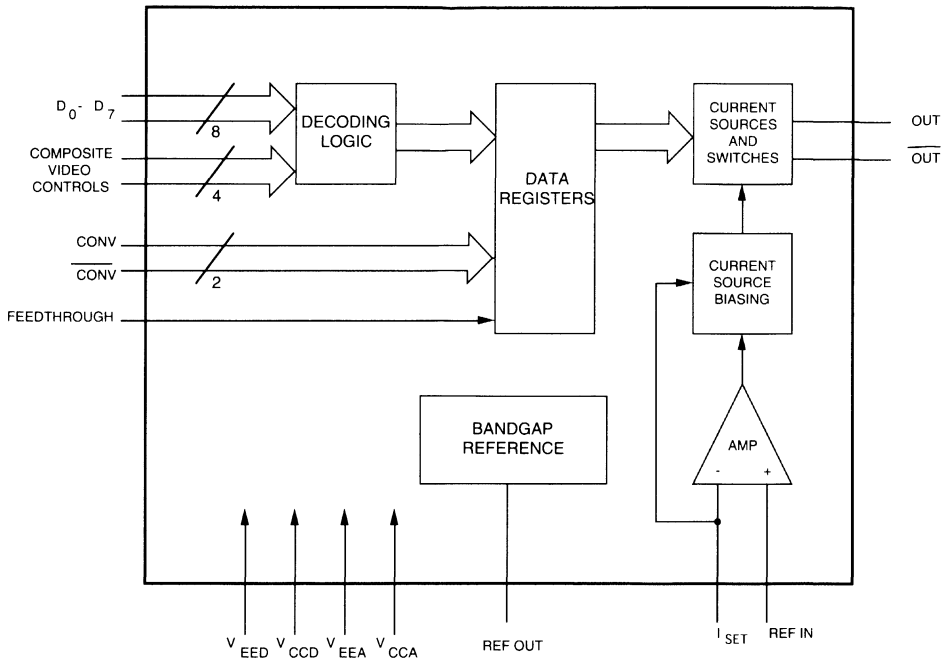
All electrical characteristics are subject to the following conditions:

All parameters having Min./Max. specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality Assurance inspection. Any blank section in the data column indicates that the specification is not tested at the specified condition.

Unless otherwise noted, all tests are pulsed tests, therefore $T_j = T_C = T_A$.

TEST LEVEL	TEST PROCEDURE
I	100% production tested at the specified temperature.
II	100% production tested at T_A = 25 °C, and sample tested at the specified temperatures.
III	QA sample tested only at the specified temperatures.
IV	Parameter is guaranteed (but not tested) by design and characterization data.
V	Parameter is a typical value for information purposes only.

FUNCTIONAL DIAGRAM



APPLICATION INFORMATION

The HDAC51400 is a high speed video Digital-to-Analog converter capable of up to 400 MWPS conversion rates. This makes the devices suitable for driving 2048 X 2048 pixel displays at 60 to 90 Hz update rates.

In addition, the HDAC51400 includes an internal bandgap reference which may be used to drive two other HDAC51400s if desired.

The HDAC51400 has 10KH and 100K ECL logic level compatible video control and data inputs. The complementary analog output currents produced by the devices are proportional to the product of the digital control and data inputs in conjunction with the analog reference current. The HDAC51400 is segmented so that the four MSBs of the input data are separated into a parallel "thermometer" code. From here, fifteen current sinks, which are identical, are driven to fabricate sixteen coarse output levels. The remaining four LSBs drive four binary weighted current switches.

MSB currents are then summed with the LSBs, which provide a one-sixteenth of full scale contribution, to provide the 256 distinct analog output levels.

The video control inputs drive weighted current sinks which are added to the output current to produce composite video output levels. These controls, Sync, Blank, Reference White (Force High), and Bright are needed in video applications.

Another feature that similar video D/A converters do not have is the Feedthrough Control. This pin allows registered or unregistered operation between the video control inputs and data. In the registered mode, the composite functions are latched to the pixel data to prevent screen-edge distortions generally found on unregistered VIDEO DACs.

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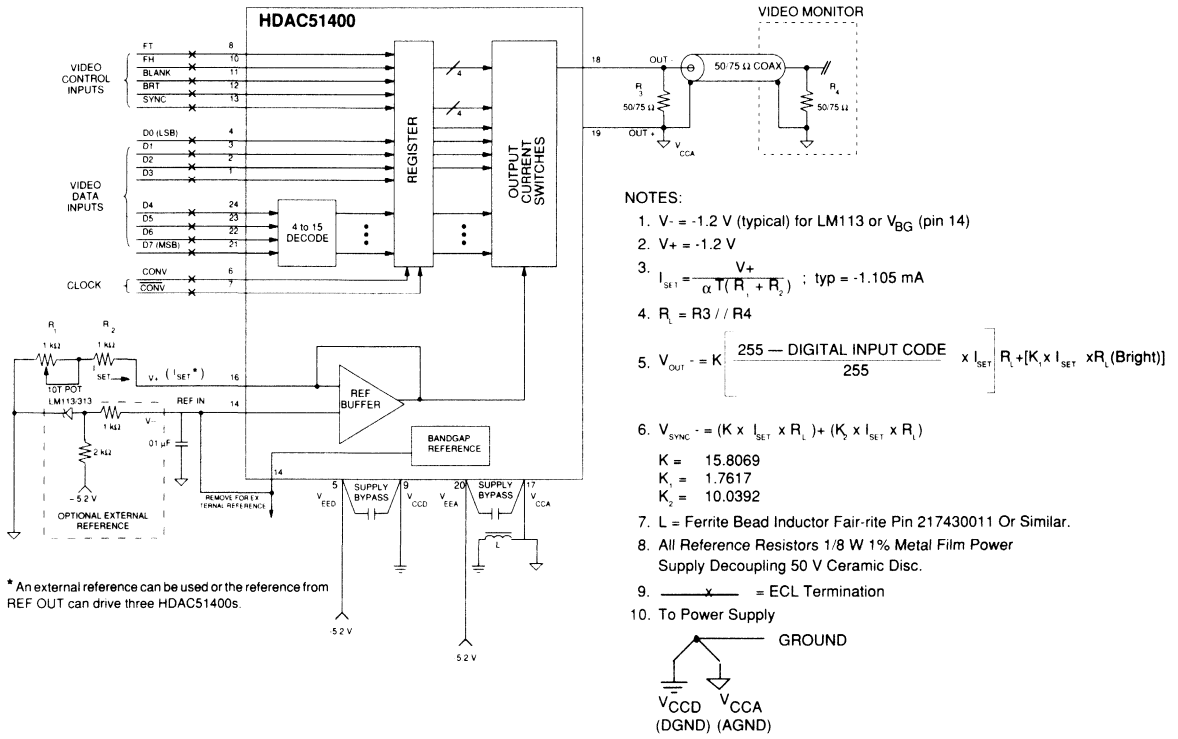
Figure 1 - Typical Interface Circuit



* An external reference can be used or the reference from REF OUT can drive three HDAC51400s.

NOTES:

1. V- = -1.2 V (typical) for LM113 or V_{BG} (pin 14)
2. V+ = -1.2 V
3. $I_{SET} = \frac{V+}{\alpha T(R_1 + R_2)}$; typ = -1.105 mA
4. R_L = R3 // R4
5. $V_{OUT} - = K\left[\frac{255 - \text{DIGITAL INPUT CODE}}{255} \times I_{SET}\right] R_L + [K_1 \times I_{SET} \times R_L(\text{Bright})]$
6. $V_{SYNC} - = (K \times I_{SET} \times R_L) + (K_2 \times I_{SET} \times R_L)$

   K = 15.8069
   K_1 = 1.7617
   K_2 = 10.0392
7. L = Ferrite Bead Inductor Fair-rite Pin 217430011 Or Similar.
8. All Reference Resistors 1/8 W 1% Metal Film Power
   Supply Decoupling 50 V Ceramic Disc.
9. ——x—— = ECL Termination
10. To Power Supply

TYPICAL INTERFACE CIRCUIT

GENERAL

A typical interface circuit using the HDAC51400 in a color raster application is shown in Figure 1. The HDAC51400 requires few external components and is extremely easy to use. The very high operating speeds of the HDAC51400 requires good circuit layout, decoupling of supplies, and proper design of transmission lines. The following are several considerations that should be noted to achieve best performance.

INPUT CONSIDERATIONS

Video input data and controls may be directly connected to the HDAC51400. Note that all ECL inputs are terminated as close to the device as possible to reduce ringing, crosstalk and reflections. A convenient and commonly used microstrip impedance is about 130 Ohms, which is easily terminated using a 330 Ohm resistor to V_{EE} and a 220 Ohm resistor to ground. This arrangement gives a Thevenin equivalent termination of 130 Ohms to -2 Volts without the need for a -2 Volt supply. Standard SIP (Single Inline Package) 220/330 resistor networks are available for this purpose.

It is recommended that stripline or microstrip techniques be used for all ECL interface. Printed circuit wiring of known impedance over a solid ground plane is recommended. The ground plane should be constructed such that analog and digital ground currents are isolated as much as possible. The HDAC51400 provides separate digital and analog ground connections to simplify ground layout.

OUTPUT CONSIDERATIONS

The analog outputs are designed to directly drive a doubly terminated 50 or 75 Ohm load transmission system as shown. The source impedances of the HDAC51400 outputs are high impedance current sinks. The load impedance (R_L) must be 25 or 37.5 Ohms to attain standard RS-343-A video levels. Any deviation from this impedance will affect the resulting video output levels proportionally. As with the data interface, it is important that the analog transmission lines have matched impedance throughout, including connectors and transitions between printed wiring and coaxial cable. The combination of matched source termination resistor R_S and load terminator R_L minimizes reflections of both forward and reverse traveling waves in the analog transmission system. The return path for analog output current is V_{CCA} which is connected to the source termination resistor R_S.

POWER CONSIDERATIONS

The HDAC51400 operates from a single standard -5.2 Volt supply. Proper bypassing of the supplies will augment the HDAC51400 inherent supply noise rejection characteristics. As shown in Figure 1, a large tantalum capacitor in parallel with smaller ceramic capacitors is recommended for best performance. The small-valued capacitors should be connected as close to the device package as possible, whereas the tantalum capacitor may be placed up to a few inches away.

The HDAC51400 operates with separate analog (V_{EEA}) and digital (V_{EED}) power supplies to establish high noise immunity. Both supplies can eventually be connected to the same power source, but they should be individually decoupled as mentioned previously. The digital supply has a separate ground return which is V_{CCD}. The analog supply return is V_{CCA}. All power and ground pins must be connected in any application. If a +5 V power source is required, the ground pins V_{CCD} and V_{CCA} become the positive supply pins while V_{EED} and V_{EEA} become the ground returns. The relative polarities of the other voltages on inputs and outputs must be maintained.

REFERENCE CONSIDERATIONS

The HDAC51400 has two reference inputs: REF IN and I_{SET}, and one reference output REF OUT. The input pins are connected to the inverting and noninverting inputs of an internal amplifier that serves as a reference buffer.

The output of the buffer amplifier is the reference for the current sinks. The amplifier feedback loop is connected around one of the current sinks to achieve better accuracy. (See Figure 7.)

Since the analog output currents are proportional to the digital input data and the reference current (I_{SET}), the full-scale output may be adjusted by varying the reference current. I_{SET} is controlled through the (I_{SET}) input on the HDAC51400. A method and equations to set I_{SET} are shown in Figure 1. The HDAC51400 can use an external negative voltage reference. The external reference must be stable to achieve a satisfactory output and the REF IN in should be driven through a resistor to minimize offsets caused by bias current. The value for I_{SET} can be varied with the 500 to 1k Ohm trimmer to change the full scale output. A double 50 Ohm load (25 Ohm) can be driven if I_{SET} is increased by 50% above for doubly-terminated 75 Ohm video applications.

DATA INPUTS AND VIDEO CONTROLS

The HDAC51400 has standard single-ended data inputs. The inputs are registered to produce the lowest differential data propagation delay (skew) to minimize glitching. There are also four video control inputs to generate composite video outputs. These are Sync, Blank, Bright and Reference White or Force High. Also provided is the Feedthrough control as mentioned earlier. The controls and data inputs are all 10 KH and 100K ECL compatible. In addition, all have internal pulldown resistors to leave them at a logic low so the pins are inactive when not used. This is useful if the devices are applied as standard DACs without the need for video controls or if less than 8-bits are used.

The HDAC51400 is usually configured in the synchronous mode. In this mode, the controls and data are synchronized to prevent pixel dropout. This reduces screen-edge distortions and provides the lowest output noise while maintaining the highest conversion rate. By leaving the Feedthrough (FT) control open (low), each rising edge of the convert (CONV) clock latches decoded data and control values into a D-type internal register. The registered data is then converted into the appropriate analog output by the switched current sinks. When FT is tied high, the control inputs and data are not registered. The analog output asynchronously tracks the input data and video controls. Feedthrough itself is asynchronous and usually used as a DC control.

The controls and data have to be present at the input pins for a set-up time of t_s before, and a hold time of t_H after the rising edge of the clock (CONV) in order to be synchronously registered. The set-up and hold times are not important in the asynchronous mode. The minimum pulse widths high (t_{PWH}) and low (t_{PWL}) as well as settling time become the limiting factors (see Figure 2).

Figure 2 - Timing Diagram

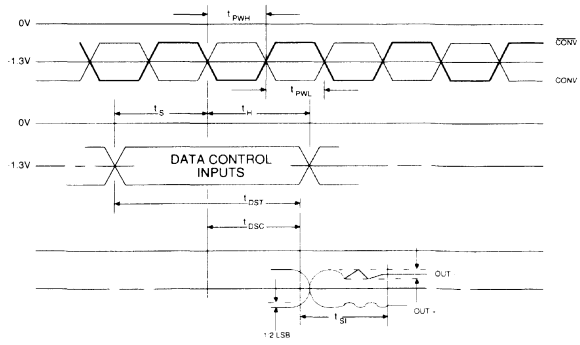


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Table I - Video Control Operation (Output values for Set-up = 10 IRE and 75 Ohm standard load)

Sync	Blank	Ref White	Bright	Data Input	Out - (mA)	Out - (V)	Out - (IRE)	Description
1	X	X	X	X	28.57	-1.071	-40	Sync Level
0	1	X	X	X	20.83	-0.781	0	Blank Level
0	0	1	1	X	0.00	0.000	110	Enhanced High Level
0	0	1	0	X	1.95	-0.073	100	Normal High Level
0	0	0	0	000...	19.40	-0.728	7.5	Normal Low Level
0	0	0	0	111...	1.95	-0.073	100	Normal High Level
0	0	0	1	000...	17.44	-0.654	17.5	Enhanced Low Level
0	0	0	1	111...	0.00	0.000	110	Enhanced High Level

The video controls produce the output levels needed for horizontal blanking, frame synchronization, etc., to be compatible with video system standards as described in RS-343-A. Table I shows the video control effects on the analog output. Internal logic governs Blank, Sync and Force High so that they override the data inputs as needed in video applications. Sync overrides both the data and other controls to produce full negative video output (Figure 8).

Reference white video level output is provided by Force High, which drives the internal digital data to full scale output or 100 IRE units. Bright gives an additional 10% of full scale value to the output level. This function can be used in graphic displays for highlighting menus, cursors or warning messages. Again, if the devices are used in non-video applications, the video controls can be left open.

CONVERT CLOCK

For best performance, the clock should be ECL drive, differentially, by utilizing CONV and $\overline{\text{CONV}}$ (Figure 3). By driving the clock this way, clock noise and power supply/output intermodulation will be minimized. The rising edge of the clock synchronizes the data and control inputs to the HDAC51400. Since the actual switching threshold of CONV is determined by $\overline{\text{CONV}}$, the clock can be driven single-ended by connecting a bias voltage to $\overline{\text{CONV}}$. The switching threshold of CONV is set by this bias voltage.

ANALOG OUTPUTS

The HDAC51400 has two analog outputs that are high impedance, complementary current sinks. The outputs vary in proportion to the input data, controls and reference current values so that the full scales output can be changed by setting I_{SET} as mentioned earlier.

In video applications, the outputs can drive a doubly terminated 50 or 75 Ohm load to standard video levels. In the standard configuration of Figure 4, the output voltage is the product of the output current and load impedance and is between 0 and -1.07 V. The OUT - output (Figure 8) will provide a video output waveform with the SYNC pulse bottom at the -1.07 V level. The OUT + is inverted with SYNC up.

Figure 3 - CONVert, $\overline{\text{CONV}}$ert Switching Levels

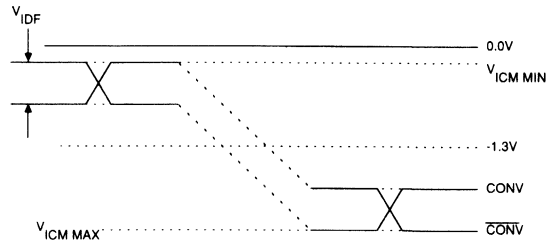


Figure 4A - Standard Load

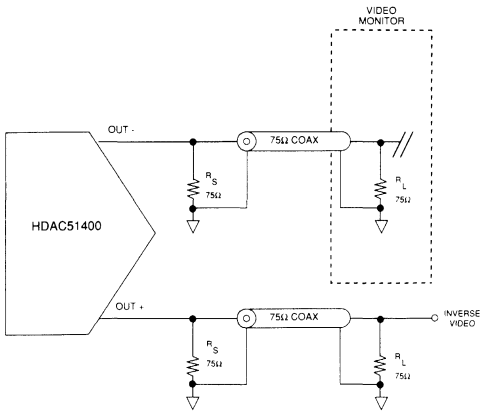
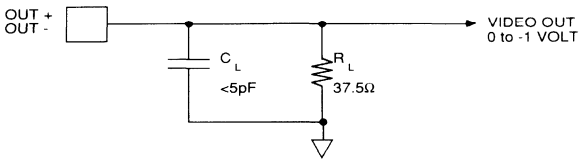


Figure 4B - Test Load



TYPICAL RGB GRAPHICS SYSTEM

In an RGB graphics system, the color displayed is determined by the combined intensities of the red, green and blue (RGB) D/A converter outputs. A change in gain or offset in any of the RGB outputs will affect the apparent hue displayed on the CRT screen.

Thus, it is very important that the outputs of the D/A converters track each other over a wide range of operating conditions. Since the D/A output is proportional to the product of the reference and digital input code, a common reference should be used to drive all three D/As in an RGB system to minimize RGB DAC-to-DAC mismatch. This may also eliminate the need for individual calibration of each DAC during production assembly.

The HDAC51400 contains an internal precision bandgap reference which completely eliminates the need for an external reference. The reference can supply up to 50 μA to an external load, such as two other DAC reference inputs.

The circuits shown in Figure 5 illustrate how a single HDAC51400 may be used as a master reference in a system with multiple DACs (such as RGB). The other DACs are simply slaved from the HDAC51400's reference output.

Figure 5 - Typical RGB Graphics System

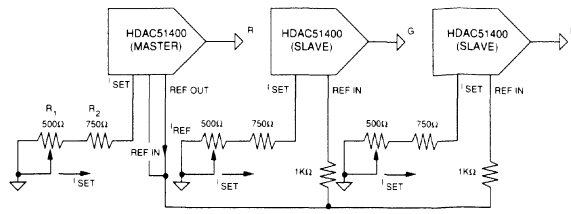


Figure 6 - Burn-In Circuit

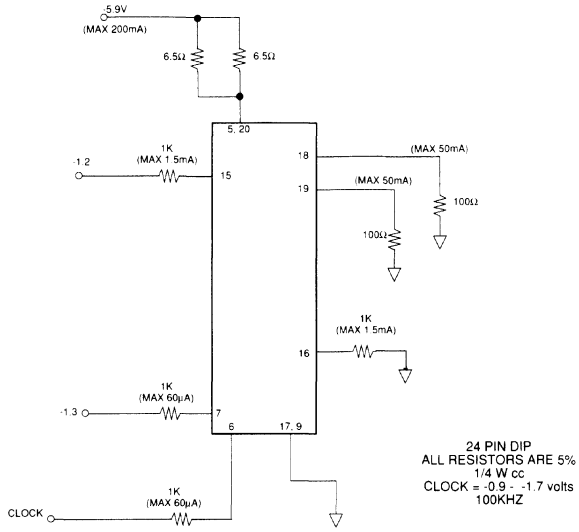


Figure 7 - DAC Output Circuit

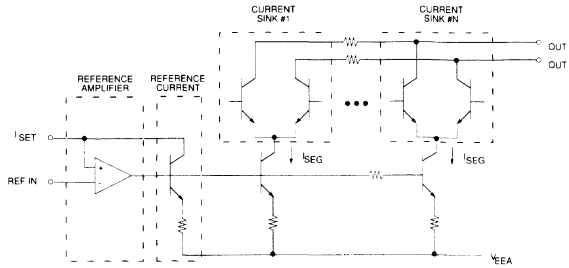


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Figure 8 - Video Output Waveform for Standard Load

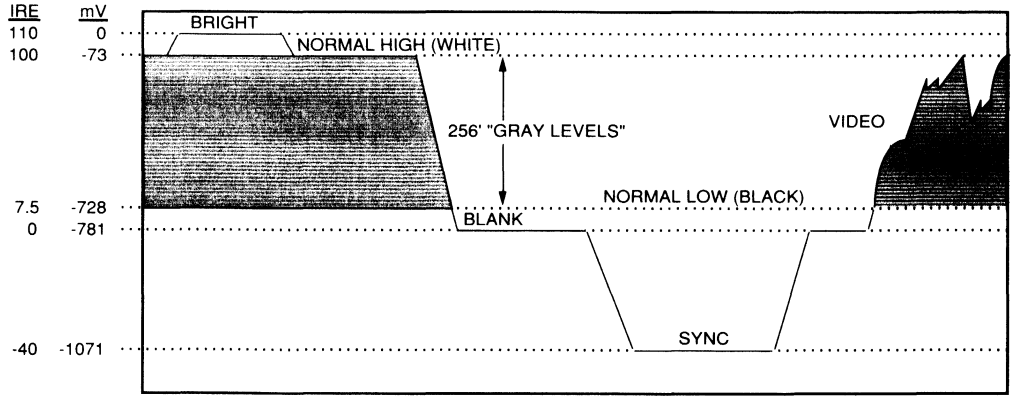
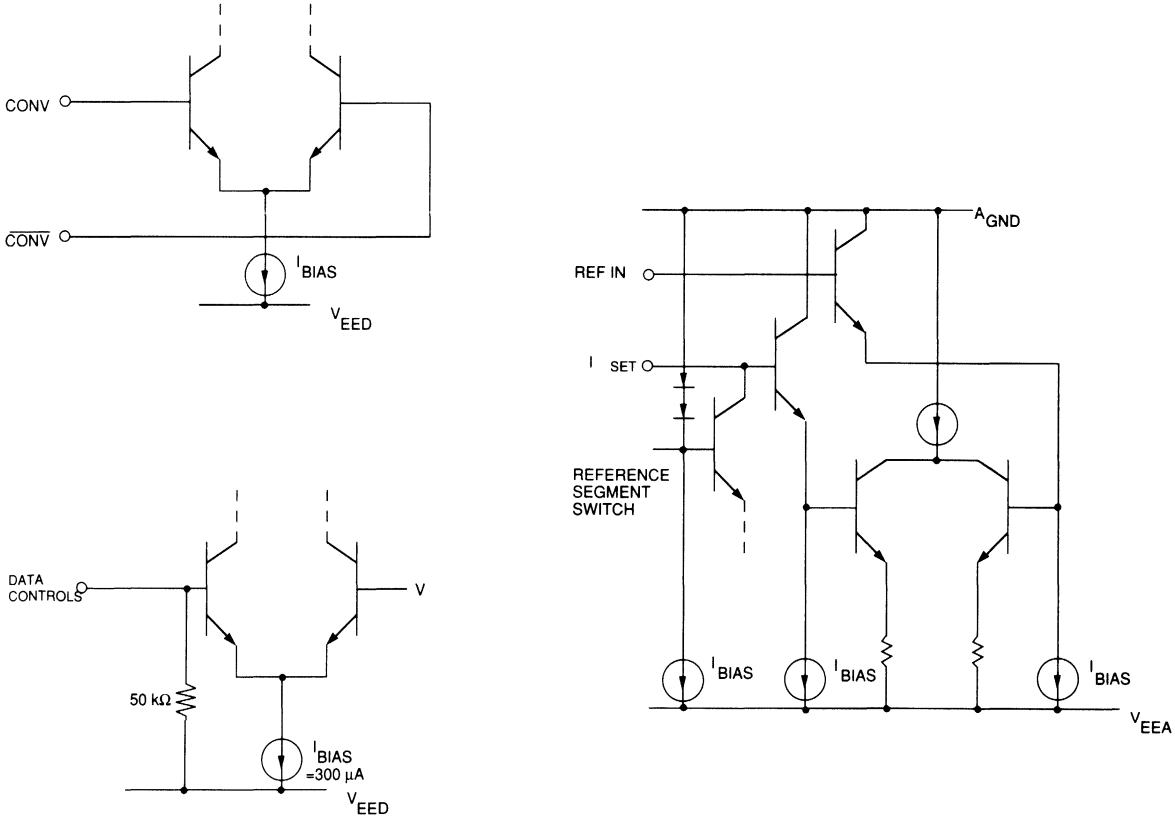
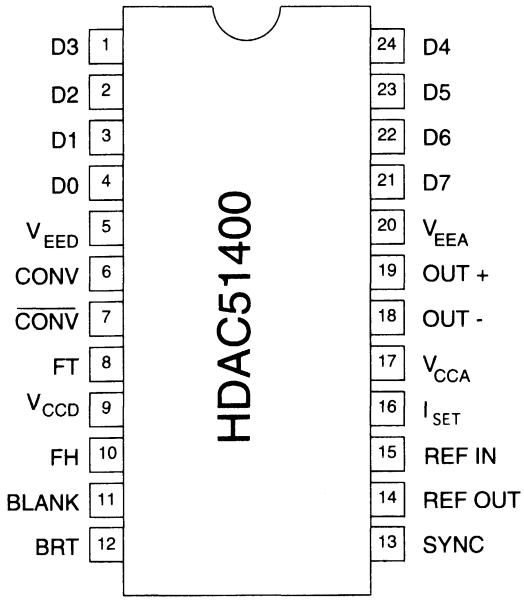


Figure 9 - Equivalent Input Circuits - Data, Clock, Controls and Reference



PIN ASSIGNMENTS



24-LEAD DIP

PIN FUNCTIONS

NAME	FUNCTION
$\overline{D3}$	Data Bit 3
$\overline{D2}$	Data Bit 2
$\overline{D1}$	Data Bit 1
$\overline{D0}$	Data Bit 0 (LSB)
V_{EED}	Digital Negative Supply
$\overline{CONV}$	Convert Clock Input
$\overline{\overline{CONV}}$	Convert Clock Input Complement
$\overline{FT}$	Register Feedthrough Control
V_{CCD}	Digital Positive Supply
$\overline{FH}$	Data Force High Control
$\overline{BLANK}$	Video Blank Input
$\overline{BRT}$	Video Bright Input
$\overline{SYNC}$	Video SYNC Input
$\overline{REF\ OUT}$	Reference Output
$\overline{REF\ IN}$	Reference Input
I_{SET}	Reference Current
V_{CCA}	Analog Positive Supply
$\overline{OUT\ -}$	Output Current Negative
$\overline{OUT\ +}$	Output Current Positive
V_{EEA}	Analog Negative Supply
$\overline{D7}$	Data Bit 7 (MSB)
$\overline{D6}$	Data Bit 6
$\overline{D5}$	Data Bit 5
$\overline{D4}$	Data Bit 4

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LEADERSHIP IN DATA CONVERSION AND SIGNAL PROCESSING

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SIGNAL PROCESSING TECHNOLOGIES

SPT5220

10-BIT, 80 MWPS VIDEO DAC

ADVANCE INFORMATION

FEATURES

- +5 V CMOS Monolithic Construction
- ±1 LSB Differential Linearity Error
- ±1 LSB Integral Linearity Error
- TTL-Compatible Inputs
- 80 MHz Pipelined Operation
- RS-343A/RS-170 Compatible Outputs
- 28-Pin DIP Package
- Typical Power Dissipation of 300 mW

APPLICATIONS

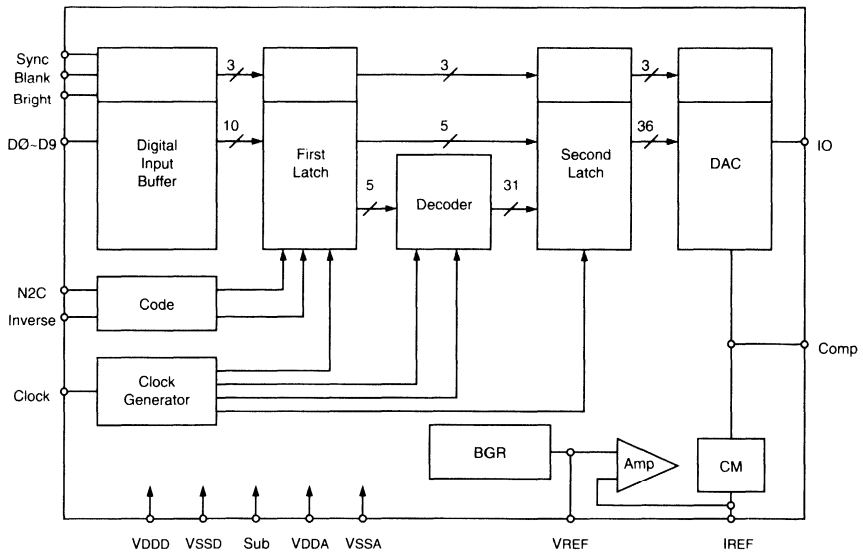
- High Resolution Color or Monochrome Raster Graphics Displays
- Medical Electronics: CAT, PET, MR Imaging Displays
- CAD/CAE Workstations
- Solids Modeling
- General Purpose High-Speed D/A Conversion
- Digital Synthesizers
- Automated Test Equipment
- Digital Transmitters/Modulators

GENERAL DESCRIPTION

The SPT5220 is a monolothic CMOS D/A converter for high-resolution color graphics and video systems. The device operates with a single +5 V power supply and all digital inputs are TTL/CMOS compatible. The data is straight binary.

The product generates doubly-terminated 75 Ω coax RS343A or 75 Ω cable RS170 compatible video output. The data latches minimize the data time skew and reduce the glitches that can adversely affect many applications.

BLOCK DIAGRAM



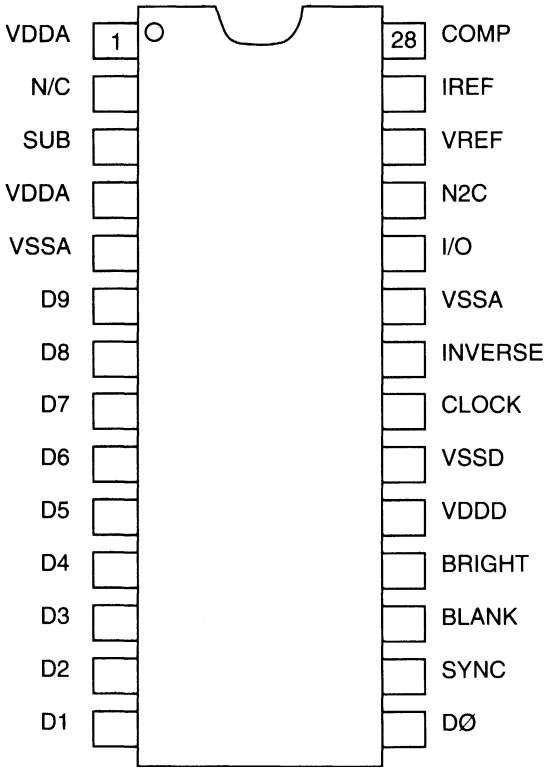
ABSOLUTE MAXIMUM RATINGS (Beyond which damage may occur)

ELECTRICAL SPECIFICATIONS

$T_A = T_{MIN}$ TO T_{MAX}, $V_{CC} = 5.0$ V, $V_{REF} = 1.2$ V

PARAMETERS	TEST CONDITIONS	TEST LEVEL	MIN	TYP	MAX	UNITS
Resolution			10			Bits
Linearity					1	LSB
Conversion Rate					80	MWPS
Glitch Impulse				50		pv-sec
Power Dissipation				300		mW

PIN ASSIGNMENTS



PIN FUNCTIONS

NAME	FUNCTION
VDDA	Analog Supply
N/C	No Connection
SUB	Substrate Power (Pad Connection to VDDA)
VDDA	Analog Supply
VSSA	Analog Ground
D9 ~ D0	Digital Inputs (D9=MSB, D0=LSB)
SYNC	Sync Signal Input
BLANK	Blank Signal Input
BRIGHT	Bright Signal Input
VDDD	Digital Supply
VSSD	Digital Ground
CLOCK	Clock Input
INVERSE	Inverse Signal Input
VSSA	Analog Ground
I/O	Analog Current Output
N2C	Not Two's Complement
IREF	Full-Scale Adjust Control
COMP	Compensation Pin

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LEADERSHIP IN DATA CONVERSION AND SIGNAL PROCESSING

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SIGNAL PROCESSING TECHNOLOGIES

HDAC52160

ULTRA-HIGH SPEED 16-BIT DAC

4

FEATURES

- Fast Settling Time - 150 nsec
- Excellent Linearity T. C. -1.5 ppm/°C
- On-Chip Band-Gap Voltage Reference
- On-Chip Application Resistors for Gain Selection
- TTL Compatible Inputs

APPLICATIONS

- High Speed Analog-to-Digital Converters
- Automatic Test Equipment
- Digital Attenuators
- Digital Communication Equipment
- Waveform Generators

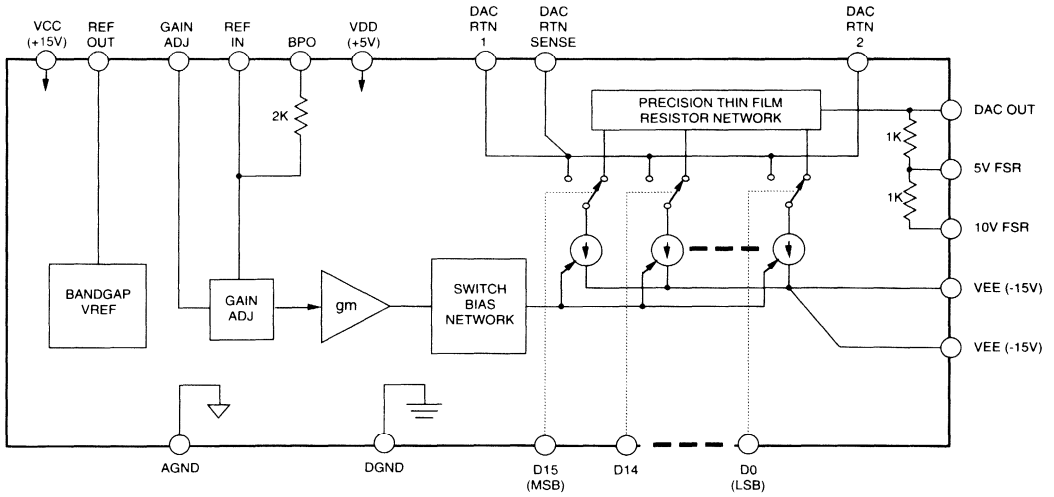
GENERAL DESCRIPTION

The HDAC52160 is a monolithic, high-performance, 16-bit digital-to-analog converter with unmatched speed and accuracy. With its 150 nanosecond settling time it is the highest speed 16-bit DAC in the industry. Unique features include the band-gap voltage reference and precision application resistors which greatly simplify device application. Unlike other high speed DACs, the HDAC52160 can be used in either a current-output or voltage-output mode.

The internal application resistors support output range selections of 0 to +10, 0 to +5, -5 to +5, and -2.5 to +2.5 volts. These internal resistors, used in conjunction with an external op amp, provide current-to-voltage conversion. Because of the high compliance voltage of the DAC output (+/- 2.5 volts), the HDAC52160 can also provide a direct voltage drive into a high impedance load without an external op amp.

The HDAC52160 operates with ±15 volt analog supplies, a separate +5 V digital supply and separate analog and digital grounds to provide maximum noise immunity. All logic input levels are TTL and 5 volt CMOS compatible. Laser-trimmed thin film technology ensures accuracy over time and environmental changes.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATING (Beyond which damage may occur) 25 °C (1)

Supply Voltages

V_{CC} to AGND ..... +18 V
V_{EE} to AGND ..... -18 V
V_{DD} to DGND ..... +6 V
AGND to DGND Differential ..... +0.5 V

Input Voltages

All Digital Inputs to DGND ..... -0.3 V to (V_{DD} +0.3 V)
REF IN to AGND ..... 0 to +10 V

Temperature

Temperature, Ambient ..... 0 to 70 °C
case ..... -60 to +140 °C
junction ..... +150 °C
Lead Temperature (soldering 10 seconds) ..... +300 °C
Storage Temperature ..... -65 to +100 °C

Note: 1. Operation at any Absolute Maximum Rating is not implied. See Electrical Specifications for proper nominal applied conditions in typical applications.

ELECTRICAL SPECIFICATIONS

T_A = 0 to +70 °C, V_{CC} = 15 V, V_{DD} = 5 V, V_{EE} = -15 V, unless otherwise specified. Minimum air flow is 50 LPM.

PARAMETER	TEST CONDITIONS	TEST LEVEL	HDAC52160B MIN	HDAC52160B TYP	HDAC52160B MAX	HDAC52160C MIN	HDAC52160C TYP	HDAC52160C MAX	UNIT
ACCURACY SPECIFICATIONS									
Integral Linearity Error	T_A=25 °C	I		±.0015	±.003		±.0015	±.003	%FSR
Integral Linearity Error	T_A=0 to 70 °C	I		±.0045	±.006		±.006	±.012	%FSR
Integral Linearity Drift	Drift	IV		±1.5			±2.0		PPM/°C
Differential Linearity Error	T_A=25 °C	I		±.003	±.006		±.003	±.006	%FSR
Differential Linearity Error	T_A=0 to 70 °C	I		±.009	±.012		±.012	±.024	%FSR
Differential Linearity Drift	Drift	IV		±2.5			±4.0		PPM/°C
Gain Error	T_A=25°C	I		±.03	±.15		±.03	±.15	%FSR
Gain Error		I		±.08	±.25		±.08	±.25	%FSR
Gain Error Drift		IV		±20			±20		PPM/°C
Unipolar Offset Error	T_A=25°C	I		±.02	±.1		±.02	±.1	%FSR
Unipolar Offset Error		I		±.02	±.3		±.02	±.3	%FSR
Bipolar Offset Error	T_A=25°C	I		±2.5	±10		±2.5	±10	mV
Bipolar Offset Error		I		±5	±15		±5	±15	mV
DAC OUTPUT SPECIFICATIONS									
I_{OUT}		V		5			5		mA
R_{OUT}		V		1k			1k		Ω
C_{OUT}	See Fig. 1	V		12			12		pF
Output Compliance[2]		V		±2.5			±2.5		V
Output Noise	BW = 1 MHz	V		40			40		µV RMS

Note 1: Operation at any Absolute Maximum Rating is not implied. See Electrical Specifications for proper nominal applied conditions in typical applications.
Note 2: Accuracy is not guaranteed beyond this limit.

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ELECTRICAL SPECIFICATIONS

T_A = 0 to +70 °C, V_{CC} = 15 V, V_{DD} = 5 V, V_{EE} = -15 V, unless otherwise specified. Minimum air flow is 50 LPM.

PARAMETER	TEST CONDITIONS	TEST LEVEL	HDAC52160B MIN	HDAC52160B TYP	HDAC52160B MAX	HDAC52160C MIN	HDAC52160C TYP	HDAC52160C MAX	UNIT
DYNAMIC SPECIFICATIONS									
Settling Time	to .0015%	V		150			150		ns
LOGIC SPECIFICATIONS									
V_{IH} 2		I	3.75			3.75			V
V_{IL} 2		I			1.5			1.5	V
I_{IH}		I		2	20		2	20	µA
I_{IL}		I		1	10		1	10	µA
REFERENCE									
Reference Output Voltage	T_A=25 °C	I	4.99	5	5.01	4.99	5	5.01	V
Reference Output Voltage		I	4.98	5	5.02	4.98	5	5.02	V
Max. Reference Output Load3	Total Current	V		8			8		mA
Output Noise4	BW = 1 MHz	V		40			40		µV RMS
POWER SUPPLIES									
V_{CC} Supply		I	14.25	15.00	15.75	14.25	15.00	15.75	V
V_{EE} Supply		I	-14.25	-15.00	-15.75	-14.25	-15.00	-15.75	V
V_{DD} Supply		I	4.75	5.00	5.25	4.75	5.00	5.25	V
V_{CC} Supply Current		I		4	6		4	6	mA
V_{EE} Supply Current		I		20	35		20	35	mA
V_{DD} Supply Current		I		6	9		6	9	mA
Power Dissipation		I		450	660		450	660	mW
PSRR, V_{CC}	+15 V±5%	V		.001			.001		%G/%PS
PSRR, V_{EE}	-15 V±5%	V		.01			.01		%G/%PS
PSRR, V_{DD}	+5 V±5%	V		.001			.001		%G/%PS

Note 3: Reference Load: REF IN = 1 mA BPO = 2.5 mA
Note 4: Reference decoupled as shown in Figure 6.

TEST LEVEL CODES

All electrical characteristics are subject to the following conditions:

All parameters having min/max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality Assurance inspection. Any blank section in the data column indicates that the specification is not tested at the specified condition.

Unless otherwise noted, all tests are pulsed tests; therefore, $T_J = T_C = T_A$.

TEST LEVEL	TEST PROCEDURE
I	100% production tested at the specified temperature.
II	100% production tested at T_A=25 °C, and sample tested at the specified temperatures.
III	QA sample tested only at the specified temperatures.
IV	Parameter is guaranteed (but not tested) by design and characterization data.
V	Parameter is a typical value for information purposes only.
VI	100% production tested at T_A = 25 °C. Parameter is guaranteed over specified temperature range.

TERMINOLOGY

INTEGRAL LINEARITY ERROR

Integral linearity error is a measure of the maximum deviation from a straight line passing through the end points of the DAC transfer function. It is measured after adjusting for zero offset error and zero gain error.

DIFFERENTIAL LINEARITY ERROR

Differential linearity error is the difference between the measured change and the ideal 1 LSB change between two adjacent codes. A specified differential nonlinearity of <1 LSB ensures monotonicity and no missing codes.

OFFSET ERROR AND GAIN ERROR

Offset error is the absolute difference between actual and theoretical output voltage at code all 1s.

Gain error will be the difference between the measured and ideal full scale output range (after offset has been adjusted to zero) expressed as a percent of the ideal output level. The actual full scale output contains both the gain error and the offset error. Both offset and gain errors are adjustable to zero using the external trim network shown in Figures 4 and 5 respectively.

OUTPUT COMPLIANCE

Output compliance is the allowable range of voltage swing for pin DAC OUT. Other specifications, such as integral nonlinearity, are not guaranteed beyond the specified output compliance voltage.

GENERAL CIRCUIT DESCRIPTION

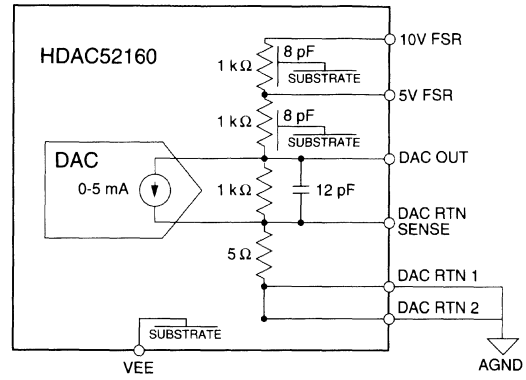
The HDAC52160 uses a unique design approach to set a new standard in monolithic DAC performance. It delivers exceptional 16-bit accuracy and stability over temperature and, at the same time, exhibits an extremely fast 150 ns settling time. On chip support functions include a stable band-gap voltage reference and application resistors for output scaling. Inclusion of these functions reduces the external analog component requirements and further increases accuracy. Digital circuitry on the chip is kept to a minimum (limited to the digital inputs), thus minimizing internal noise generation and providing interface flexibility.

DAC CIRCUITRY

The HDAC52160 uses current source segmentation for the most significant bits and an R-2R ladder for the least significant bits. The ladder, which consists of a resistor network, successively divides the (remaining) reference current to produce a binary weighted current division. In other words, in moving down the ladder, each 2R resistor leg has half the current flow of the previous leg. Each 2R resistor leg is connected to a current source that is trimmed during manufacturing to provide the 16-bit accuracy. Bipolar switches within each leg are controlled by the respective data bits (pins D0 through D15). When the controlling data bit is low, the 2R resistor leg current is steered to pin DAC OUT. When the data bit is high, the leg current is steered to the DAC RTN pins (DAC RTN 1, and DAC RTN 2), which are externally connected to analog ground.

Figure 1 illustrates the equivalent output circuit of the HDAC52160 showing on-chip application resistors and parasitic capacitances.

Figure 1 - Equivalent HDAC52160 Output Circuit



APPLICATION INFORMATION

ACTIVE CURRENT - TO - VOLTAGE CONVERSION

In many DAC applications the output current needs to be converted into a usable voltage signal. The most common current-to-voltage configuration for the HDAC52160 output is shown in Figure 2. Here, an external op amp in conjunction with the internal feedback resistor(s) is used for current-to-voltage (I-to-V) conversion. The op amp provides both a buffered Vout and maintains DAC OUT at a virtual ground. This way, Vout can provide up to a 10 volt output swing (using internal feedback resistors) and the Output Compliance specification (±2.5 volts maximum) is met.

Vout swing is determined by the feedback resistance. For a 5 volt Vout swing, the op amp's output is connected to pin 5 V FSR ("Full Scale Range") which provides an internal 1 kΩ feedback resistance. A 10 volt Vout swing is derived by connecting the op amp output to pin 10 V FSR. This feedback

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connection option is illustrated by the dotted line in Figure 2. Properly trimmed (as discussed later), the connections of Figure 2 as indicated, would result in the ideal output values as listed in Table I.

Figure 2 - Connection of External OP AMP for Active Current-to-Voltage Conversion

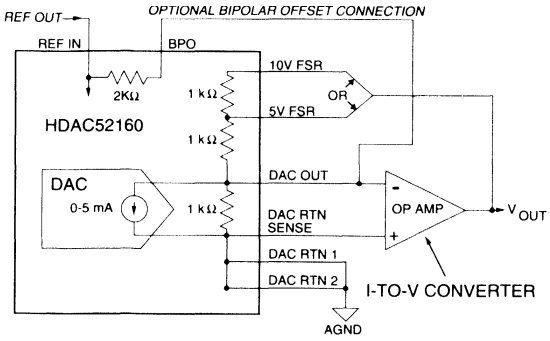


Table I - Normalized voltage values for programmable Output Ranges. (Using Figure 6)

INPUT CODE	OUTPUT VOLTAGE RANGES			
	UNIPOLAR		BIPOLAR	
	5 VOLT	10 VOLT	5 VOLT	10 VOLT
1111 1111 1111 1111	0	0	- 2.50 V	- 5.00 V
1111 1111 1111 1110	+ 76.3 µ V	+ 152.6 µ V	- 2.499924 V	- 4.999846 V
0111 1111 1111 1111	+ 2.500 V	+ 5.00 V	0.00 V	0.00 V
0000 0000 0000 0000	+4.999924 V	+ 9.999846 V	+2.499924 V	+ 4.999846 V

To configure the bipolar output range as indicated in Table I, the BPO pin is connected to DAC OUT. This connection option is illustrated in Figure 2; this offsets the output range by half of the full scale range, so that a half-scale digital input value results in a output current value of zero.

The pin connections for the active I-to-V ranges supported by the internal application resistors are summarized in Table II.

OPERATIONAL AMPLIFIER SELECTION

Selection of the external op amp involves understanding the final system performance requirements in terms of both speed and accuracy. To maintain the 16-bit accuracy provided by DAC OUT at Vout shown in Figure 2, the op amp open loop gain (Avol) must be 96 dB minimum. Any gain lower than this will contribute an error in the I-to-V conversion circuit. To maintain the 150 ns settling time capability provided by DAC OUT at Vout, the op amp must have a minimum gain bandwidth of 50 MHz and settling time of less than 100 ns to 0.0015% of full scale.

Table II - Device Pin Connection Summary for Output Range Programming. (Active I-to-V Conversion Only)

DEVICE PINS	OUTPUT VOLTAGE RANGES			
	UNIPOLAR		BIPOLAR	
	5 VOLT	10 VOLT	5 VOLT	10 VOLT
BPO	NOT CONNECTED	NOT CONNECTED	CONNECTED TO **DAC OUT**	CONNECTED TO **DAC OUT**
5V FSR	CONNECTED TO OP AMP OUTPUT	NOT CONNECTED	CONNECTED TO OP AMP OUTPUT	NOT CONNECTED
10V FSR	NOT CONNECTED	CONNECTED TO OP AMP OUTPUT	NOT CONNECTED	CONNECTED TO OP AMP OUTPUT

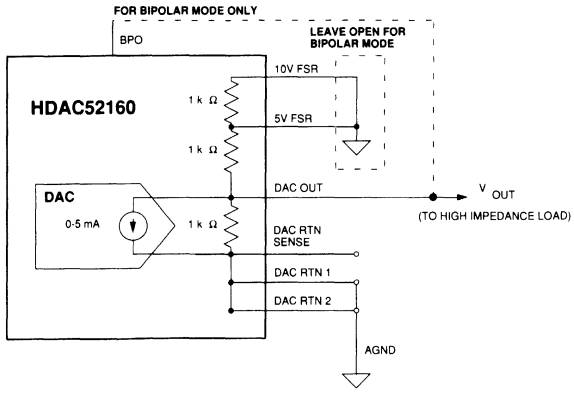
PASSIVE CURRENT-TO-VOLTAGE CONVERSION

Because of the HDAC52160's high voltage compliance, a voltage output can be derived directly at DAC OUT in a method suitable for some applications. By driving a load resistor directly with the current from DAC OUT, a voltage drop results producing Vout. An example of this implementation is shown in Figure 3, where an internal feedback resistor is used as the load 10 V FSR is grounded to optimize settling time). By utilizing all internal resistors, this circuit offers optimized stability and matching.

Output current from the DAC ranges between 0 and 5 mA, which corresponds to an input code of all 1s and all 0s, respectively. For unipolar mode, the net 500 Ω load of Figure 3 results in a -2.5 to 0 volt output range. For bipolar mode, the output voltage range is from +1.67 V to -1.67 V (typical). Both output ranges are within the specified output compliance limits. An external load resistor could also be used with this circuit, however there are difficulties with this arrangement; thermal tracking is not optimum, and the gain adjustment required to overcome the absolute internal resistance and DAC output current errors is beyond the correction range provided by the trim circuit, which is described later.

Note that the input resistance of the circuit driven by Vout will be placed in parallel with the load resistor. This hence limits the application of Figure 3 to high impedance loads. Also note that if a buffer (or other active circuit) is used at Vout in Figure 3, that circuit's CMRR must be at least 100 dB to maintain the DAC's accuracy. This is an advantage of the active current-to-voltage configuration shown in Figure 2, where the input of the op amp is always at virtual ground.

Figure 3 - Connection of Internal Load Resistors for Passive Unipolar/Bipolar Current-to-Voltage Conversion

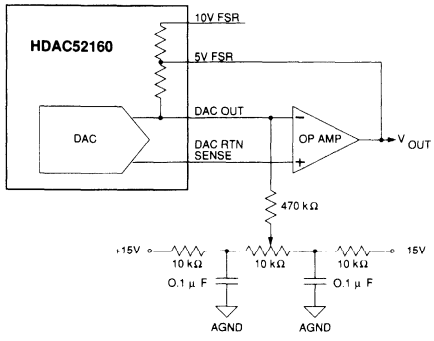


OUTPUT OFFSET COMPENSATION

Although the zero offset error of the HDAC52160 is within ±0.1% of the full scale range, some applications require better accuracy. The offset trim network of Figure 4, shown connected to DAC OUT, will allow offset adjustment in excess of ±0.2 %. This trim network can be used for the active I-to-V conversion network of Figure 2 or the passive circuit of Figure 3. When using an external op amp as in Figure 2, optimum offset stability may be achieved by using the nulling network recommended by the op amp's manufacturer.

Although accuracy of the offset network components is not important, temperature tracking of the resistor and potentiometer values will affect offset trim stability. The resistors and potentiometer should have a low temperature coefficient and the potentiometer should be a high quality, multi-turn component to ensure minute adjustability and stability over time and temperature. The 0.1 µF capacitors shown (typically ceramic) are used to decouple power supply noise from the DAC output circuit.

Figure 4 - Offset Compensation



LOGIC INTERFACE

Because of the low logic input current specification, most TTL families will adequately drive the HDAC52160, even though minimum VIH is specified at 3.75 volts, a figure relatively high by TTL standards. Non-adherence to the VIH spec can result in a less than specified DAC accuracy. High-Speed CMOS logic (HC) or High-Speed CMOS logic with TTL compatible inputs (HCT) are directly compatible with the HDAC52160 logic inputs.

GAIN ADJUSTMENT

With the gain error of the HDAC52160 pre-trimmed to within ±0.15% of full scale accuracy, many applications require external gain adjustments. Configuration of the external gain adjustment network is shown is Figure 5. The adjustment potentiometer is connected between two low noise voltage sources, REF OUT and AGND, as shown. The two bypass capacitors shown further help to eliminate noise. Because of the voltage source asymmetry in relationship to the potentiometer wiper, the adjustment range is an asymmetric -0.6% to +1%. This adjustment range does sufficiently compensate for the error of the device, and the network will work for any type of output configuration. The adjustment range can be made larger and symmetrical by using a circuit similar to the offset compensation network as shown in Figure 4, but with the consequence of introducing power supply noise (and power supply variations) into the vital voltage reference circuit.

The selection criteria for the gain adjustment network components is similar to those described for the offset compensation network: accuracy is not as important as temperature stability.

Figure 5 - Gain Trim Network Suitable for All Output Configurations

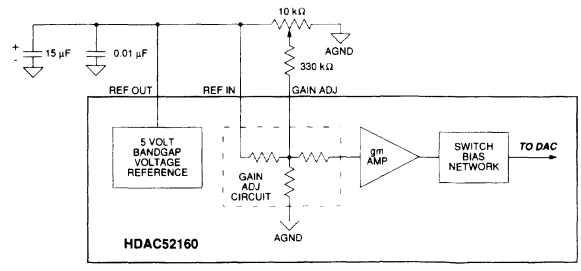


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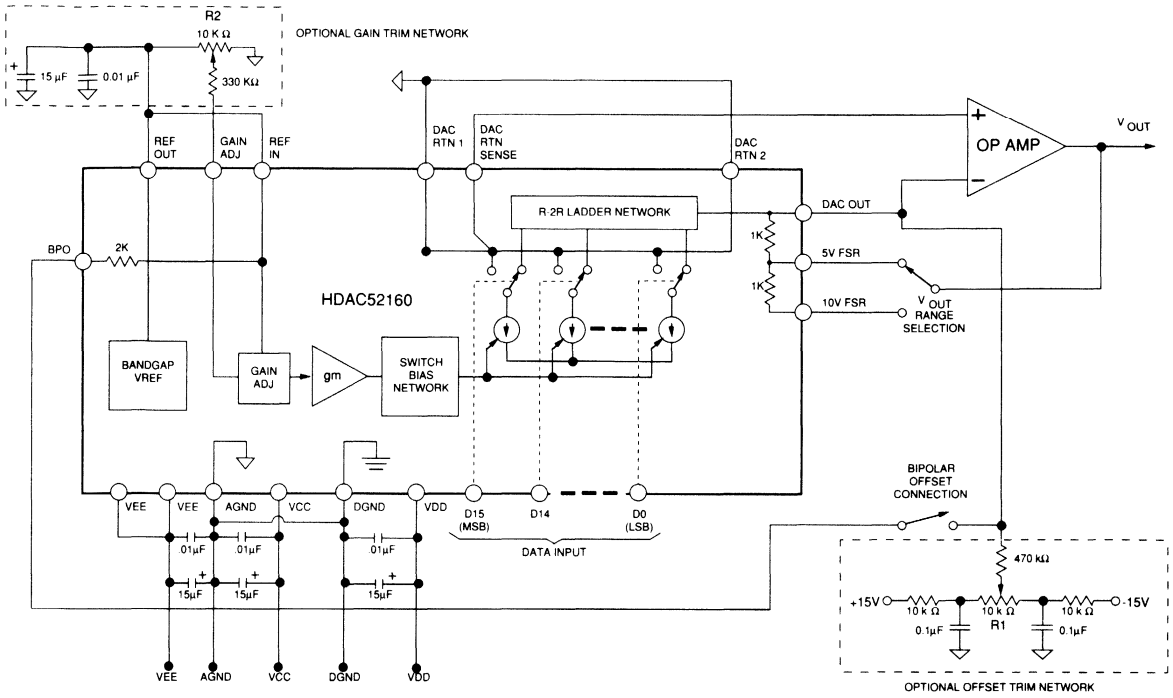
Figure 6 - Typical HDAC52160 Application Circuit



OFFSET AND GAIN CALIBRATION PROCEDURE

This calibration procedure is only applied to the I-to-V applications as shown in Figure 6.

The calibration consists of adjusting the "Vout" most negative voltage to its ideal value for the offset adjustment and adjusting the most positive "Vout" to its ideal value for gain adjustment. The offset and gain errors listed in the specifications for both Unipolar and Bipolar operation, may be adjusted to zero using R1 and R2 (see Figure 6) respectively. All components in the "optional offset trim network" and "optional gain trim network" shown in Figure 6 should have a low temperature coefficient. The potentiometers (R1 and R2) should be multi-turn components to insure minute adjustability.

If the adjustment is not needed, remove the "optional offset trim network" from the circuit.

Unipolar

The first step is offset adjustment. Set the input code to 1111 1111 1111 1111 and adjust R1 until Vout reads zero volts for either 5 V FSR operation or 10 V FSR operation.

Next is the gain adjustment. Set the input code to 0000 0000 0000 0000 and adjust R2 until Vout reads +4.999924 Volts for 5 V FSR operation or +9.999846 Volts for 10 V FSR operation.

Bipolar

For the Bipolar mode of operation, the calibration will start by adjusting the offset. Set the input code to 1111 1111 1111 1111 and adjust R1 until Vout reads -2.50000 Volts for 5 V FSR or -5.00000 Volts for 10 V FSR operation. The gain error calibration is done by setting the input code to 0000 0000 0000 0000 and adjusting R2 until Vout reads +2.499924 Volts for 5 V FSR operation or +4.999848 Volts for 10 V FSR operation.

CIRCUIT LAYOUT CONSIDERATIONS

In any analog system design, care must be taken in the circuit layout process. The design of a high-speed, 16-bit analog system offers an exceptional challenge. The integrity of the system's power supply and grounding is critical, and as with any precision analog component, good decoupling is needed directly at the device. Analog signal traces must be routed in a manner to minimize coupling from potential noise sources. With a 5 volt full-scale output voltage range, a mere 38 μVp-p noise level is equivalent to 1/2 LSB. Low amplitude noise such as this is virtually impossible to eliminate without totally shielding the analog circuit portion.

The power supply must be a well-regulated, noise-free analog voltage source. As with any analog device, the PSRR performance of the HDAC52160 degrades with higher frequency components. Logic noise in the supply or ground line contains high frequency components, so separate supplies and ground returns are recommended for the analog and logic portions of the system. Radiated noise from digital signal traces and power supply traces must also be avoided. Completely shield the analog circuit portion from digital circuitry and digital power supplies and ground. A separate analog ground plane near the device should be used to shield the digital data lines going into the device; this plane should have a trace that completely surrounds the digital inputs, if possible. If an analog ground plane is used with the device for shielding, keep the space between the digital ground plane and analog ground plane wide to prevent capacitive coupling. The best analog ground plane is one with the least resistance, i.e., the minimum total "squares" of surface area, regardless of size. All device grounding should be to the analog ground plane, except for the GND RTN pins which should be tied to the plane at one connection point only.

Figure 6 shows the implementation of decoupling devices (0.01 μF and 15 μF in parallel) at pin REF OUT. These devices should be connected to the analog ground and their incorporation will minimize the overall D/A conversion noise.

Since virtually all the interfacing to the HDAC52160 is analog in nature (the logic inputs are actually analog current switches), DGND and AGND should be tied together at the device and treated as an analog ground. This analog ground and the systems digital ground should be inter-tied only at a single point which has a low impedance path back to the system's power supplies. This will prevent modulation of the analog ground by digital power supply currents as well as digital noise injection.

The external components should be connected to the HDAC52160 with minimum length leads to help prevent noise coupling. The inputs of the external op amp are especially sensitive, so they should have short traces and be well shielded.

To the circuit driven by the HDAC52160, a voltage drop in the common analog ground will appear as a voltage offset. To avoid this, the HDAC52160 has provided a DAC SENSE pin which can be used for remote ground potential sensing.

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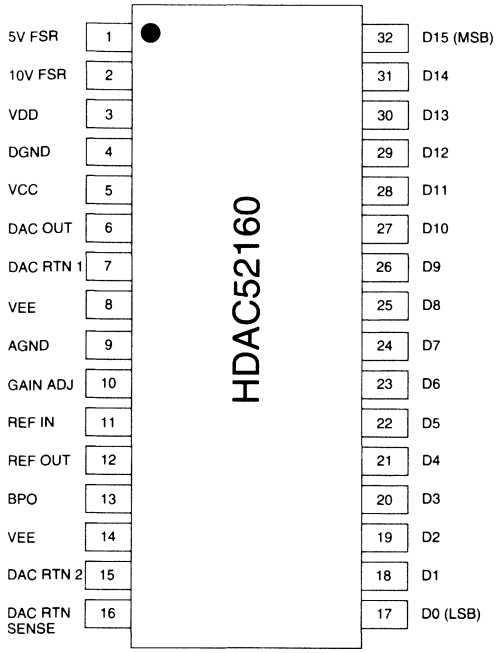
PIN ASSIGNMENT



PIN FUNCTIONS

NAME	FUNCTION
5 V FSR	Output range scaling application resistor
10 V FSR	Output range scaling application resistor
VDD	+5 volt power supply connection
DGND	Digital ground connection
VCC	+15 volt power supply connection
DAC OUT	Analog current output of DAC
DAC RTN 1	DAC ground current return path
VEE	-15 volt power supply connection
AGND	Analog ground connection
Gain ADJ	Input reference trim adjustment
REF IN	Input for internal or external reference
REF OUT	Output of internal reference
BPO	Output offsetting application resistor
VEE	-15 volt power supply connection
DAC RTN 2	DAC ground current return path
DAC RTN SENSE	DAC ground current sense connection
D0	Input data bit 0 (LSB)
D1-14	Input data bit 1-14
D15	Input data bit 15 (MSB)

LEADERSHIP IN DATA CONVERSION AND SIGNAL PROCESSING

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SIGNAL PROCESSING TECHNOLOGIES

SPT5300

18-BIT AUDIO DAC

ADVANCED INFORMATION

FEATURES

- On-Chip Analog Switch for Analog PCM Output
- On-Chip Clock Generator (With External X-tal)
- 8 Times Oversampling
  (Digital Filter - Passband Ripple: 0.000075 dB
  Stopband Attenuation: < -108 dB)
- 16/18-Bit 2s Complement Serial Data Input (MSB First)
- Digital Attenuation Control
- Master Clock Rate: 384 or 512 Times Compatible
- Adjustable System Sampling Rates Including
  32 kHz, 44.1 kHz, and 48 kHz
- Single 5 V Supply

APPLICATIONS

- Compact Disk Players
- DAT Recorders and Players
- Synthesizer Keyboards
- Digital Mixing Consoles
- LDP, DCC and MD
  High Quality Digital Audio Systems

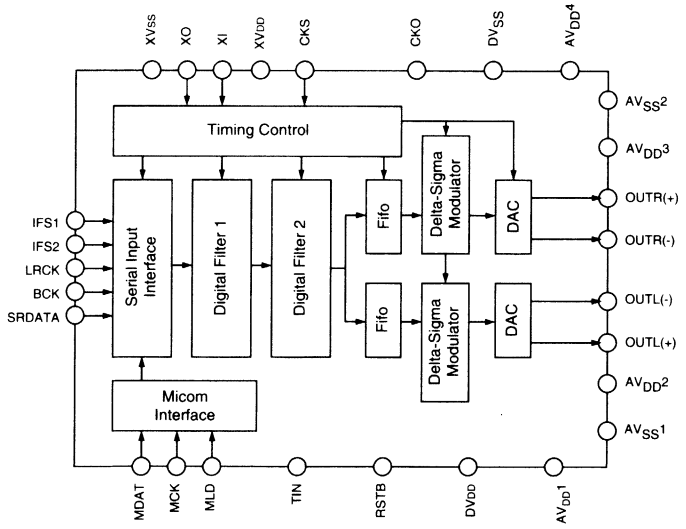
GENERAL DESCRIPTION

The SPT5300 is a CMOS 16/18-bit two-channel digital-to-analog converter for digital audio systems. It is a delta-sigma D/A converter which, in addition to the conventional D/A function, includes an 8X digital interpolation filter followed by a 128X oversampling delta-sigma modulator. The modulator output is the PCM signal generated by the internal control signal.

The total D/A system provides a linear phase response. The delta-sigma D/A converter also includes an extremely flexible serial port utilizing two select pins to support four different interface modes.

The master clock can be either 384 or 512 times the input word rate, supporting various audio environments. The SPT5300 is offered in a 28L small outline package (SOIC) over the commercial temperature range of 0 to +70 °C.

BLOCK DIAGRAM



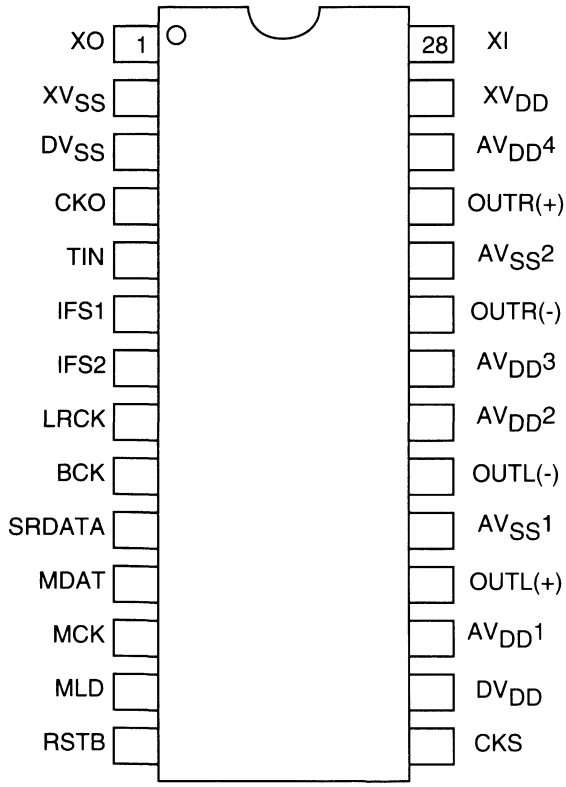
ABSOLUTE MAXIMUM RATINGS (Beyond which damage may occur)

ELECTRICAL SPECIFICATIONS

T_A = 25 °C, V_{DD}=5 V, V_{SS}= 0 V, Clock Rate = 384 times, Input Word Rate=44.1 kHz, Input Data=18 Bits, unless otherwise specified.

PARAMETERS	TEST CONDITIONS	TEST LEVEL	MIN	TYP	MAX	UNITS
Dynamic Range	1 kHz (0 dB)			102		dB
THD	1 kHz (0 dB)			0.0025		%
Signal-to-Noise	1 kHz (0 dB)			108		dB
Crosstalk	1 kHz (0 dB)			100		dB
Power Dissipation				320	440	mW

PIN ASSIGNMENTS



PIN FUNCTIONS

NAME	FUNCTION
XO	X-tal Output
XV_{SS}	Digital Ground (X-tal Oscillator Part)
DV_{SS}	Digital Ground
CKO	384 fs/256 fs Output
TIN	Test Input (This pin must be "L" for normal operation.)
IFS1	Input Format Select 1
IFS2	Input Format Select 2
LRCK	Left/Right Clock Input
BCK	Serial Bit Clock Input
SRDATA	Serial Digital Data Input
MDAT	Micom Command Data Input
MCK	Micom Command Clock Input
MLD	Micom Command Load Input
RSTB	Reset (When Low: Reset)
CKS	Master Clock Select Input (When CKS is low: 512 fs When CKS is high: 384 fs)
DV_{DD}	Digital Supply Voltage
$AV_{DD}1$	Analog Supply Voltage 1
OUTL(+)	L-Channel Positive Output
$AV_{SS}1$	Analog Ground 1
OUTL(-)	L-Channel Negative Output
$AV_{DD}2$	Analog Supply Voltage 2
$AV_{DD}3$	Analog Supply Voltage 3
OUTR(-)	R-Channel Negative Output
$AV_{SS}2$	Analog Ground 2
OUTR(+)	R-Channel Positive Output
$AV_{DD}4$	Analog Supply Voltage 4
XV_{DD}	Digital Supply Voltage (X-tal Oscillator Part)
XI	X-tal Input

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Section 5 Comparators

HCMP96850	High-Speed Single	5-5
HCMP96870A	High-Speed Dual	5-13
SPT9689	Sub-Nanosecond Dual	5-23
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SIGNAL PROCESSING TECHNOLOGIES

HCMP96850

SINGLE ULTRA FAST VOLTAGE COMPARATOR

FEATURES

- Propagation Delay of 2.4 ns (Typ.)
- Propagation Delay Skew <300 ps
- Low Offset ±3 mV
- Latch Control

APPLICATIONS

- High Speed Instrumentation, ATE
- High Speed Timing
- Window Comparators
- Line Receivers
- A/D Conversion
- Threshold Detection

5

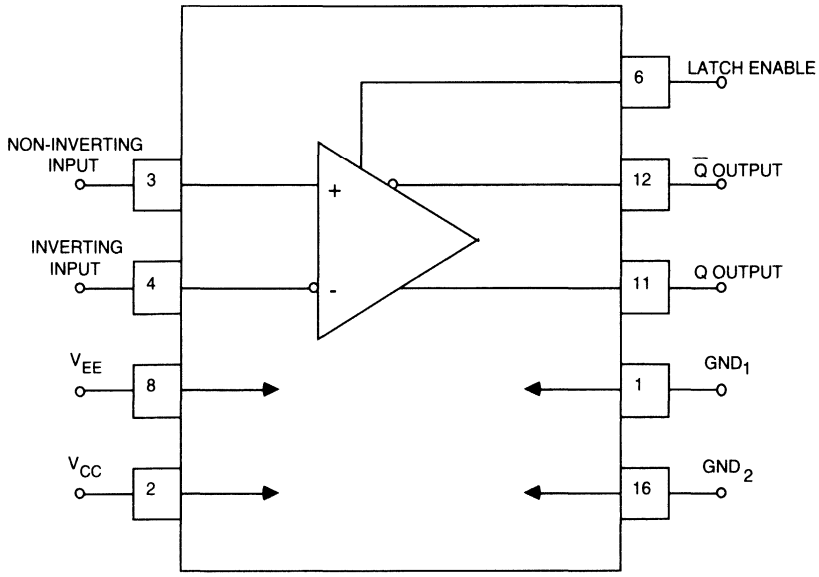
GENERAL DESCRIPTION

The HCMP96850 is a single, very high speed monolithic comparator. It is pin-compatible with and has improved performance over the AD9685 and the AM6685. The HCMP96850 is designed for use in Automatic Test Equipment (ATE), high speed instrumentation, and other high speed comparator applications.

Improvements over other sources include reduced power consumption, reduced propagation delays, and higher input impedance.

The HCMP96850 is available in a 16 lead DIP or in die form.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Beyond which damage may occur)[1] 25 °C

Supply Voltages

Positive Supply Voltage (V_{CC} Measured to GND)..... -0.5 to +6.0 V
Negative Supply Voltage (V_{EE} to GND)..... -6.0 to +0.5 V
Ground Voltage Differential.....-0.5 to +0.5 V

Input Voltages

Input Voltage.....-4.0 to +4.0 V
Differential Input Voltage.....-5.0 to +5.0 V
Input Voltage, Latch Controls.....V_{EE} to 0.5 V

Output

Output Current.....30 mA

Temperature

Operating Temperature, ambient..... -25 to +85 °C
junction.....+150 °C
Lead Temperature, (soldering 60 seconds)..... +300 °C
Storage Temperature..... -65 to +150 °C

Note: 1. Operation at any Absolute Maximum Rating is not implied. See Electrical Specifications for proper nominal applied conditions in typical applications.

ELECTRICAL SPECIFICATIONS

T_A = +25 °C, V_{CC} = +5.0 V ±.25 V, V_{EE} = -5.2 V ±.3 V, R_L = 50 Ohms, unless otherwise specified.

PARAMETERS	TEST CONDITIONS	TEST LEVEL	MIN	TYP	MAX	UNITS
DC ELECTRICAL CHARACTERISTICS						
Input Offset Voltage	R_S = 0 Ohms	IV	-3		+3	mV
Input Offset Voltage (V_{os})	R_S = 0 Ohms, $T_{MIN} < T_A < T_{MAX}$	IV	-3.5		+3.5	mV
(V_{os}) Tempco		V		4		µV/°C
Input Bias Current		I		4	±20	µA
Input Bias Current	$T_{MIN} < T_A < T_{MAX}$	IV		7		µA
Input Offset Current		I	-1.0		+1.0	µA
Input Offset Current	$T_{MIN} < T_A < T_{MAX}$	IV	-1.5		+1.5	µA
Positive Supply Current		I		3.3	5	mA
Negative Supply Current		I		13.5	18	mA
Common Mode Range		I	-2.5		+2.5	V
Open Loop Gain		V		4000		V/V
Input Resistance		V		60		kΩ
Input Capacitance		V		3		pF
Input Capacitance	(LCC Package)	V		1		pF
Power Supply Sensitivity	V_{CC} and V_{EE}	V		70		dB
Common Mode Rejection Ratio		V		80		dB
Power Dissipation	I_{OUTPUT} = 0 mA	IV		90	120	mW

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ELECTRICAL SPECIFICATIONS

T_A = +25 °C, V_{CC} = +5.0 V ±.25 V, V_{EE} = -5.2 V ±.3 V, R_L = 50 Ohms, unless otherwise specified.

PARAMETERS	TEST CONDITIONS	LEVEL	MIN	TYP	MAX	UNITS
OUTPUT LOGIC LEVELS (ECL 10 KH Compatible)						
Output High	50 Ohms to -2 V	I	-.98		-.81	V
Output Low	50 Ohms to -2 V	I	-1.95		-1.63	V
AC ELECTRICAL CHARACTERISTICS[1]						
Propagation Delay	10mV O.D.	III		2.4	3.0	ns
Latch Set-up Time		III		0.6	1	ns
Latch to Output Delay	50 mV O.D.	III			3	ns
Latch Pulse Width		V		2		ns
Latch Hold Time		III			0.5	ns
Rise Time	20% to 80%	V		1.76		ns
Fall Time	20% to 80%	V		1.76		ns

Note 1: 100 mV input step

5

TEST LEVEL CODES

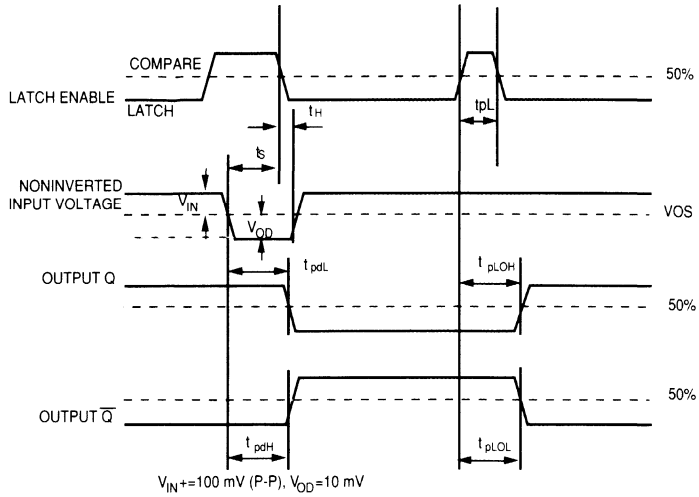
All electrical characteristics are subject to the following conditions:

All parameters having Min./Max. specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality Assurance inspection. Any blank section in the data column indicates that the specification is not tested at the specified condition.

Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

TEST LEVEL	TEST PROCEDURE
I	100% production tested at the specified temperature.
II	100% production tested at T_A = 25 °C, and sample tested at the specified temperatures.
III	QA sample tested only at the specified temperatures.
IV	Parameter is guaranteed (but not tested) by design and characterization data.
V	Parameter is a typical value for information purposes only.

Figure 1 - Timing Diagram



The set-up and hold times are a measure of the time required for an input signal to propagate through the first stage of the comparator to reach the latching circuitry. Input signal changes occurring before t_S will be detected and held; those occurring after t_H will not be detected. Changes between t_S and t_H may or may not be detected.

SWITCHING TERMS (refer to Figure 1)

t_{pdH} INPUT TO OUTPUT HIGH DELAY - The propagation delay measured from the time the input signal crossed the input offset voltage to the 50% point of an output LOW to HIGH transition.

t_{pdL} INPUT TO OUTPUT LOW DELAY - The propagation delay measured from the time the input signal crosses the input offset voltage to the 50% point of an output HIGH to LOW transition.

t_{pLOH} LATCH ENABLE TO OUTPUT HIGH DELAY - The propagation delay measured from the 50% point of the Latch Enable signal HIGH to LOW transition to 50% point of an output LOW to HIGH transition.

t_{pLOL} LATCH ENABLE TO OUTPUT LOW DELAY - The propagation delay measured from the 50% point of the Latch Enable signal HIGH to LOW transition to the 50% point of an output HIGH to LOW transition.

t_H MINIMUM HOLD TIME - The minimum time after the negative transition of the Latch Enable signal that the input signal must remain unchanged in order to be acquired and held at the outputs.

t_{pL} MINIMUM LATCH ENABLE PULSE WIDTH - The minimum time that the Latch Enable signal must be HIGH in order to acquire an input signal change.

t_S MINIMUM SET-UP TIME - The minimum time before the negative transition of the Latch Enable signal that an input signal change must be present in order to be acquired and held at the outputs.

V_{OD} VOLTAGE OVERDRIVE.

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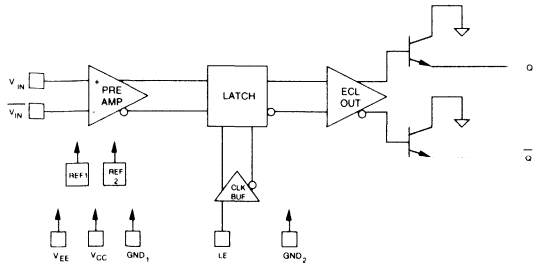
INTERNAL FUNCTION DIAGRAM



GENERAL INFORMATION

The HCMP96850 is an ultra high speed single voltage comparator. It offers tight absolute characteristics which guarantee matching from package to package. The device has differential analog inputs and complementary logic outputs compatible with ECL systems. The output stage is adequate for driving terminated 50 Ohm transmission lines.

The HCMP96850 has one latch enable control and can be driven by standard ECL logic. It also has two separate ground pins, one for the output to accommodate large ground currents without affecting the rest of the circuit, while the other is for the small signal intermediate stages. The input stage is referenced to V_{CC} and V_{EE}.

This comparator offers the following improvements over existing devices:

- Short propagation delays
- Low offset voltage and temperature coefficient
- Low power
- Minimal thermal tails
- Does not oscillate

All of these features combined produce high performance products with timing stability and repeatability for large system precision.

TYPICAL INTERFACE CIRCUIT

A typical interface circuit using the comparator is shown in Figure 2. Although it needs few external components and is easy to apply, there are several considerations that should be noted to achieve optimal performance. The very high operating speeds of the comparator require careful layout, decoupling of supplies, and proper design of transmission lines.

Since the HCMP96850 comparator is a very high frequency and high gain device, certain layout rules must be followed to avoid spurious oscillations. The comparator should be soldered to the board with component lead lengths kept as short as possible. A ground plane should be used, while the input impedance to the part is kept as low as possible, to decrease parasitic feedback. If the output board traces are longer than approximately one-half inch, microstripline techniques must be employed to prevent ringing on the output waveform. Also, the microstriplines must be terminated at the far end of the characteristic impedance of the line to prevent reflections. The HCMP96850 is capable of driving 50 Ohm terminated lines. The termination can be directly tied to -2.0 V or a Thevenin equivalent terminated to the negative supply if a -2.0 V supply is not available. Both supply voltage pins should be decoupled with high frequency capacitors as close to the device as possible.

All pins designated N/C should be soldered to ground for additional noise immunity and interelectrode shielding. All ground pins should be connected to the same ground plane.

The timing diagram for the comparator is shown in Figure 1. The latch enable (LE) pulse is shown at the top. If LE is high in the HCMP96850, the comparator tracks the input difference voltage. When LE is driven low, the comparator outputs are latched into their existing logic states.

The leading edge of the input signal (which consists of 10 mV overdrive) changes the comparator output after a time of t_{pdL} or t_{pdH} (Q or $\overline{Q}$). The input signal must be maintained for a time t_s (set-up time) before the latch enable falling edge and held for time t_H after the falling edge for the comparator to accept data. After t_H, the output ignores the input status until the latch is strobed again. A minimum latch pulse width of t_{pL} is needed for strobe operation, and the output transitions occur after a time of t_{pLOH} or t_{pLOL}.

Unused outputs must be terminated with 50 Ohms to ground while unused latch enable pins should be connected directly to ground.

Figure 2 - Typical Interface Circuit

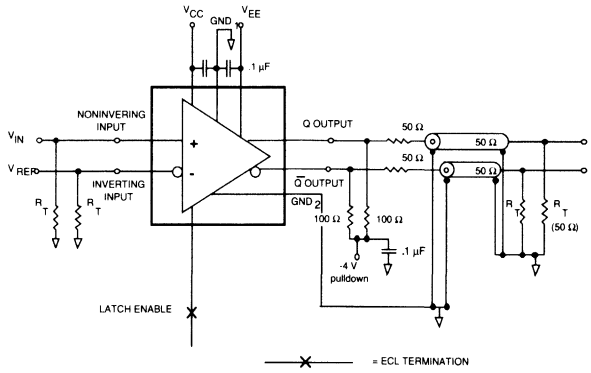


Figure 3 - Equivalent Input Circuit

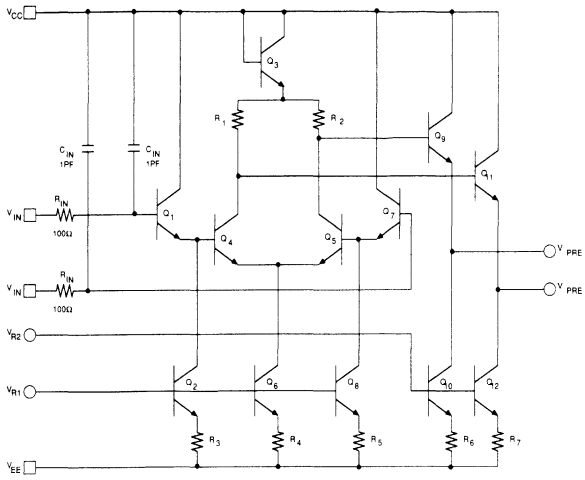


Figure 4 - Output Circuit

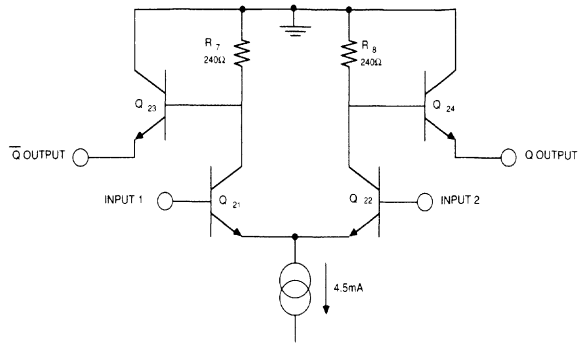


Figure 5A - Test Load

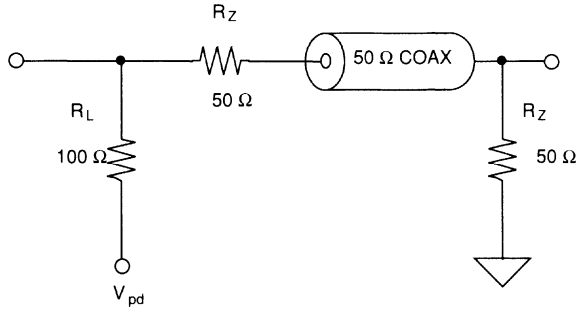
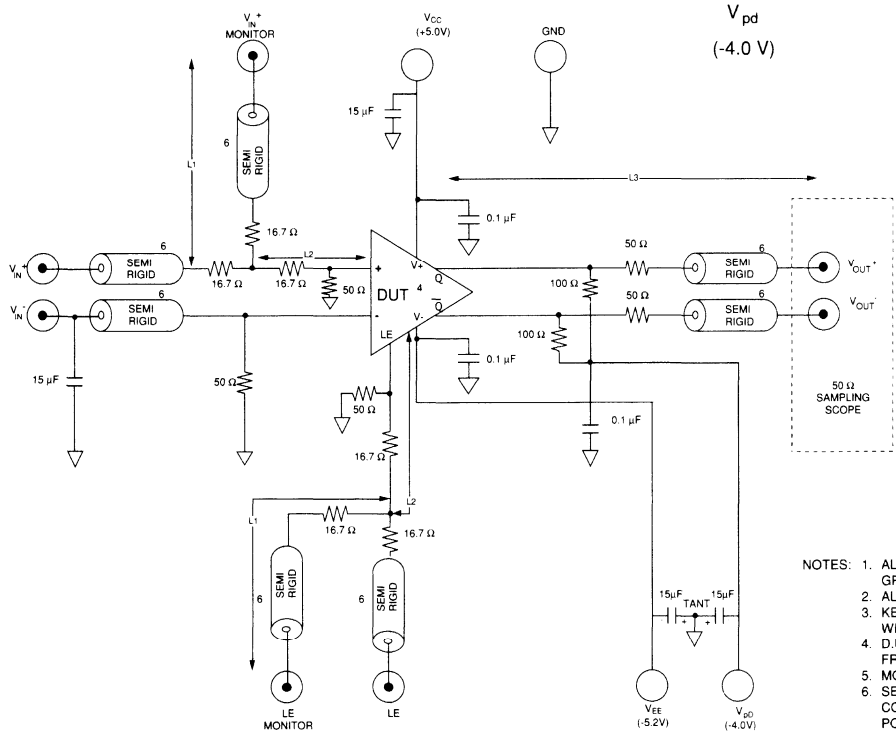


Figure 5B - AC Test Fixture



NOTES:
1. ALL BNC & SEMIRIGID COAX SHIELD ARE GROUNDED.
2. ALL RESISTORS 1% (10 Ω ≈ 49.9 Ω).
3. KEEP ALL LEADS AS SHORT AS POSSIBLE WITH ELECTRICAL LENGTHS L1 = L2 = L3.
4. D.U.T. PLUGS INTO A 16 PIN HIGH FREQUENCY PIN SOCKET.
5. MONITOR INPUT IMPEDANCE 50 Ω TO GND.
6. SEMIRIGID COAX SHIELD SHOULD BE CONNECTED AS CLOSE TO THE DEVICE AS POSSIBLE.

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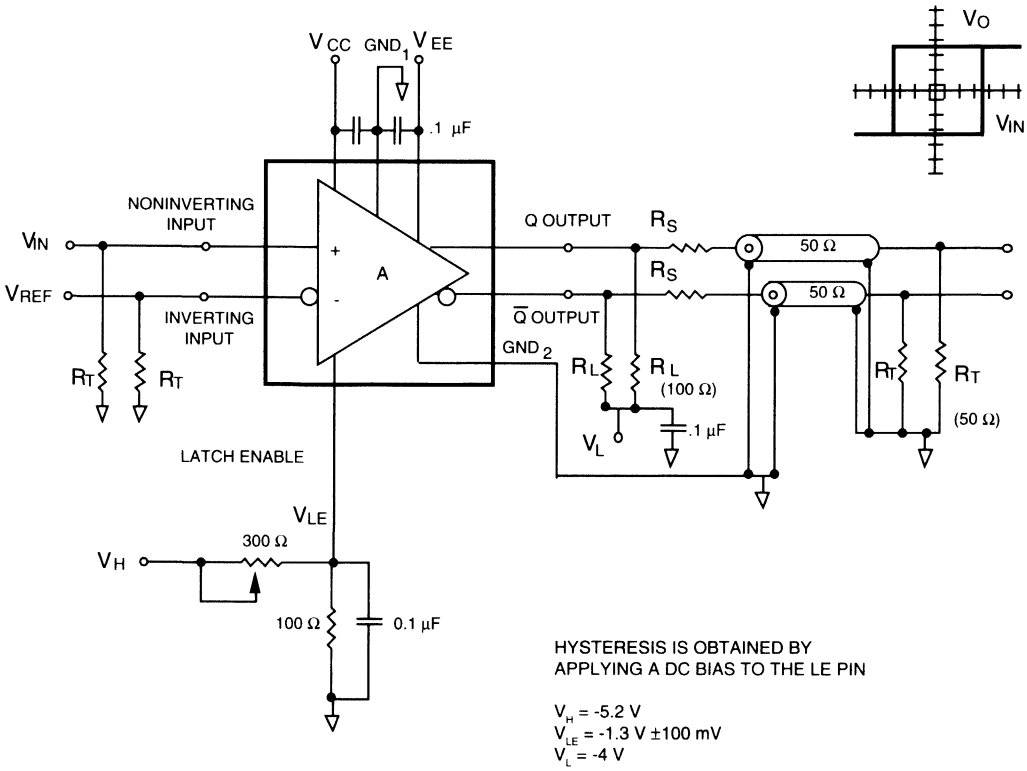
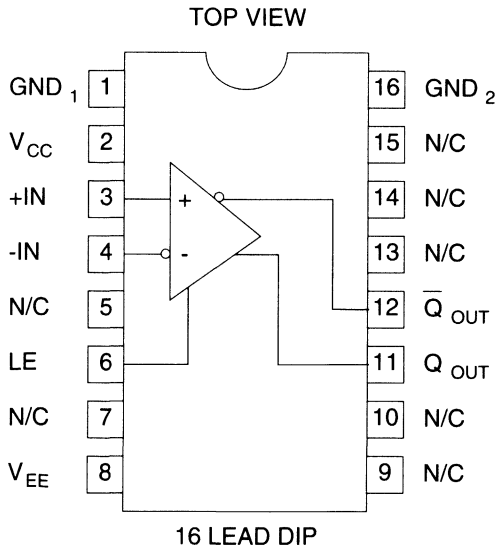
Figure 6 - HCMP96850 with Hysteresis



PIN ASSIGNMENTS



PIN FUNCTIONS

NAME	FUNCTION
GND_1	Circuit Ground
V_{CC}	Positive Supply Voltage
+IN	Noninverting Input
-IN	Inverting Input
N/C	No Connection
LE	Latch Enable
V_{EE}	Negative Supply Voltage
Q_{OUT}	Output
$\overline{Q}_{OUT}$	Inverted Output
GND_2	Output Ground

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SIGNAL PROCESSING TECHNOLOGIES

HCMP96870A

DUAL ULTRA FAST VOLTAGE COMPARATOR

FEATURES

- Propagation Delay <2.3 ns
- Propagation Delay Skew <300 ps
- 300 MHz Minimum Tracking Bandwidth
- Low Offset ±3 mV
- Low Feedthrough and Crosstalk
- Differential Latch Control

APPLICATIONS

- High Speed Instrumentation, ATE
- High Speed Timing
- Window Comparators
- Line Receivers
- A/D Conversion
- Threshold Detection

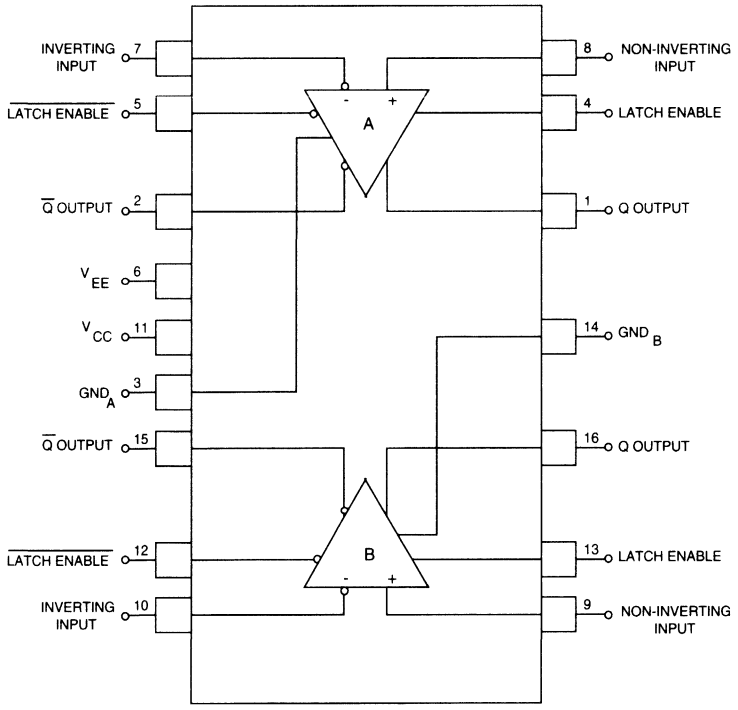
GENERAL DESCRIPTION

The HCMP96870A is a dual, very high speed monolithic comparator. It is pin-compatible with, and has improved performance over AMD's AM6687 and Analog Devices AD9687. The HCMP96870A is designed for use in Automatic Test Equipment (ATE), high speed instrumentation, and other high speed comparator applications.

Improvements over other sources include reduced power consumption, reduced propagation delays, and higher input impedance.

The HCMP96870A is available in a 16 lead cerdip, 16 lead PDIP, 20 contact leadless chip carrier (LCC), 20 lead PLCC, and in die form.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Beyond which damage may occur)[1] 25 °C

Supply Voltages

Positive Supply Voltage (V_{CC} Measured to GND)..... -0.5 to +6.0 V
Negative Supply Voltage (V_{EE} to GND)..... -6.0 to +0.5 V
Ground Voltage Differential.....-0.5 to +0.5 V

Input Voltages

Input Voltage.....-4.0 to +4.0 V
Differential Input Voltage.....-5.0 to +5.0 V
Input Voltage, Latch Controls.....V_{EE} to 0.5 V

Output

Output Current.....30 mA

Temperature

Operating Temperature, ambient.....0 to +70 °C
junction.....+150 °C
Lead Temperature, (soldering 60 seconds)..... +300 °C
Storage Temperature..... -65 to +150 °C

Note: 1. Operation at any Absolute Maximum Rating is not implied. See Electrical Specifications for proper nominal applied conditions in typical applications.

ELECTRICAL SPECIFICATIONS

INDUSTRIAL TEMPERATURE RANGE (-25 to +85 °C)

T_A = +25 °C, V_{CC} = +5.0 V, V_{EE} = -5.20 V, R_L = 50 Ohm, unless otherwise specified.

PARAMETERS	TEST CONDITIONS	TEST LEVEL	MIN	TYP	MAX	UNITS
DC ELECTRICAL CHARACTERISTICS						
Input Offset Voltage	R_S = 0 Ohms	III	-3	±.5	+3	mV
Input Offset Voltage	R_S = 0 Ohms, $T_{MIN} < T_A < T_{MAX}$	IV	-3.5		+3.5	mV
Offset Voltage Tempco		V		4		µV/°C
Input Bias Current		I		6	±20	µA
Input Bias Current	$T_{MIN} < T_A < T_{MAX}$	IV		7	±38	µA
Input Offset Current		I	-1.0		+1.0	µA
Input Offset Current	$T_{MIN} < T_A < T_{MAX}$	IV	-1.5		+1.5	µA
Positive Supply Current		I		7	10	mA
Negative Supply Current		I		27	36	mA
Common Mode Range		I	-2.5		+2.5	V
Open Loop Gain		V		4000		V/V
Input Resistance		V		60		kΩ
Input Capacitance		V		3		pF
Input Capacitance	(LCC Package)	V		1		pF
Power Supply Sensitivity	V_{CC} and V_{EE}	IV	50	100		dB
Common Mode Rejection Ratio		IV	50	85		dB

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ELECTRICAL SPECIFICATIONS

INDUSTRIAL TEMPERATURE RANGE (-25 to +85 °C)

T_A = +25 °C, V_{CC} = +5.0 V, V_{EE} = -5.20 V, R_L = 50 Ohm, unless otherwise specified.

PARAMETERS	TEST CONDITIONS	TEST LEVEL	MIN	TYP	MAX	UNITS
DC ELECTRICAL CHARACTERISTICS						
Power Dissipation	I_{OUTPUT} = 0 mA	I		185	250	mW
OUTPUT LOGIC LEVELS (ECL 10 KH Compatible)						
Output High	50 Ohms to -2 V	I	-.98		-.81	V
Output Low	50 Ohms to -2 V	I	-1.95		-1.63	V
AC ELECTRICAL CHARACTERISTICS[1]						
Propagation Delay	10 mV OD	III		2.0	2.3	ns
Latch Set-up Time		III		0.6	1	ns
Latch to Output Delay	50 mV OD	III			3	ns
Latch Pulse Width		V		2		ns
Latch Hold Time		III			0.5	ns
Rise Time	20% to 80%	V		1.2		ns
Fall Time	20% to 80%	V		1.2		ns
Min Clock Rate		V		300		MHz

Note 1. 100 mV input step.

5

TEST LEVEL CODES

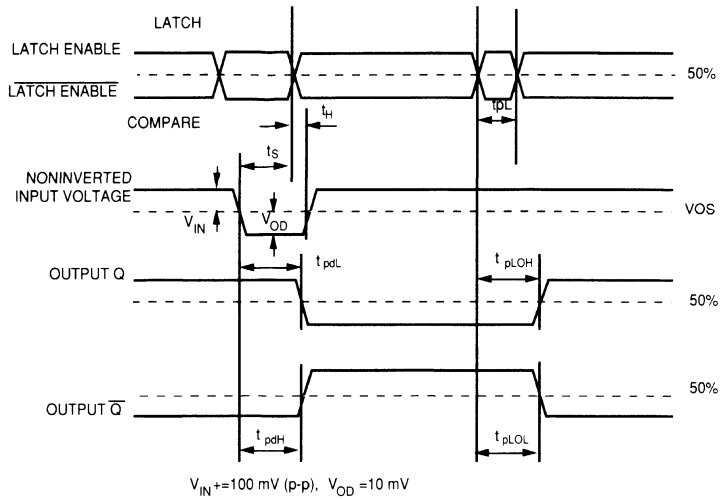
All electrical characteristics are subject to the following conditions:

All parameters having Min./Max. specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality Assurance inspection. Any blank section in the data column indicates that the specification is not tested at the specified condition.

Unless otherwise noted, all tests are pulsed tests, therefore $T_j = T_C = T_A$.

TEST LEVEL	TEST PROCEDURE
I	100% production tested at the specified temperature.
II	100% production tested at T_A = 25 °C, and sample tested at the specified temperatures.
III	QA sample tested only at the specified temperatures.
IV	Parameter is guaranteed (but not tested) by design and characterization data.
V	Parameter is a typical value for information purposes only.

Figure 1 - Timing Diagram



The set-up and hold times are a measure of the time required for an input signal to propagate through the first stage of the comparator to reach the latching circuitry. Input signals occurring before t_s will be detected and held; those occurring after t_H will not be detected. Changes between t_s and t_H may not be detected (LE is the inverse of $\overline{LE}$).

SWITCHING TERMS (refer to Figure 1)

t_{pdH} INPUT TO OUTPUT HIGH DELAY - The propagation delay measured from the time the input signal crossed the input offset voltage to the 50% point of an output LOW to HIGH transition.

t_{pdL} INPUT TO OUTPUT LOW DELAY - The propagation delay measured from the time the input signal crosses the input offset voltage to the 50% point of an output HIGH to LOW transition.

t_{pLOH} LATCH ENABLE TO OUTPUT HIGH DELAY - The propagation delay measured from the 50% point of the Latch Enable signal HIGH to LOW transition to 50% point of an output LOW to HIGH transition.

t_{pLOL} LATCH ENABLE TO OUTPUT LOW DELAY - The propagation delay measured from the 50% point of the Latch Enable signal HIGH to LOW transition to the 50% point of an output HIGH to LOW transition.

t_H MINIMUM HOLD TIME - The minimum time after the negative transition of the Latch Enable signal that the input signal must remain unchanged in order to be acquired and held at the outputs.

t_{pL} MINIMUM LATCH ENABLE PULSE WIDTH - The minimum time that the Latch Enable signal must be HIGH in order to acquire an input signal change.

t_S MINIMUM SET-UP TIME - The minimum time before the negative transition of the Latch Enable signal that an input signal change must be present in order to be acquired and held at the outputs.

$t_{pdL} - t_{pdH}$ DIFFERENTIAL PROPAGATION DELAY (SKEW) INPUT TO OUTPUT - The delay or skew between comparators.

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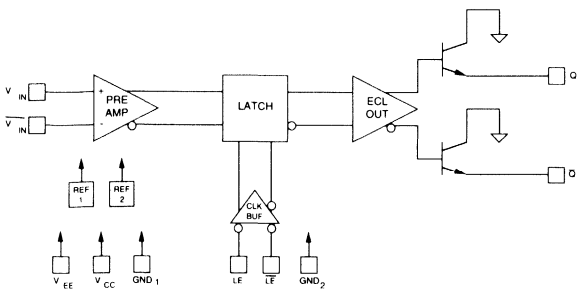
INTERNAL FUNCTIONAL DIAGRAM



GENERAL INFORMATION

The HCMP96870A is an ultra high speed dual voltage comparator. It offers tight absolute characteristics. The device has differential analog inputs and complementary logic outputs compatible with ECL systems. The output stage is adequate for driving terminated 50 ohm transmission lines.

The HCMP96870A has a complementary latch enable control for each comparator. Both can be driven by standard ECL logic.

The dual comparator shares the same V_{CC} and V_{EE} connections but have separate grounds for each comparator to achieve high crosstalk rejection.

This comparator offers the following improvements over existing devices:

- Shorter propagation delays
- Lower offset voltage and temperature coefficient
- Lower overall system power
- Better rejection between comparator channels
- Minimal thermal tails
- Does not oscillate

All of these features combined produce high performance products with timing stability and repeatability for large system precision.

TYPICAL INTERFACE CIRCUIT

The typical interface circuit using the comparator is shown in Figure 2. Although it needs few external components and is easy to apply, there are several conditions that should be met to achieve optimal performance. The very high operating speeds of the comparator require careful layout, decoupling of supplies, and proper design of transmission lines.

Since the HCMP96870A comparator is a very high frequency and high gain device, certain layout rules must be followed to avoid spurious oscillations. The comparator should be soldered to the board with component lead lengths kept as short as possible. A ground plane should be used, and the input impedance to the part should be kept as low as possible to decrease parasitic feedback. If the output board traces are longer than approximately one-half inch, microstripline techniques must be employed to prevent ringing on the output waveform. Also, the microstriplines must be terminated at the far end with the characteristic impedance of the line to prevent reflections. The HCMP96870A is capable of driving 50 ohm terminated lines. The termination can be directly tied to -2.0 V or a Thevenin equivalent terminated to the negative supply if a -2.0 V supply is not available. Both supply voltage pins should be decoupled with high frequency capacitors as close to the device as possible.

All pins designated "N/C" should be soldered to ground for additional noise immunity and interelectrode shielding. All ground pins should be connected to the same ground plane.

The timing diagram for the comparator is shown in Figure 1. The latch enable (LE) pulse is shown at the top. If LE is high and $\overline{LE}$ low in the HCMP96870A, the comparator tracks the input difference voltage. When LE is driven low and $\overline{LE}$ high, the comparator outputs are latched into their existing logic states. Please note that the Latch Enable and $\overline{\text{Latch Enable}}$ notations are not consistent with the industry standard; these names have always been opposite to the pins' functional descriptions. Please see the timing diagram in Figure 1 for absolute clarification.

The leading edge of the input signal (which consists of 10 mV overdrive) changes the comparator output after a time of t_{pdL} or t_{pdH} (Q or $\overline{Q}$). The input signal must be maintained for a time t_s (set-up time) before the latch enable falling edge and LE rising edge and held for time t_H after the falling edge for the comparator to accept data. After t_H, the output ignores the input status until the latch is strobed again. A minimum latch pulse width of t_{pL} is needed for strobe operation, and the output transitions occur after a time of t_{pLOH} or t_{pLOL}.

Unused outputs must be terminated with 50 ohms to ground while unused latch enable pins should be connected to the appropriate supplies: ground or V_{EE}.

Figure 2 - Typical Interface Circuit

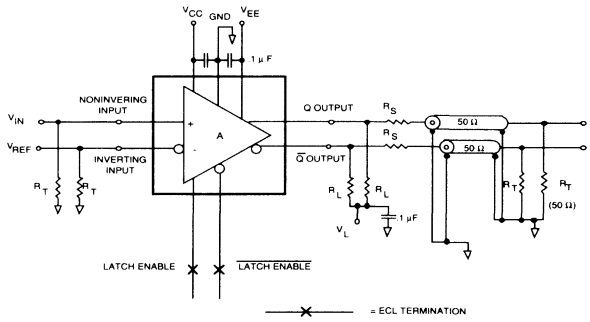


Figure 3 - Equivalent Input Circuit

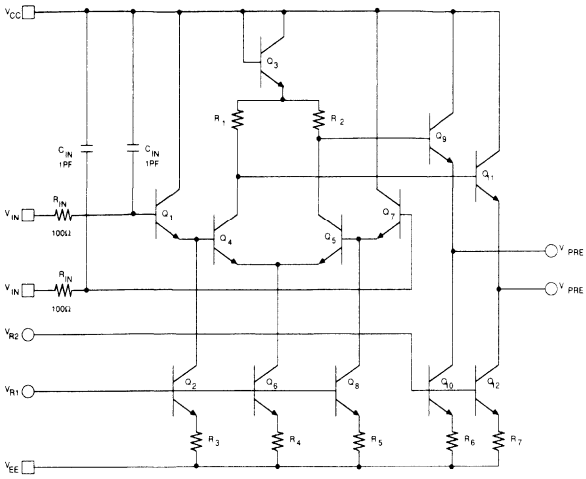


Figure 4 - Output Circuit

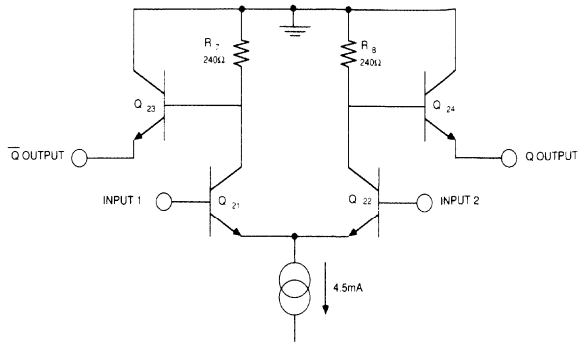


Figure 5A - Test Load

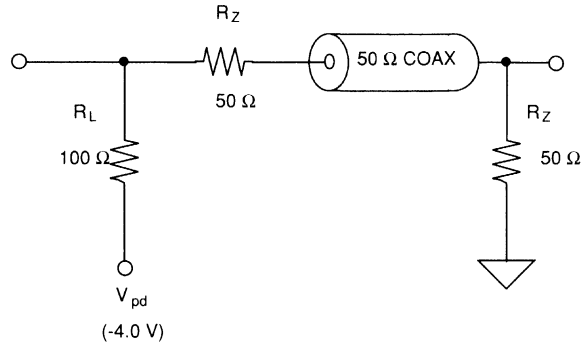
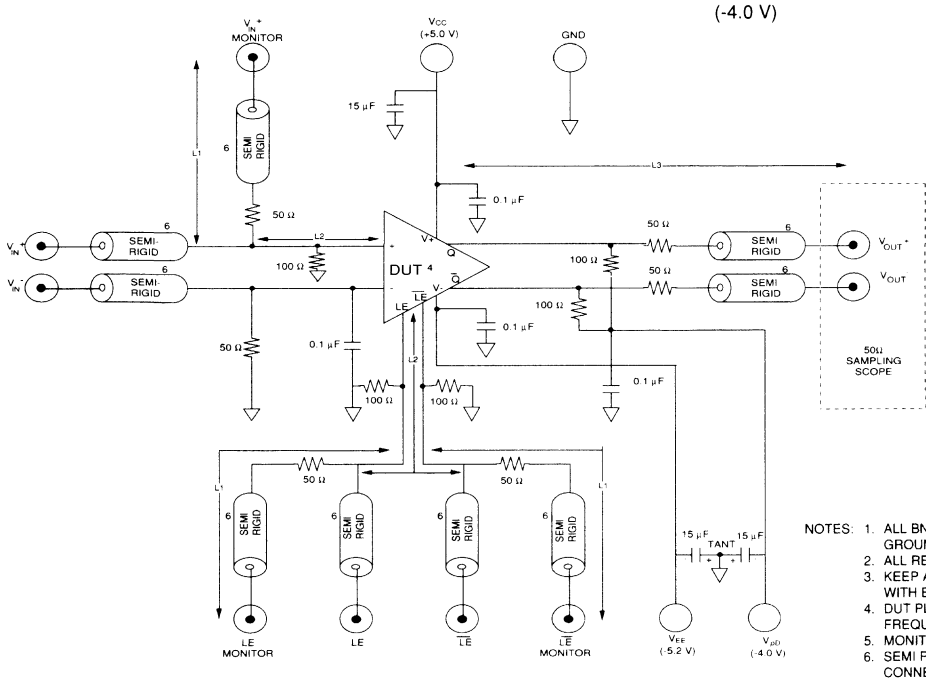


Figure 5B - AC Test Fixture



NOTES:
1. ALL BNC & SEMI RIGID COAX SHIELD ARE GROUNDED.
2. ALL RESISTORS 1% (50 Ω = 49.9 Ω).
3. KEEP ALL LEADS AS SHORT AS POSSIBLE WITH ELECTRICAL LENGTHS L1 = L2 + L3.
4. DUT PLUGS INTO A 16 PIN HIGH FREQUENCY PIN SOCKET.
5. MONITOR INPUT IMPEDANCE 50 Ω TO GND.
6. SEMI RIGID COAX SHIELD SHOULD BE CONNECTED AS CLOSE TO THE DEVICE AS POSSIBLE.

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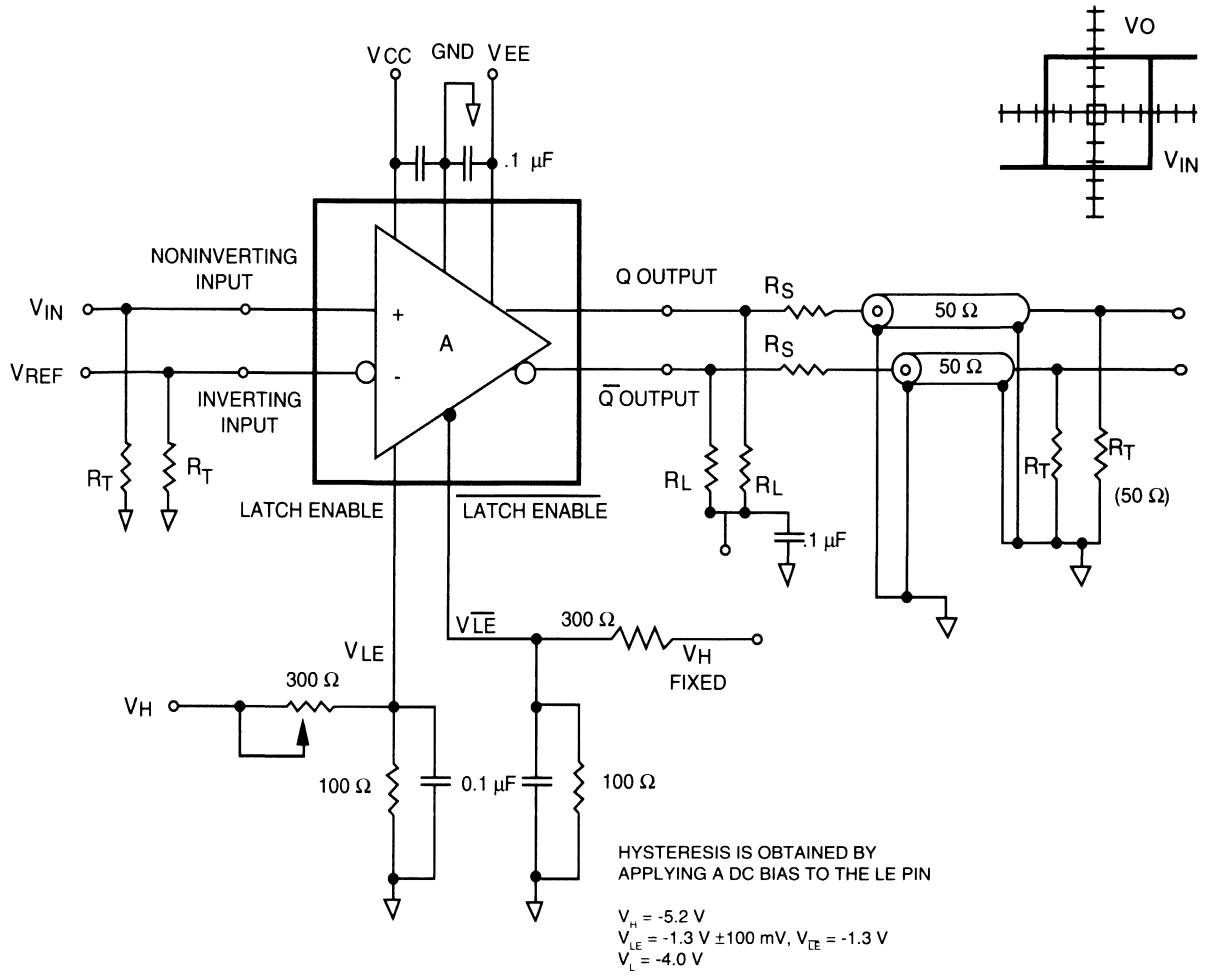
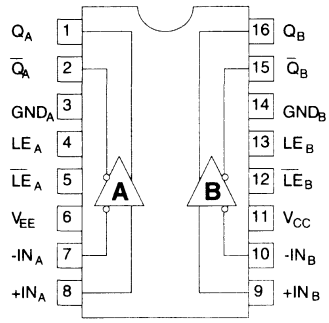
Figure 6 - HCMP96870A with Hysteresis



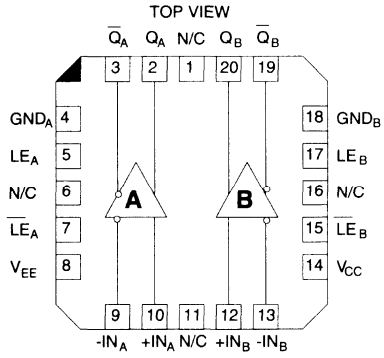
PIN ASSIGNMENTS

TOP VIEW



16 LEAD DIP

TOP VIEW



20 CONTACT CERAMIC LCC/PLCC

PIN FUNCTIONS

NAME	FUNCTION
Q_A	Output A
$\overline{Q}_A$	Inverted Output A
GND_A	Ground A
LE_A	Latch Enable A
$\overline{LE}_A$	Inverted Latch Enable A
V_{EE}	Negative Supply Voltage
$-IN_A$	Inverting Input A
$+IN_A$	Non-Inverting Input A
$+IN_B$	Non-Inverting Input B
$-IN_B$	Inverting Input B
V_{CC}	Positive Supply Voltage
LE_B	Latch Enabled B
$\overline{LE}_B$	Inverted Latch Enable B
GND_B	Ground B
Q_B	Output B
$\overline{Q}_B$	Inverted Output B

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LEADERSHIP IN DATA CONVERSION AND SIGNAL PROCESSING

4755 Forge Road, Co. Springs, CO 80907
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SIGNAL PROCESSING TECHNOLOGIES

SPT9689

DUAL ULTRA-FAST VOLTAGE COMPARATOR

FEATURES

- 650 ps Propagation Delay
- 100 ps Propagation Delay Variation
- 900 MHz Tracking Bandwidth
- 70 dB CMRR
- Low Feedthrough and Crosstalk
- Differential Latch Control
- ECL Compatible

APPLICATIONS

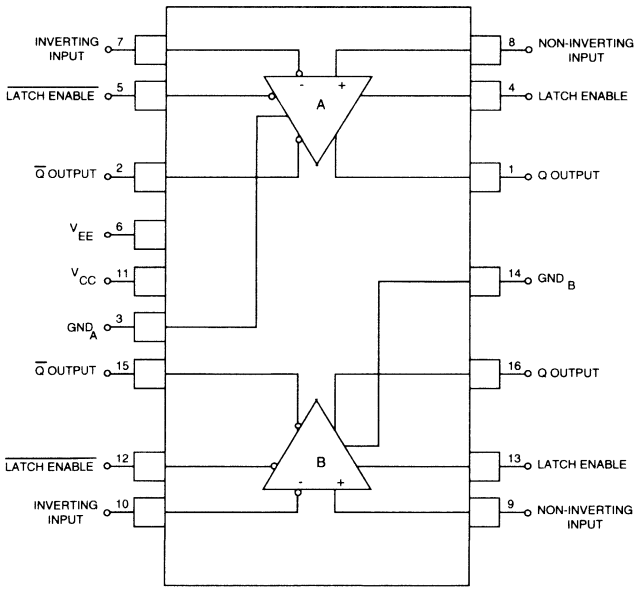
- Automated Test Equipment
- High Speed Instrumentation
- Window Comparators
- High Speed Timing
- Line Receivers
- High Speed Triggers
- Threshold Detection
- Peak Detection

5

GENERAL DESCRIPTION

The SPT9689 is a *Sub*-nanosecond monolithic dual comparator. The propagation delay variation is less than 100 ps from 5 mV to 50 mV input overdrive voltage. The input slew rate is 10 V/ns. The device utilizes a high precision differential input stage with a common-mode range of -2.5 V to +4.0 V. ECL compatible complimentary digital outputs are capable of driving 50 Ω terminated transmission lines and providing 30 mA output drive. The SPT9689 is pin-compatible to HCMP96870 and is available in 20 lead LCC, 16 lead ceramic sidebrazed DIP, PLCC and die form.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Beyond which damage may occur)[1] 25 °C

Supply Voltages

Positive Supply Voltage (V_{CC} Measured to GND)..... .....-0.5 to +6.0 V
Negative Supply Voltage (V_{EE} to GND).....-6.0 to +0.5 V
Ground Voltage Differential.....-0.5 to +0.5 V

Input Voltages

Input Common Mode Voltage..... ..... -4.0 to +5.0 V
Differential Input Voltage..... -3.0 to +3.0 V
Input Voltage, Latch Controls.....V_{EE} to 0.5 V

Output

Output Current.....30 mA

Temperature

Operating Temperature, ambient..... -55 to +125 °C
junction.....+150 °C
Lead Temperature, (soldering 60 seconds)..... +300 °C
Storage Temperature..... -65 to +150 °C

Note: 1. Operation at any Absolute Maximum Rating is not implied. See Electrical Specifications for proper nominal applied conditions in typical applications.

ELECTRICAL SPECIFICATIONS

INDUSTRIAL TEMPERATURE RANGE (-25 to +85 °C)

T_A = +25 °C V_{CC} = +5.0 V ±.25 V, V_{EE} =-5.20 V, RL = 50 Ohm to -2 V, unless otherwise specified.

DC ELECTRICAL PARAMETERS	TEST CONDITIONS	TEST LEVEL	SPT9689A MIN	SPT9689A TYP	SPT9689A MAX	SPT9689B MIN	SPT9689B TYP	SPT9689B MAX	UNITS
Input Offset Voltage	$V_{IN,CM}$=0	I	-10	±3.0	10	-25	±12	25	mV
Input Offset Voltage	$V_{IN,CM}$=0								
	$T_{MIN} < T_A < T_{MAX}$	IV	-15	±4.5	15	-30	±15	30	mV
Offset Voltage Tempco		V		10			40		µV/°C
Input Bias Current		I		±8	±20		±8	±20	µA
Input Bias Current	$T_{MIN} < T_A < T_{MAX}$	IV		±12	±30		±12	±30	µA
Input Offset Current		I		±1.0	±3.0		±2.0	±5.0	µA
Input Offset Current	$T_{MIN} < T_A < T_{MAX}$	IV		±2.0	±5.0		±4.0	±7.0	µA
Positive Supply Current	Dual	I		18	30		18	35	mA
Negative Supply Current	Dual	I		40	55		40	60	mA
Common Mode Range		I	-2.5		+4.0	-2.5		+4.0	V
Open Loop Gain		V		66			66		dB
Differential Input Resistance		V		500			500		kΩ
Input Capacitance	Cerdip Package	V		2.0			2.0		pF
Input Capacitance	LCC Package	V		0.6			0.6		pF
Power Supply Sensitivity		V		70			70		dB

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ELECTRICAL SPECIFICATIONS

INDUSTRIAL TEMPERATURE RANGE (-25 to +85 °C)

T_A = +25 °C, V_{CC} = +5.0 V ±.25 V, V_{EE} = -5.20 V, RL = 50 Ohm to -2 V, unless otherwise specified.

DC ELECTRICAL PARAMETERS	TEST CONDITIONS	TEST LEVEL	SPT9689A MIN	SPT9689A TYP	SPT9689A MAX	SPT9689B MIN	SPT9689B TYP	SPT9689B MAX	UNITS
Common Mode Rejection Ratio	Vcmv=-2.5 to +4.0	V		70			70		dB
Power Dissipation	Dual, Without Load	I		350	425		350	475	mW
Power Dissipation	Dual, With Load	I		400	550		400	550	mW
Output High Level	ECL 50 Ohms to -2 V	I	-1.00		-.81	-1.00		-.81	V
Output Low Level	ECL 50 Ohms to -2 V	I	-1.95		-1.54	-1.95		-1.54	V

AC ELECTRICAL PARAMETERS	TEST CONDITIONS	TEST LEVEL	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Propagation Delay	20 mV O.D.	III		650	850		750	950	ps
Latch Set-up Time		V		450	600		450	600	ps
Latch to Output Delay	50 mV O.D.	V		350	500		350	500	ps
Latch Pulse Width		V		500			500		ps
Latch Hold Time		V		30			30		ps
Rise Time	20% to 80%	V		180			180		ps
Fall Time	20% to 80%	V		80			80		ps
Slew Rate		V		10			10		V/ns
Bandwidth	-3 dB	V		900			900		MHz

CAUTION: ESD SENSITIVE DEVICE

TEST LEVEL CODES

All electrical characteristics are subject to the following conditions:

All parameters having min/max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality Assurance inspection. Any blank section in the data column indicates that the specification is not tested at the specified condition.

Unless otherwise noted, all tests are pulsed tests; therefore, $T_J = T_C = T_A$.

TEST LEVEL	TEST PROCEDURE
I	100% production tested at the specified temperature.
II	100% production tested at T_A=25 °C, and sample tested at the specified temperatures.
III	QA sample tested only at the specified temperatures.
IV	Parameter is guaranteed (but not tested) by design and characterization data.
V	Parameter is a typical value for information purposes only.
VI	100% production tested at T_A = 25 °C. Parameter is guaranteed over specified temperature range.

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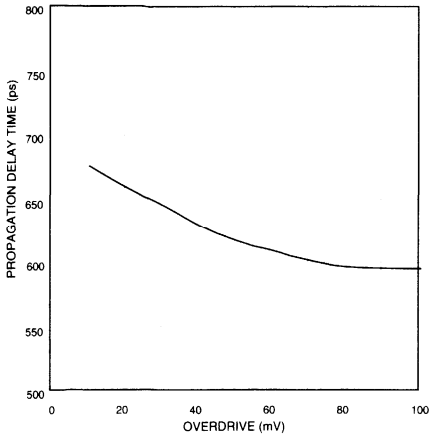
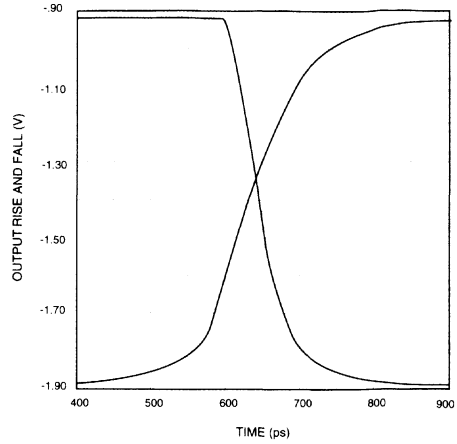
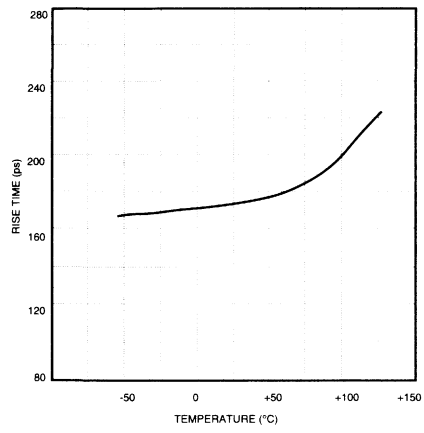
PROPAGATION DELAY VS OVERDRIVE VOLTAGE



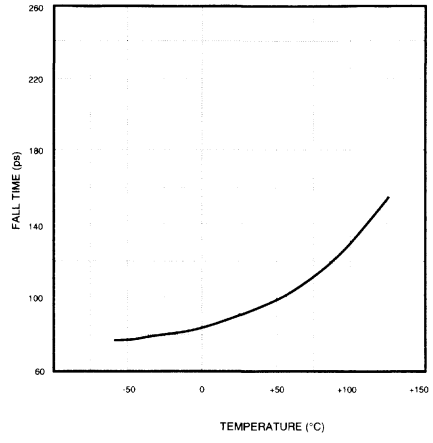
RISE AND FALL OF OUTPUTS VS TIME CROSSOVER



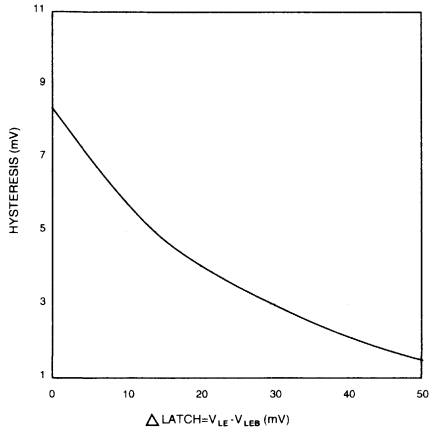
RISE TIME VS TEMPERATURE



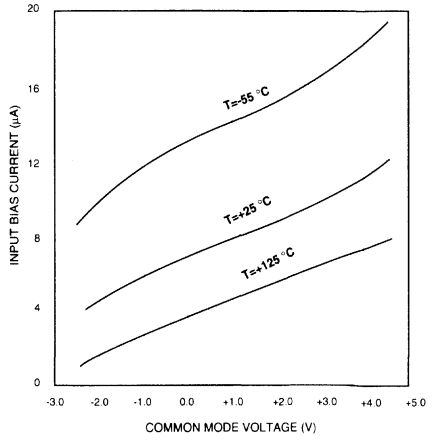
FALL TIME VS TEMPERATURE



HYSTERESIS VS △ LATCH



INPUT BIAS CURRENT VS COMMON MODE VOLTAGE



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GENERAL INFORMATION

The SPT9689 is an ultra high speed dual voltage comparator. It offers tight absolute characteristics. The device has differential analog inputs and complementary logic outputs compatible with ECL systems. The output stage is adequate for driving terminated 50 ohm transmission lines.

The SPT9689 has a complementary latch enable control for each comparator. Both can be driven by standard ECL logic.

The negative common mode voltage is -2.5 V. The positive common mode voltage is +4.0 V.

The dual comparators share the same V_{CC} and V_{EE} connections but have separate grounds for each comparator to achieve high crosstalk rejection.

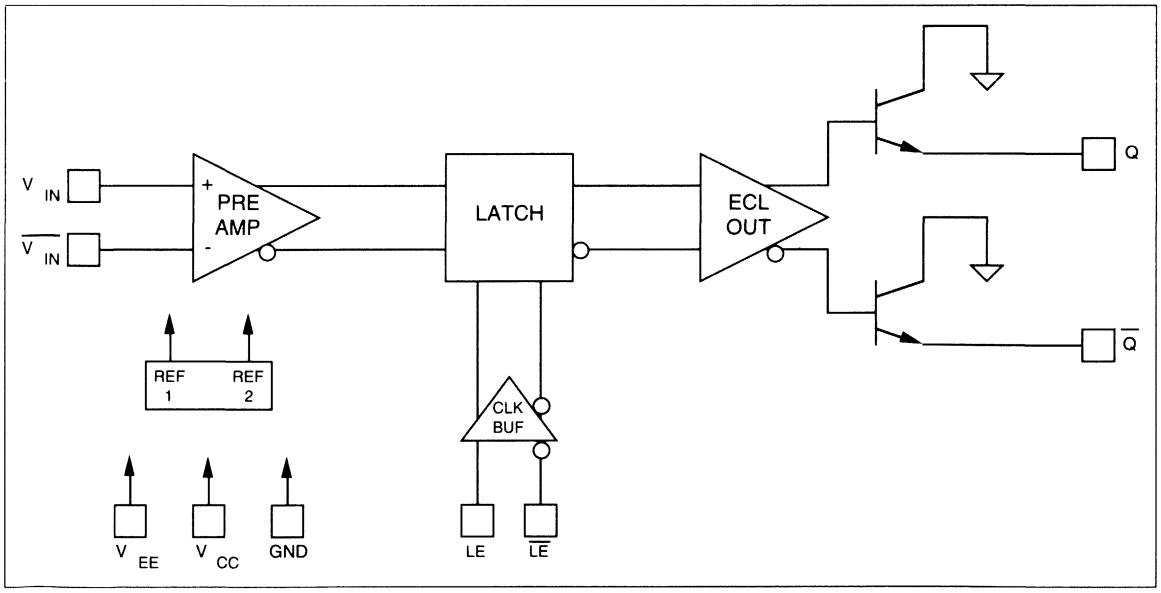
This comparator offers the following improvements over existing devices:

- Proprietary design techniques such as precision clamping of the gain stages result in well behaved and stable output transient response
- Ultra-fast propagation delay time of 650 ps
- Very low propagation delay skew of less than 100 ps in response to input overdrive of +5 to +50 mV
- Excellent input and output rejection between comparator channels
- Hysteresis can be programmed by using LE and $\overline{LE}$ pins to stabilize the output
- Low offset voltage, temperature coefficient and thermal tails

All of these combined features produce high performance products with timing stability and repeatability for large system precision.

5

INTERNAL FUNCTION DIAGRAM



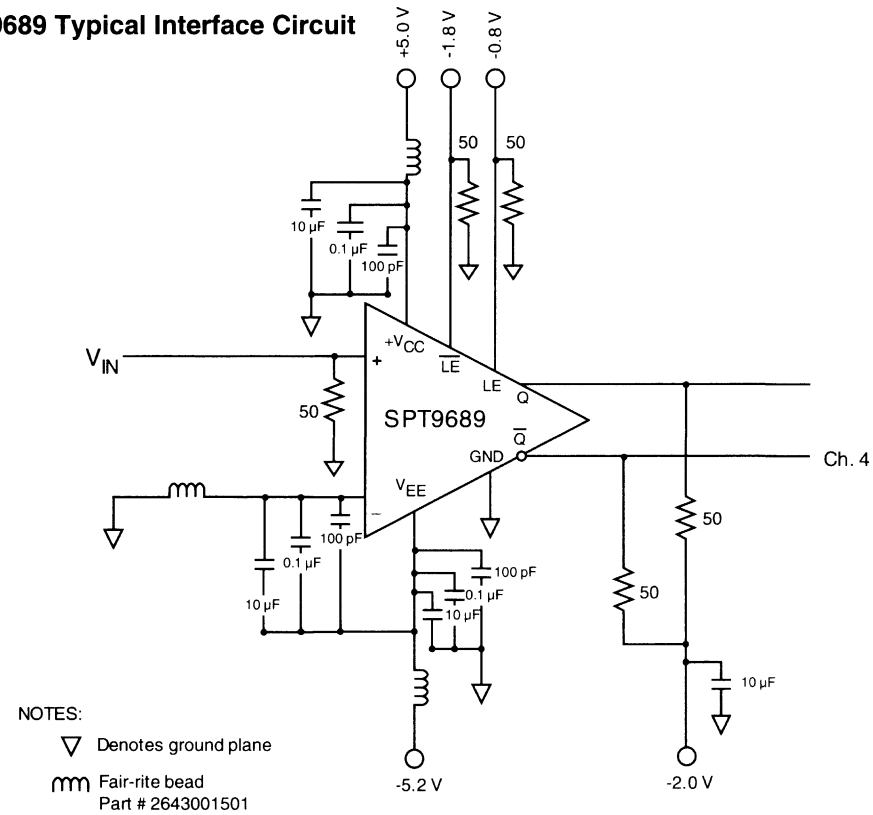
TYPICAL INTERFACE CIRCUIT

The typical interface circuit using the comparator is shown in Figure 1. Although it needs few external components and is easy to apply, there are several conditions that should be noted to achieve optimal performance. The very high operating speeds of the comparator require careful layout, decoupling of supplies, and proper design of transmission lines.

Since the SPT9689 comparator is a very high frequency and high gain device, certain layout rules must be followed to avoid oscillations. The comparator should be soldered to the board with component lead lengths kept as short as possible. A ground plane should be used, while the input impedance to the part is kept as low as possible, to decrease parasitic feedback. If the output board traces are longer than approximately half an inch, microstripline techniques must be employed to prevent ringing on the output waveform. Also, the microstriplines must be terminated at the far end with the characteristic impedance of the line to prevent reflections. The SPT9689 is capable of driving 50 ohm terminated lines. The termination can be directly tied to -2.0 V or a Thevenin equivalent terminated to the negative supply if a -2.0 V supply is not available. Both supply voltage pins should be decoupled with high frequency capacitors as close to the device as possible.

All pins designated "N/C" should be soldered to ground for additional noise immunity and interelectrode shielding. All ground pins should be connected to the same ground plane.

Figure 1 - SPT9689 Typical Interface Circuit



All resistors are chip type 1%
0.1 µF and 100 pF capacitors are chip type mounted as close to pins as possible
10 µF tant capacitors have lead lengths < 0.25" long

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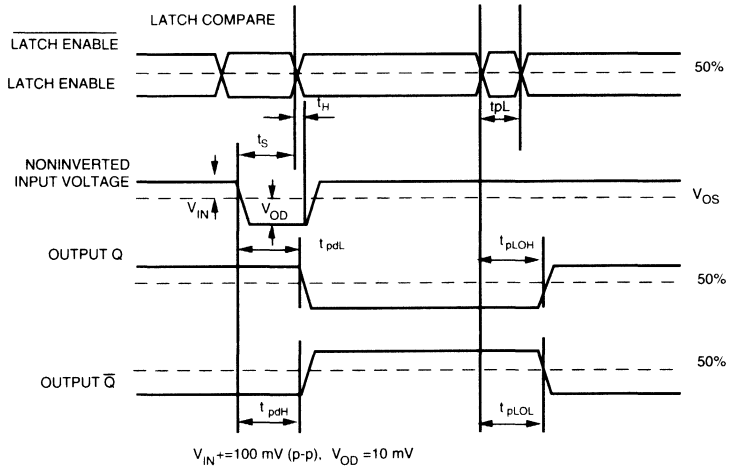
TIMING INFORMATION

The timing diagram for the comparator is shown in Figure 1. The latch enable (LE) pulse is shown at the top. If LE is high and $\overline{LE}$ low in the SPT9689, the comparator tracks the input difference voltage. When LE is driven low and $\overline{LE}$ high, the comparator outputs are latched into their existing logic states.

The leading edge of the input signal (which consists of 10 mV overdrive) changes the comparator output after a time of t_{pdL} or t_{pdH} (Q or $\overline{Q}$). The input signal must be maintained for a time t_s (set-up time) before the latch enable falling edge and $\overline{LE}$ rising edge and held for time t_H after the falling edge for the comparator to accept data. After t_H, the output ignores the input status until the latch is strobed again. A minimum latch pulse width of t_{pL} is needed for strobe operation, and the output transitions occur after a time of t_{pLOH} or t_{pLOL}.

Unused outputs must be terminated with 50 ohms to ground while unused latch enable pins should be connected directly to ground.

Figure 2 - Timing Diagram



The set-up and hold times are a measure of the time required for an input signal to propagate through the first stage of the comparator to reach the latching circuitry. Input signals occurring before t_s will be detected and held; those occurring after t_H will not be detected. Changes between t_s and t_H may not be detected.

SWITCHING TERMS (refer to Figure 2)

t_{pdH} INPUT TO OUTPUT HIGH DELAY - The propagation delay measured from the time the input signal voltage to the 50% point of an output LOW to HIGH transition

t_{pdL} INPUT TO OUTPUT LOW DELAY - The propagation delay measured from the time the input signal reaches the input overdrive voltage to the 50% point of an output HIGH to LOW transition

t_{pLOH} LATCH ENABLE TO OUTPUT HIGH DELAY - The propagation delay measured from the 50% point of the Latch Enable signal HIGH to LOW transition to 50% point of an output LOW to HIGH transition

t_{pLOL} LATCH ENABLE TO OUTPUT LOW DELAY - The propagation delay measured from the 50% point of the Latch Enable signal HIGH to LOW transition to the 50% point of an output HIGH to LOW transition

t_H MINIMUM HOLD TIME - The minimum time after the negative transition of the Latch Enable signal that the input signal must remain unchanged in order to be acquired and held at the outputs

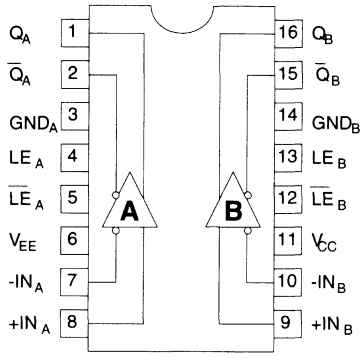
t_{pL} MINIMUM LATCH ENABLE PULSE WIDTH - The minimum time that the Latch Enable signal must be HIGH in order to acquire an input signal change

t_s MINIMUM SET-UP TIME - The minimum time before the negative transition of the Latch Enable signal that an input signal change must be present in order to be acquired and held at the outputs

V_{OD} VOLTAGE OVERDRIVE

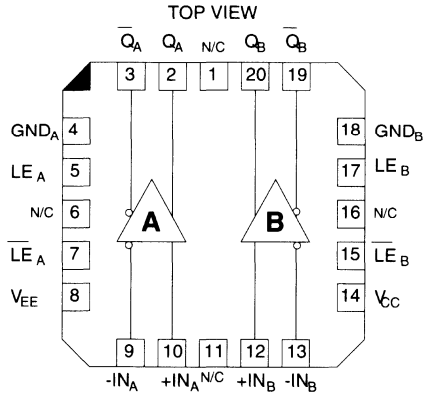
PIN ASSIGNMENTS

TOP VIEW



16 LEAD DIP

TOP VIEW



20 CONTACT CERAMIC LCC/PLCC

PIN FUNCTIONS

NAME	FUNCTION
Q_A	Output A
$\overline{Q}_A$	Inverted Output A
GND_A	Ground A
LE_A	Inverted Latch Enable A
$\overline{LE}_A$	Latch Enable A
V_{EE}	Negative Supply Voltage
$-IN_A$	Inverting Input A
$+IN_A$	Non-Inverting Input A
$+IN_B$	Non-Inverting Input B
$-IN_B$	Inverting Input B
V_{CC}	Positive Supply Voltage
LE_B	Inverted Latch Enabled B
$\overline{LE}_B$	Latch Enable B
GND_B	Ground B
Q_B	Output B
$\overline{Q}_B$	Inverted Output B

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LEADERSHIP IN DATA CONVERSION AND SIGNAL PROCESSING

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SIGNAL PROCESSING TECHNOLOGIES

SPT9691

WIDE INPUT VOLTAGE, JFET COMPARATOR

FEATURES

- Common Mode Range -4.0 to +8.0 V
- Low Input Bias Current <100 pA
- Propagation Delay 2.7 ns (max)
- 300 MHz Minimum Tracking Bandwidth
- Low Offset ±25 mV
- Low Feedthrough and Crosstalk
- Differential Latch Control

APPLICATIONS

- Automated Test Equipment
- High Speed Instrumentation
- Window Comparators
- High Speed Timing
- Line Receivers
- High Speed Triggers
- Threshold Detection
- Peak Detection

5

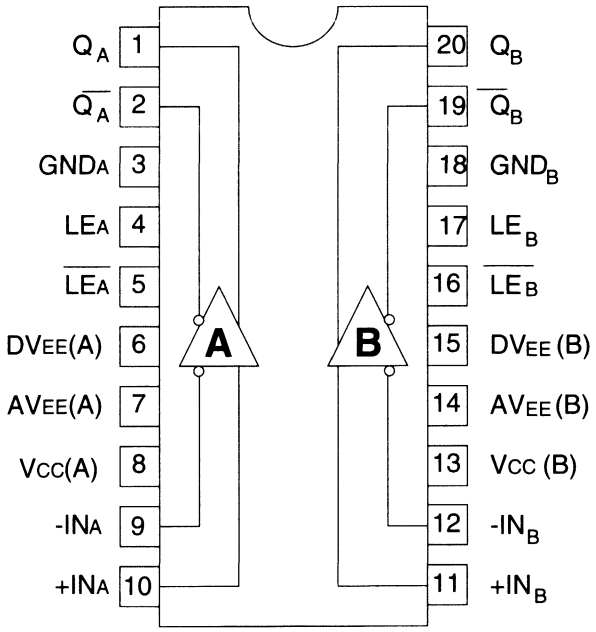
GENERAL DESCRIPTION

The SPT9691 is a high speed, wide common mode voltage, JFET input, dual comparator. It is designed for applications that measure critical timing parameters in which wide common mode input voltages of -4.0 to +8.0 V are required. Propagation delays are constant for overdrives greater than 200 mV.

JFET inputs reduce the input bias currents to the nanoamp level, eliminating the need for input drivers and buffers in most applications. The device has differential analog inputs and complementary logic outputs compatible with ECL systems. Each comparator has a complementary latch enable control that can be driven by standard ECL logic.

The SPT9691 is available in 20-lead LCC (leadless chip carrier), PLCC, sidebrazed ceramic dip and plastic DIP packages as well as in die form.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Beyond which damage may occur)[1] 25°C

Supply Voltages (Measured to GND)

Positive Supply Voltage (AV_{CC}) ..... -0.5 to +11.0 V
Negative Supply Voltage (AV_{EE}) ..... -11.0 to +0.5 V
Negative Supply Voltage (DV_{EE}) ..... -6.0 to +0.5 V

Input Voltages

Input Common Mode Voltage ..... DV_{EE}-1 to $+AV_{CC}$+1
Differential Input Voltage ..... -12.0 to +12.0 V
Input Voltage, Latch Controls ..... V_{EE} to 0.5 V
V_{IN} to AV_{CC} Differential Voltage ..... -16 to +1.0 V
V_{IN} to AV_{EE} Differential Voltage ..... +4 to +21.0 V

Output

Output Current ..... 30 mA

Temperature

Operating Temperature, ambient ..... 0 to +70 °C
junction ..... +150 °C
Lead Temperature, (soldering 60 seconds) ..... +300 °C
Storage Temperature ..... -65 to +150 °C

Note: 1. Operation at any Absolute Maximum Rating is not implied. See Electrical Specifications for proper nominal applied conditions in typical applications. Application of multiple maximum rating conditions at the same time may damage the device.

ELECTRICAL SPECIFICATIONS

COMMERCIAL TEMPERATURE RANGE (0 to 70 °C)

T_A = +25 °C, V_{CC} = +10 V, AV_{EE}=-10.0 V, DV_{EE}=-5.2 V, RL = 50 Ohm to -2V, unless otherwise specified.

DC ELECTRICAL PARAMETERS	TEST CONDITIONS	TEST LEVEL	MIN	TYP	MAX	UNITS
Input Offset Voltage	$V_{IN,CM}$=0 $T_{MIN} < T_A < T_{MAX}$	I IV	-25 -25	0.0 0.0	+25 +25	mV mV
Offset Voltage Tempco		V		50		µV/°C
Input Bias Current		I		±0.1	±10	nA
Input Bias Current	$T_{MIN} < T_A < T_{MAX}$	IV		±2.0	±100	nA
Input Offset Current		V		±1.0		nA
Input Offset Current	$T_{MIN} < T_A < T_{MAX}$	V		±10		nA
Positive Supply Current (Dual)	Vcc=10 V	I		23	30	mA
Negative Supply Current (Dual)	V_{AEE}=-10.0 V	I		15	20	mA
Negative Supply Current (Dual)	V_{DEE}=-5.2 V	I		55	70	mA
Common Mode Range		I	-4.0		+8.0	V
Differential Voltage Range		I			±10	V
Open Loop Gain		V		60		dB
Differential Input Resistance		V		2		GΩ
Input Capacitance	Sidebrazed Package LCC Package PLCC Package PDIP	V		2.9 1.0 1.0 2.9		pF pF pF pF
Power Supply Sensitivity		V		60		dB

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ELECTRICAL SPECIFICATIONS

COMMERCIAL TEMPERATURE RANGE (0 to 70 °C)

T_A = +25 °C, V_{CC} = +10 V, AV_{EE}=-10.0 V, DV_{EE}=-5.2 V, RL = 50 Ohm to -2V, unless otherwise specified.

DC ELECTRICAL PARAMETERS	TEST CONDITIONS	TEST LEVEL	MIN	TYP	MAX	UNITS
Common Mode Rejection Ratio		I	50	60		dB
	$T_{MIN} < T_A < T_{MAX}$	IV	45	55		dB
Power Dissipation	Dual	I		700	800	mW
Output High Level	ECL 50 Ohms to -2V	I	-.98		-.70	V
Output Low Level	ECL 50 Ohms to -2V	I	-1.95		-1.65	V
AC ELECTRICAL PARAMETERS						
Propagation Delay[1]	150 mV O.D.	III	1.7	2.2	2.7	ns
Propagation Delay TEMPCO		V		2		ps/ °C
Propagation Delay Skew (A vs B)		V		100		ps
Propagation Delay Dispersion[2]	150 mV Overdrive Min.	V		200		ps
Latch Set-up Time		V		1.7		ns
Latch to Output Delay	150 mV O.D.	V		0.8		ns
Latch Pulse Width		V		2		ns
Latch Hold Time		V		-1.9		ns
Rise Time	20% to 80%	V		0.4		ns
Fall Time	20% to 80%	V		0.4		ns
Slew Rate		V		3		V/ns
Bandwidth	-3 dB	V		300		MHz

NOTES:
[1]Valid for both high-to-low and low-to-high transitions
[2]Dispersion is the change in propagation delay due to changes in slew rate, overdrive, and common mode level.

TEST LEVEL CODES

All electrical characteristics are subject to the following conditions:

All parameters having min/max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality Assurance inspection. Any blank section in the data column indicates that the specification is not tested at the specified condition.

Unless otherwise noted, all tests are pulsed tests; therefore, $T_J = T_C = T_A$.

TEST LEVEL	TEST PROCEDURE
I	100% production tested at the specified temperature.
II	100% production tested at T_A=25 °C, and sample tested at the specified temperatures.
III	QA sample tested only at the specified temperatures.
IV	Parameter is guaranteed (but not tested) by design and characterization data.
V	Parameter is a typical value for information purposes only.
VI	100% production tested at T_A = 25 °C. Parameter is guaranteed over specified temperature range.

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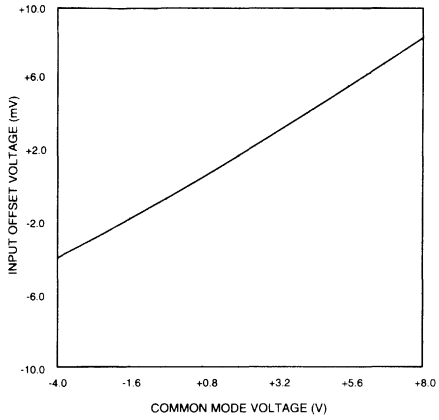
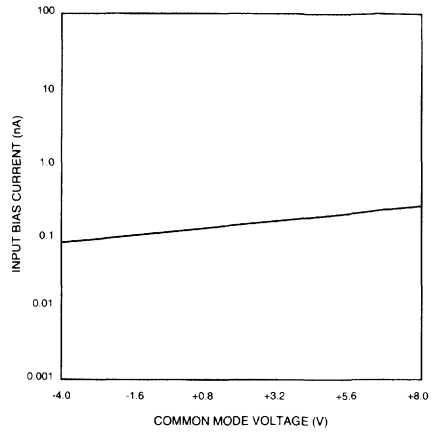
TYPICAL PERFORMANCE CURVES

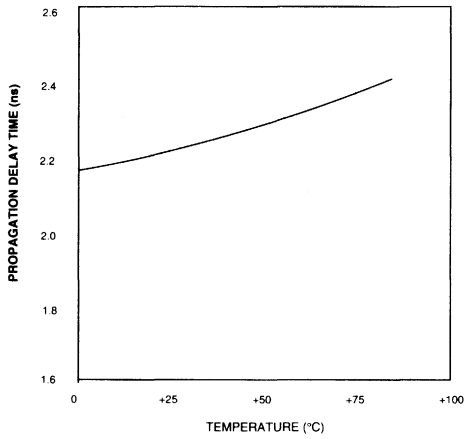
INPUT OFFSET VOLTAGE VS COMMON MODE VOLTAGE (T=+25 °C)



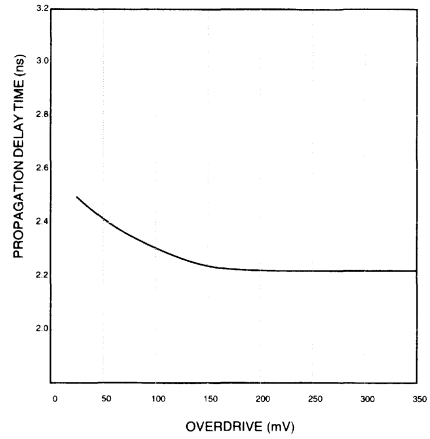
INPUT BIAS CURRENT VS COMMON MODE VOLTAGE (+25 °C)



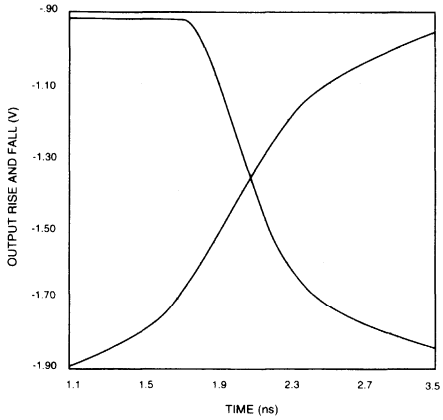
PROPOGATION DELAY TIME VS TEMPERATURE (V_{OD}=150 mV)



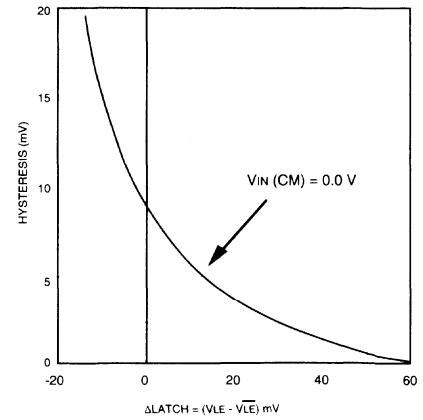
PROPAGATION DELAY TIME VS OVERDRIVE (mV)



RISE AND FALL OF OUTPUTS VS TIME CROSSOVER



HYSTERESIS VS ΔLATCH



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GENERAL INFORMATION

The SPT9691 is an ultra high speed dual voltage comparator. It offers tight absolute characteristics. The device has differential analog inputs and complementary logic outputs compatible with ECL systems. The output stage is adequate for driving terminated 50 ohm transmission lines.

The SPT9691 has a complementary latch enable control for each comparator. Both can be driven by standard ECL logic.

A common mode voltage range of -4 V to +8 V is achieved by a proprietary JFET input design which requires a separate negative power supply (AV_{EE}).

The dual comparators have separate V_{CC}, AV_{EE}, DV_{EE}, and grounds for each comparator to achieve high crosstalk rejection. Single channel operation can be accomplished by floating all pins (including the ground and supply pins) of the unused comparator. Power dissipation during single mode operation will be reduced to 1/2 of the dual mode operation.

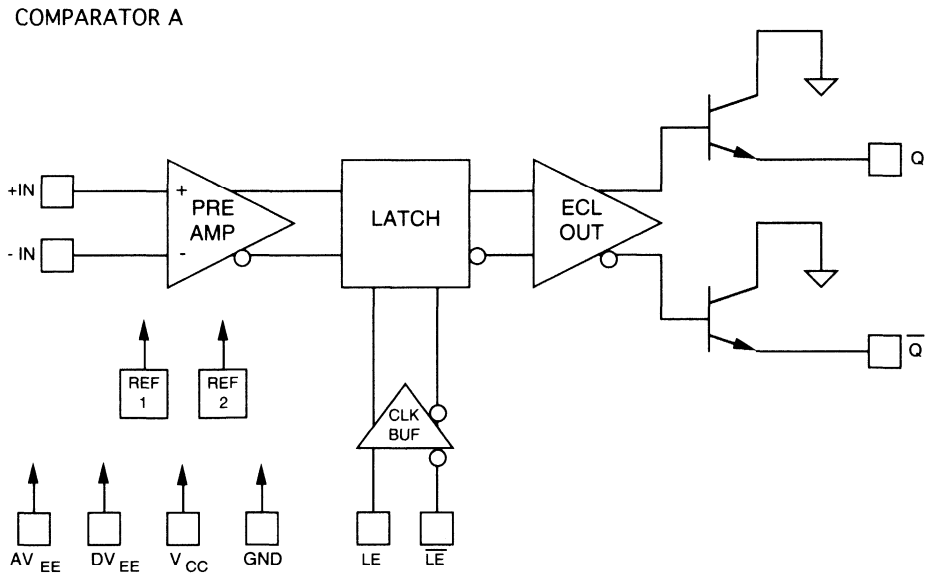
This comparator offers the following improvements over existing devices:

- Ultra low input bias current and input current offset
- Common mode voltage of -4 to +8 V
- Short propagation delays
- Excellent input and output rejection between comparator channels
- Improved input protection reliability due to JFET input stage design

All of these combined features produce high performance products with timing stability and repeatability for large system precision.

5

INTERNAL FUNCTION DIAGRAM



TYPICAL INTERFACE CIRCUIT

The typical interface circuit using the comparator is shown in Figure 1. Although it needs few external components and is easy to apply, there are several conditions that should be noted to achieve optimal performance. The very high operating speeds of the comparator require careful layout, decoupling of supplies, and proper design of transmission lines.

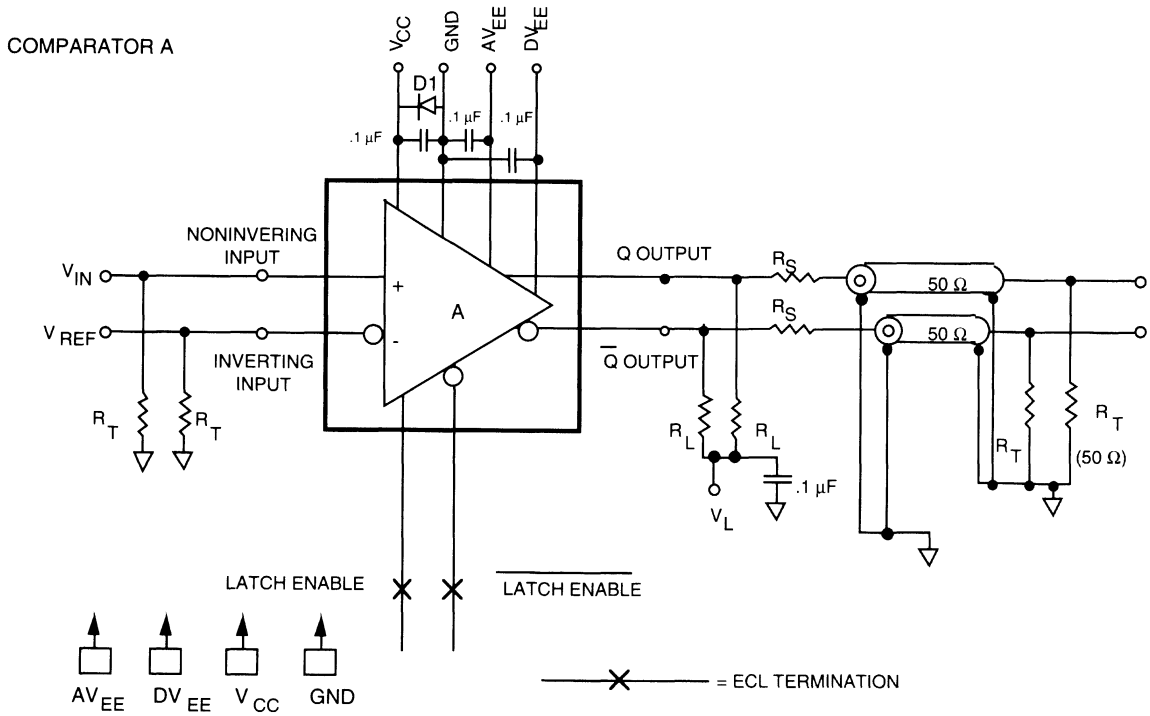
Since the SPT9691 comparator is a very high frequency and high gain device, certain layout rules must be followed to avoid oscillations. The comparator should be soldered to the board with component lead lengths kept as short as possible. A ground plane should be used, while the input impedance to the part is kept as low as possible, to decrease parasitic feedback. If the output board traces are longer than approximately half an inch, microstripline techniques must be employed to prevent ringing on the output waveform. Also, the microstriplines must be terminated at the far end with the characteristic impedance of the line to prevent reflections. The SPT9691 is capable of driving 50 ohm terminated lines. The termination can be directly tied to -2.0 V or a Thevenin equivalent terminated to the negative supply if a -2.0 V supply is not available. All supply voltage pins should be decoupled with high frequency capacitors as close to the device as possible.

Diode D1 connected between V_{CC} and GND is recommended to prevent possible damage to the device in case the V_{CC} supply is disconnected. The diode should be a 1N914 or equivalent. If V_{CC} is disconnected with this diode in place, there will be approximately a 6 mA current draw from both AV_{EE} and DV_{EE}.

Note: At no time should both inputs be allowed to float with power applied to the device. At least one of the inputs should be tied to a voltage within the common mode range (-4.0 to +8.0 V) to prevent possible damage to the device. To prevent possible latch-up during initial power up, the input voltages should not exceed ±1 V.

All ground pins should be connected to the same ground plane to further improve noise immunity and shielding.

FIGURE 1 SPT9691 TYPICAL INTERFACE CIRCUIT



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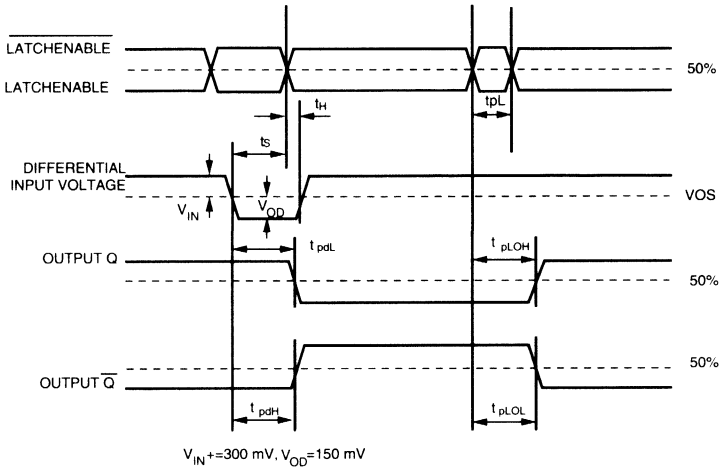
TIMING INFORMATION

The timing diagram for the comparator is shown in Figure 2. If LE is high and $\overline{LE}$ low in the SPT9691, the comparator tracks the input difference voltage. When LE is driven low and $\overline{LE}$ high, the comparator outputs are latched into their existing logic states.

The leading edge of the input signal (which consists of the overdrive voltage) changes the comparator output after a time of t_{pdL} or t_{pdH} (Q or $\overline{Q}$). The input signal must be maintained for a time t_s (set-up time) before the LE falling edge and $\overline{LE}$ rising edge and held for time t_H after the falling edge for the comparator to accept data. After t_H, the output ignores the input status until the latch is strobed again. A minimum latch pulse width of t_{pL} is needed for strobe operation, and the output transitions occur after a time of t_{pLOH} or t_{pLOL}.

Unused outputs must be terminated with 50 ohms to ground while unused $\overline{LE}$ pins should be connected directly to ground.

Figure 2 - Timing Diagram



The set-up and hold times are a measure of the time required for an input signal to propagate through the first stage of the comparator to reach the latching circuitry. Input signals occurring before t_s will be detected and held; those occurring after t_H will not be detected. Changes between t_s and t_H may not be detected.

SWITCHING TERMS (refer to Figure 2)

t_{pdH} INPUT TO OUTPUT HIGH DELAY - The propagation delay measured from the time the input signal reaches the input overdrive voltage to the 50% point of an output LOW to HIGH transition.

t_{pdL} INPUT TO OUTPUT LOW DELAY - The propagation delay measured from the time the input signal reaches the input overdrive voltage to the 50% point of an output HIGH to LOW transition.

t_{pLOH} LATCH ENABLE TO OUTPUT HIGH DELAY - The propagation delay measured from the 50% point of the Latch Enable signal HIGH to LOW transition to 50% point of an output LOW to HIGH transition.

t_{pLOL} LATCH ENABLE TO OUTPUT LOW DELAY - The propagation delay measured from the 50% point of the Latch Enable signal HIGH to LOW transition to the 50% point of an output HIGH to LOW transition.

t_H MINIMUM HOLD TIME - The minimum time after the negative transition of the Latch Enable signal that the input signal must remain unchanged in order to be acquired and held at the outputs.

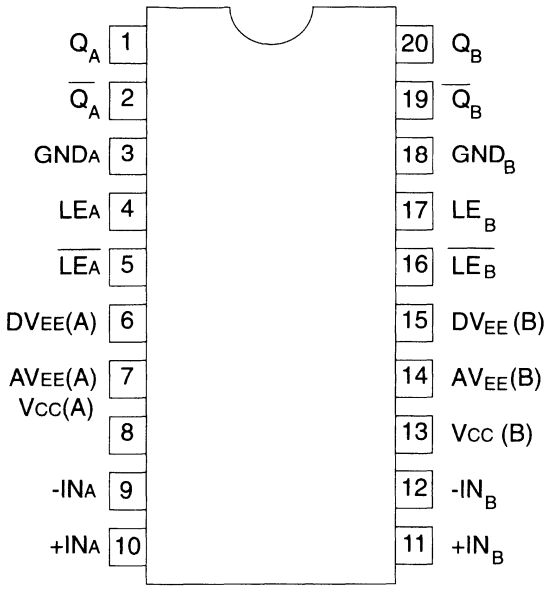
t_{pL} MINIMUM LATCH ENABLE PULSE WIDTH - The minimum time that the Latch Enable signal must be HIGH in order to acquire an input signal change.

t_S MINIMUM SET-UP TIME - The minimum time before the negative transition of the Latch Enable signal that an input signal change must be present in order to be acquired and held at the outputs.

V_{OD} VOLTAGE OVERDRIVE

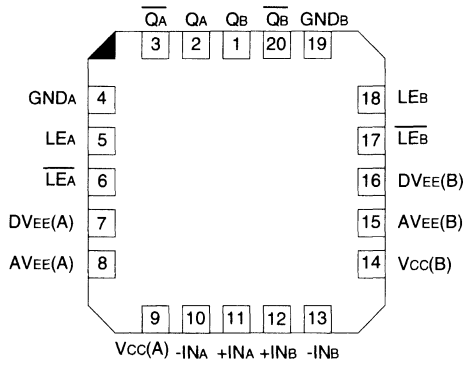
PIN ASSIGNMENTS

TOP VIEW



20 LEAD DIP/PDIP

TOP VIEW



20 CONTACT CERAMIC LCC/PLCC

PIN FUNCTIONS

NAME	FUNCTION
Q_A	Output A
$\overline{Q}_A$	Inverted Output A
GND_A	Ground A
$\overline{LE}_A$	Inverted Latch Enable A
LE_A	Latch Enable A
V_{CC}(A)	Positive Supply Voltage (+10 V)
AV_{EE}(A)	Negative Supply Voltage (-10 V)
DV_{EE}(A)	Negative Supply Voltage (-5.2 V)
V_{CC}(B)	Positive Supply Voltage (+10 V)
AV_{EE}(B)	Negative Supply Voltage (-10 V)
DV_{EE}(B)	Negative Supply Voltage (-5.2 V)
-IN_A	Inverting Input A
+IN_A	Noninverting Input A
+IN_B	Noninverting Input B
-IN_B	Inverting Input B
$\overline{LE}_B$	Inverted Latch Enabled B
LE_B	Latch Enable B
GND_B	Ground B
$\overline{Q}_B$	Inverted Output B
Q_B	Output B

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Section 6 Filters

HSCF24040 7th Order Low Pass, µP Programmable 6-5

6

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SIGNAL PROCESSING TECHNOLOGIES

HSCF24040

PROGRAMMABLE 7TH ORDER LOW PASS ACTIVE FILTER

FEATURES

- 85 dB Dynamic Range
- Cut Off Frequency (fc) up to 20 kHz
- On-Chip Anti-Aliasing Protection
- Programmable Bandedge Frequency for both RC and Switched Capacitor Filter
- S/H Output
- Microprocessor Compatible
- 7th Order Ladder Filter with cosine Prefiltering Stage
- Stopband Attenuation >76 dB at 3 fc
- Programmable DC Gains of 1, 2, 4, 8
- On-Chip Oscillator (External Crystal)

APPLICATIONS

- High Performance Modems
- 12-Bit Signal Processing Systems
- Pre-Sample Anti-Alias Filter
- Test Equipment/Instrumentation
- Spectrum Analyzer
- Medical Telemetry/Filtering
- Speech Analysis and Synthesis
- Data Acquisition Systems
- Computer Controlled Test Systems

6

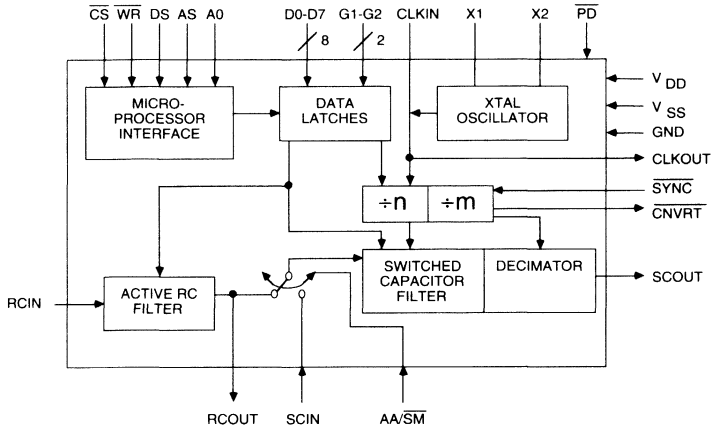
GENERAL DESCRIPTION

The HSCF24040 is a monolithic 7th order low pass active filter system. It offers 76 dB of stop-band attenuation and 85 dB of dynamic range wich makes it the first switched-capacitor filter suitable for 12-bit systems. Because of the internal 3rd order RC anti-aliasing filter, no external components are required for device operation. Both the RC filter and switched-capacitor filter have digitally programmable cut off frequencies.

The last stage of the SC filter contains a programmable decimator which provides a sample/hold output function that reduces the sample rate at SCOUT. This ensures that the hold period of the sample and hold output is long enough to perform an A/D conversion or be resampled by an external S/H.

The HSCF24040 is manufactured using a BEMOS process which allows the fabrication of low power CMOS logic, linear CMOS circuits, bipolar linear circuitry and thin film resistors on a single chip. The HSCF24040 is packaged on a 32 pin DIP, operates on a ±5V supply voltage and is offered in commercial temperature range.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Beyond Which Damage May Occur) (1)

Supply Voltages
- VDD to GND ..... 0 to +7V
- VSS to GND ..... 0 to -7V

Input Voltages
- Digital Input Voltages
  - All except CLKIN, $\overline{CS}$ ..... -0.3V to (VDD +0.3V)
  - CLK, $\overline{CS}$ ..... (VS -0.3V) to (VDD +0.3V)
- Analog Input Voltages
  - SCIN< RCIN ..... (VSS -0.3V) to (VDD +0.3V)

Output Voltages
- Analog Output Voltages
  - SCOUT, RCOUT ..... Momentary Short to VDD

Temperature
- Temperature, case ..... -60 to 140°C
- junction ..... +150°C
- Lead Temperature (soldering 10 seconds) .... +300°C
- Storage Temperature ..... -65 to 150°C

Note (1): Operation at any Absolute Maximum Rating is not implied. See Electrical Specifications for proper nominal applied conditions in typical applications.

ELECTRICAL SPECIFICATIONS

VDD = +5V, VSS = -5V, T_A = 0 to 70°C, unless otherwise specified. All typical specifications are for T_A = 25°C only.

DC ELECTRICAL PARAMETERS	TEST CONDITIONS	TEST LEVEL	MIN	TYP	MAX	UNITS
DC Gain of Combined RCF and SCF:						
HSCF24040ACJ						
SCF Gain Setting = 1.0	SCBW = 5 kHz	I	0.995	1.0	1.005	V/V
SCF Gain Setting = 2.0	RCBW = 7 kHz	I	1.99	2.0	2.01	V/V
SCF Gain Setting = 4.0		I	3.97	4.0	4.03	V/V
SCF Gain Setting = 8.0		I	7.92	8.0	8.08	V/V
DC Gain of RCF Only		I	0.95		1.05	V/V
DC Gain of SCF Only	SCF Gain Setting = 1.0	I	0.95		1.05	V/V
RCOUT Offset Voltage		I	-10		+10	mV
System Pedestal		III		80		mV
Output Drive Capability, RCOUT and SCOUT						
Maximum Voltage Swing	RL = 5 kΩ	I	+3.0			V
Minimum Voltage Swing	RL = 5 kΩ	I			-3.0	V
Maximum Sink/Source Current	RL = 5 kΩ	I	600			µA
Analog Input Voltage Range (1)						
RCIN		I	-3.0		+3.0	V
SCIN; SCF Gain Setting = 1.0		I	-3.0		+3.0	V
SCIN: SCF Gain Setting = 2.0		I	-1.5		+1.5	V
SCIN; SCF Gain Setting = 4.0		I	-0.75		+0.75	V
SCIN; SCF Gain Setting = 8.0		I	-0.375		+0.375	V
Analog Input Impedance						
RCIN Resistance		I	100			kΩ
RCIN Capacitance		II			25	pF
SCIN Resistance		I	50			kΩ
SCIN Capacitance		II			25	pF

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ELECTRICAL SPECIFICATIONS

VDD = +5V, VSS = -5V, T_A = 0 to 70°C, unless otherwise specified. All typical specifications are for T_A = 25°C only.

DC ELECTRICAL PARAMETERS	TEST CONDITIONS	TEST LEVEL	MIN	TYP	MAX	UNITS
POWER SUPPLIES						
Operating Current						
IDD; Normal Mode	XTAL Oscillator Active	I		15	20	mA
IDD; Power Down Mode	XTAL Oscillator Active	I		2	4	mA
ISS; Normal Mode	XTAL Oscillator Active	I		15	18	mA
ISS; Power Down Mode	XTAL Oscillator Active	I		1	3	mA
Power Dissipation						
Normal Mode	XTAL Oscillator Active	I		150		mW
Power Down Mode	XTAL Oscillator Active	I		15		mW
AC ELECTRICAL PARAMETERS						
RC FILTER (RL = 5 kΩ, CL = 50 pF)						
Programmable Bandwidth (Fo, -3dB)		I	7		80	kHz
Bandedge Tolerance, Referenced to Fo		I	-5		+5	%
Passband Response, DC to 0.25Fo Referenced to RCF DC Gain		I	-0.1		+0.1	dB
Stopband Loss, Referenced to RCF DC Gain						
0.25Fo		I			0.2	dB
Fo		I	2	3	4	dB
17.25Fo		I	72			dB
Harmonic Distortion, ±3V Sinusoidal Input at RCIN						
Magnitude of Harmonics		II		-80		dB
THD		I		0.01	0.02	%
Dynamic Range		II	85	90		dB
Integrated Noise Voltage, 0.01Fo to 2.0Fo		II		50	70	µV rms
SC FILTER (RL = 5 kΩ, CL = 50 pF)						
Programmable Bandwidth (Fc=-.1 dB)		I	78		20,000	Hz
Bandedge Tolerance, Referenced to Fc		I	-0.5		+0.5	%
Passband Response, DC to Fc Referenced to SCF DC Gain		I	-0.1		+0.1	dB
SC FILTER (RL = 5kΩ, CL = 50 pF)						
Stopband Loss, Referenced to SCF DC Gain						
1.5Fc		I	30			dB
2.0Fc		I	50			dB
2.5Fc		I	66			dB
3.0Fc		I	76			dB
Harmonic Distortion, ±3V Sinusoidal Input at SCIN						
Magnitude of Harmonics		II		-72		dB
THD		I		0.05	0.075	%

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ELECTRICAL SPECIFICATIONS

VDD = +5V, VSS = -5V, T_A = 0 to 70°C, unless otherwise specified. All typical specifications are for T_A = 25°C only.

AC ELECTRICAL PARAMETERS	TEST CONDITIONS	TEST LEVEL	MIN	TYP	MAX	UNITS
SC FILTER (RL = 5kΩ, CL = 50 pF)						
Dynamic Range		II	85	90		dB
Integrated Noise, Voltage, 0.01Fc to 2.0Fc		II		70	100	µV rms
DIGITAL INPUTS (Pins D0-D7, G1, G2, $\overline{SYNC}$, CLKIN, $\overline{PD}$, AA/$\overline{SM}$, A0, AS, DS, $\overline{CS}$, $\overline{WR}$)						
VIH (Input Voltage High)		I	2.0			V
VIL (Input Voltage Low)		I			0.8	V
IIN (Input Current)		I			1.0	µA
CIN (Input Capacitance)		II			10	pF
DIGITAL OUTPUTS (Pins CLKOUT, $\overline{CNVRT}$)						
VOL (Output Voltage Low)	Driving Standard TTL Load	I			0.4	V
VOH (Output Voltage High)	Driving Standard TTL Load	I	2.4			V
CLOCK FREQUENCY						
Internal Oscillator Frequency	External Xtal	I	1		4	MHz
Input Clock Frequency (Note: 2)		I			4	MHz
MICROPROCESSOR INTERFACE TIMING						
Non-Multiplexed Address/Data bus:						
Tas (Address Setup Time)		I	100			nsec
Tah (Address Hold Time)		I	10			nsec
MICROPROCESSOR INTERFACE TIMING						
Multiplexed Address/Data Bus:						
Tasm (Address Setup Time)		I	20			nsec
Tahm (Address Hold Time)		I	10			nsec
Tds (Data Setup Time)		I	100			nsec
Tdh (Data Hold Time)		I	10			nsec
Tdpw (Data Latch Pulse width, DS or $\overline{WR}$)		I	100			nsec
Taps (Address Latch Pulse Width)		I	50			nsec
Tcsh (Chip Select Hold, $\overline{CS}$ or $\overline{WR}$)		I	10			nsec
SCOUT SYNCHRONIZATION TIMING						
T1 (CLKIN to CLKOUT Delay)		I			50	nsec
T2 ($\overline{SYNC}$ Delay Time)		I	100			nsec
T3 ($\overline{SYNC}$ Setup Time)		I	75			nsec
T4 ($\overline{SYNC}$ Pulse Width) (Note: 3)		I	75			nsec
T5 (CLKIN to $\overline{CNVRT}$ Delay)		I			85	nsec

Notes:

1. Input voltages outside of these ranges will degrade harmonic distortion performance.
2. The minimum input clock frequency is constrained only by the SC filter bandwidth. SC bandwidths below 78 Hz may degrade at high temperatures due to leakage currents.
3. It is required that the external $\overline{SYNC}$ input return to a logic high at least 1 CLKIN clock cycle prior to the falling edge of the next $\overline{CNVRT}$ output.

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TEST LEVEL CODES

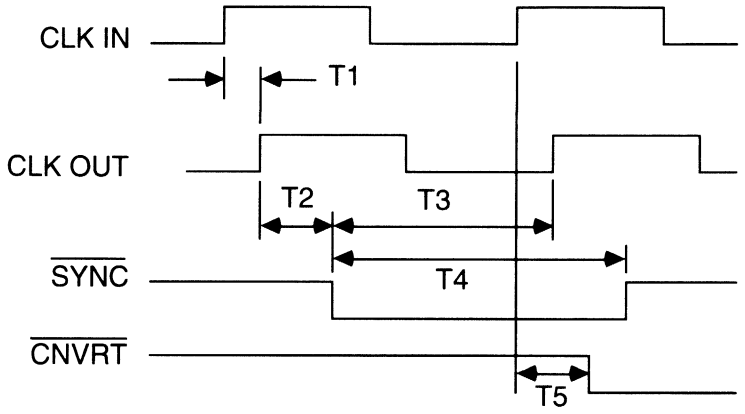
All electrical characteristics are subject to the following conditions:

All parameters having Min./Max. specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality Assurance inspection. Any blank section in the data column indicates that the specification is not tested at the specified condition.

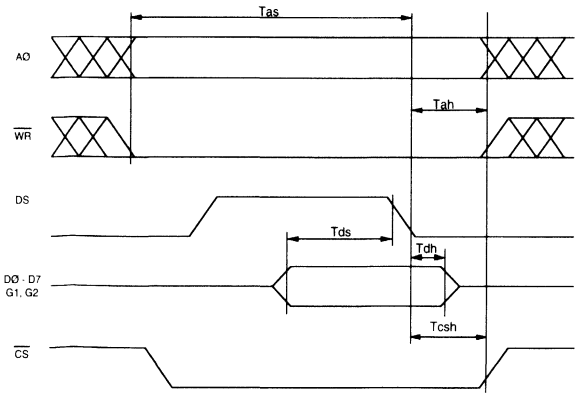
Unless otherwise noted, all tests are pulsed tests, therefore $T_j = T_C = T_A$.

TEST LEVEL	TEST PROCEDURE
I	100% production tested at the specified temperature.
II	100% production tested at T_A = 25 °C, and sample tested at the specified temperatures.
III	QA sample tested only at the specified temperatures.
IV	Parameter is guaranteed (but not tested) by design and characterization data.
V	Parameter is a typical value for information purposes only.

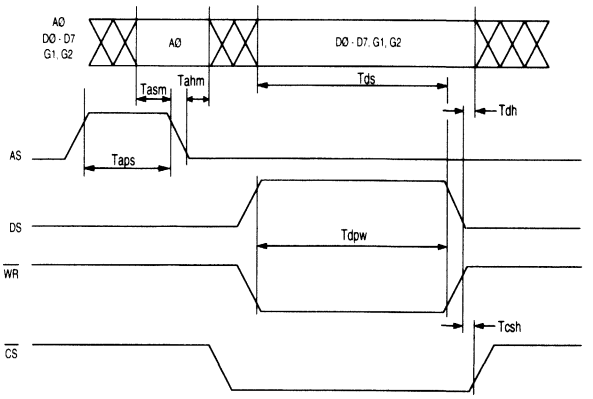
SCOUT SYNCHRONIZATION TIMING



TIMING DIAGRAM FOR NON-MULTIPLEXED BUS



TIMING DIAGRAM FOR MULTIPLEXED BUS



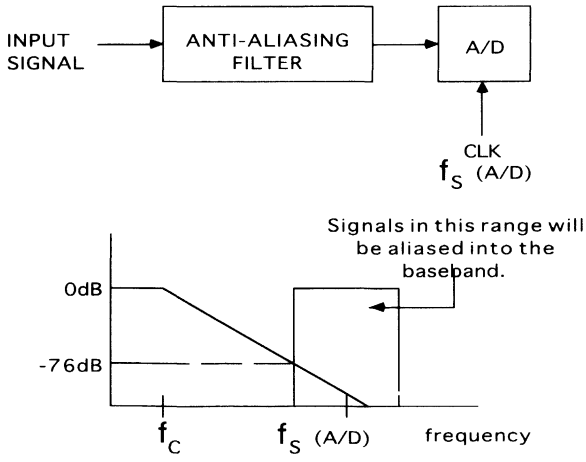
GENERAL DESCRIPTION

(Please refer to AN109 EB105 Evaluation Board and AN111 Analog/Digital Interface Requirements for addional information on the HSCF24040.)

SC FILTER

SC filters are sampled data filters that provide extremely accurate and stable responses. This is because their internal "time constants" depend only upon the switching frequency and the ratios of monolithic capacitors. The switching frequency is normally derived from a crystal controlled oscillator and is thus, extremely precise. On-chip capacitor ratios are accurate to within approximately 0.1%. Therefore, high order sharp rolloff filters can be manufactured that require no post production trimming. Since the filter bandedge can be programmed by varying the frequency of the clock that controls the filters switches, the filter bandedge can be made to track the sample rate of an external A/D converter. The filter in the HSCF24040 has 7 poles (Chebyshev approximation) to insure a minimum loss of 76 dB at 3 times the bandedge so that the system A/D can sample as low as 4 times the bandedge (see Figure 1). The SC filter has a differential signal path to improve its PSRR, distortion, and dynamic range. Through digital programming, bandedges of up to 20 kHz and DC gains of 1, 2, 4, or 8 can be achieved.

Figure 1 - Requirements for an Anti-Aliasing Filter Prior to A/D Conversion



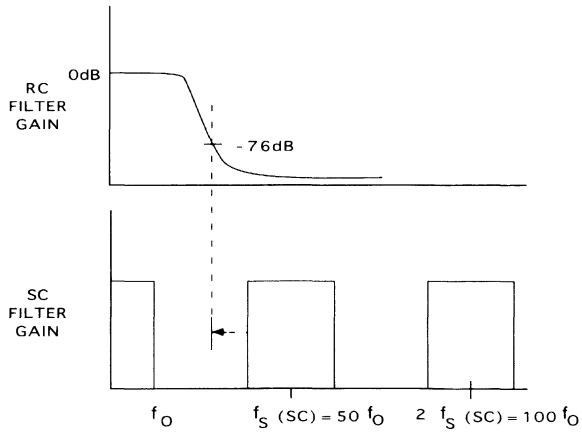
NOTE: Since the filter loss is greater than 76 dB, any aliased signals will be below the 12 bit level.

ACTIVE RC FILTER

Although the SC filter is programmable and offers excellent performance, it does have one major drawback. Because it is a sample data filter, it can fold or alias out-of-band energy into the desired passband in which the same way as the external A/D. Therefore a continuous-time filter is required in front of the SC filter to provide aliasing protection. We are, however, aided by the fact that the filter sampling rate is many times greater than the bandedge frequency (50 times in this case). Thus, a low order, active RC filter with a bandedge accuracy of only 5% will suffice. This concept is illustrated in Figure 2. The bandedge for this RC filter must be programmable to insure sufficient rejection of the SC filter images located at multiples of the SC filter rate. Eight different RC filter bandedges spanning a 12-to-1 range are available on the HSCF24040. The programmability is achieved by switching different resistor and capacitor values into the filter. A single RC filter bandwith setting (3 dB) of f_0 (RCF) will provide 76 dB of anti-aliasing protection for SC filter bandwidths ranging from f_0 (RCF)/5.71 to f_0 (RCF)/4.

The topology of the RC filter has been chosen so that the DC gain and the pole Q's rely on ratio matching of the on-chip resistors and capacitors. The RC filter bandedge is laser trimmed for high accuracy during the manufacturing process.

Figure 2 - RC Filter Provides Anti-Aliasing for SC Filter



NOTE: The RC filter should provide >76 dB of loss for several different SC filter sample rates f_s (SC).

DECIMATOR

The decimator block samples the differential output of the SC filter and converts it to a single ended signal. The decimator also provides a sample-and-hold output (SCOUT) at a pro-

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grammable sample rate of 25fc, 12.5fc, 6.25fc, or 4.167fc, where fc is the SC filter bandwidth. By choosing the proper decimation rate, the hold time at SCOUT will be sufficiently long to allow an A/D conversion to take place. (An external sample and hold may be required for hold times longer than 100 µsec to prevent more than 1/2 LSB of droop for a 12-bit A/D converter).

The $\overline{\text{CNVRT}}$ output is an active low digital output that indicates when the SCOUT output is valid. Applying a falling edge to the $\overline{\text{SYNC}}$ input initiates the $\overline{\text{CNVRT}}$ pulse on the next rising edge of CLKOUT. The use of the decimator block with $\overline{\text{SYNC}}$ and $\overline{\text{CNVRT}}$ insures the proper timing interface between SCOUT and an external A/D converter or sample and hold and eliminates the need for a smoothing filter at the SCOUT output.

PROGRAMMABILITY

The chip contains an 8-bit and a 2-bit data register. Data in the 8-bit register controls the SC filter bandedge, RC filter bandedge, and the decimation rate. (A programmable divide down chain generates the SC filter clocks from the master clock. A similar divide down chain determines the decimation rate from the SC filter clocks). Data in the 2-bit register controls the programmable D.C. gain of the SC filter. The truth tables for both registers are shown in Table I.

Table I - Programmable Features

RCF BANDEDGE				DC GAIN		
RCF 3dB BW	D7	D6	D5	DC GAIN	G1	G2
80KHz	0	0	0	1	1	1
56KHz	0	0	1	2	1	0
40KHz	0	1	0	4	0	1
28KHz	0	1	1	8	0	0
20KHz	1	0	0			
14KHz	1	0	1			
10KHz	1	1	0			
7KHz	1	1	1			

CLOCK TO SCF BANDEDGE DIVIDE DOWN RATIO				DECIMATOR SAMPLE RATE		
fCLK/fc	D0	D1	D2	fS/H/fc	D3	D4
200	0	0	0	25.000	0	0
400	0	0	1	12.500	0	1
800	0	1	0	6.250	1	0
1,600	0	1	1	4.167	1	1
3,200	1	0	0			
6,400	1	0	1			
12,800	1	1	X			

fc = 0.1dB bandwidth of the SC filter.
fCLK = Master clock frequency at CLKOUT.
fS/H = Sample rate at SCOUT output.

The SC filter's bandedge is programmed by selecting one of the divide down ratios shown in Table I. This ratio is divided into the master clock frequency to arrive at the filter cutoff frequency. As an example, assuming a typical master clock frequency of 4 MHz and a divide down ratio of 400 (D0, D1, D2=001), the filter's bandedge would be 10 kHz. Alternately, selecting a divide down ratio of 3200 (D0, D1, D2=100) would provide a filter bandedge of 1250Hz. With a constant master clock frequency, up to seven discrete SC filter bandedges can be obtained. An inifinite number of different bandedges can be derived by varying both the divide down ratios and the master clock frequency. This provides the ultimate level in programming flexibility.

For the sidebrazed package, direct microprocessor interface is available: The five control signals, A0, AS, $\overline{\text{WR}}$, $\overline{\text{CS}}$, and DS, allow the user to directly interface to 8-bit microprocessors without additional glue logic. Both Motorola's MPX'ed and non-MPX'ed bus formats as well as Intel's MPX'ed bus format are supported. Interface connections for both the Intel and Motorola 8-bit microprocessors are shown in Table II. In addition to the data-latch format, the D0-D7 and G1-G2 inputs can be hardwired for direct programming without the need for a latch signal by tying the $\overline{\text{CS}}$ input to VSS. A0=1 selects the BW registers D0-D7 and A0=0 selects the gain registers G1, G2.

Table II - Microprocessor Interface Connections

HSCF24040	INTEL (MPX'ED) 8088, 8085, 8051	MOTOROLA (MPX'ED) 6801, 6803	MOTOROLA (NON-MPX'ED) 680D, 6801, 6802, 6809
$\overline{\text{CS}}$	Generated from A8-A15	Generated from A8-A15	Generated from A0-A15
DS	VDD Supply	E	E
$\overline{\text{WR}}$	$\overline{\text{WR}}$	R/$\overline{\text{WR}}$	R/$\overline{\text{WR}}$
A0	ADi	ADi	Ai
AS	ALE	AS	ADD Supply
D0-D7	AD0-AD7	AD0-AD7	D0-D7
G1-G2	ADi	ADi	Di

NOTE: Tying $\overline{\text{CS}}$ to the VSS Supply disables the microprocessor interface and allow D0-D7, G1-G2 to be programmed directly without the need for a latch signal.

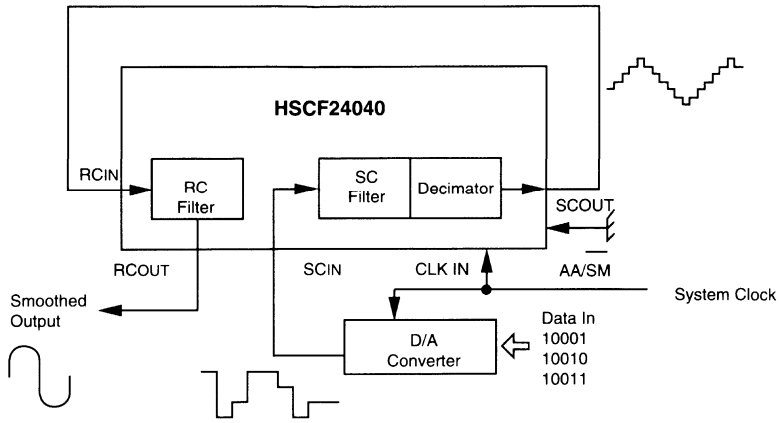
OSCILLATOR

The HSCF24040 provides an on-chip oscillator (external crystal) for applications where a system clock is not available. The user has a choice of either the clock driven or oscillator mode. The oscillator mode is enabled by tying the CLKIN input to VSS.

TYPICAL APPLICATION CIRCUIT

Figure 3 illustrates how the HSCF24040 might be used for smoothing the output from a D/A converter. In this case, the D/A output is fed into the SCIN input of the device. The SCIN input is enabled by tying AA/SM to ground. The SCOUT output is fed externally into the RCIN input. The smoothed output is finally brought off-chip via the RCOUT pin. (Note that the smoothed output will not correct the inherent sin (X)/(X) droop of the original D/A converter output).

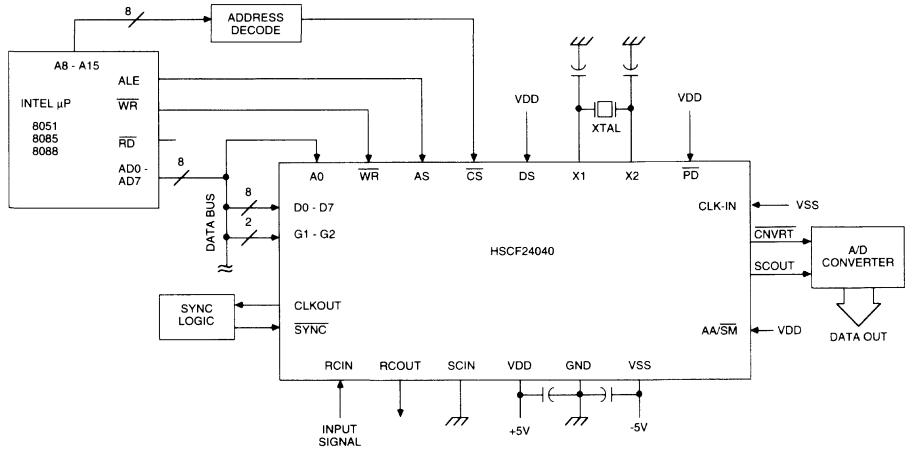
Figure 3 - HSCF24040 as a Smoothing Filter For a D/A Converter



The HSCF24040 can be used as the band limiting filter for a 12-bit data acquisition system as shown in Figure 4. The basic function of the device is to bandlimit the input signal so that unwanted, out-of-band signals are not aliased (folded) into the desired passband. The input signal enters the HSCF24040 through RCIN and is processed by the RC filter. The signal is then processed by the switched-capacitor filter, and finally the decimator to facilitate its interface with the A/D converter. Figure 1 shows that for a 12-bit system the filter must provide at least 75 dB of loss at the frequency fs-fc (where fs is the sampling rate of the A/D converter and fc is the desired channel bandwidth).

In many applications the user may want a programmable channel bandwidth. An instrument that records signals that range from 100 Hz to 20 kHz would require that the A/D sample rate be variable. Figure 1 shows that the required filter bandwidth is directly proportional to the sample rate of the A/D converter. The filtering necessary for the multiple sampling rates can be accomplished by using the programmable bandwidth capability of the HSCF24040 to adjust the desired filter response to the sample rate. This eliminates the need for a parallel bank of fixed bandwidth anti-aliasing filters, one for each sample rate.

Figure 4 - The HSCF24040 as an Anti-Aliasing Filter in a 12-bit Data Acquisition System



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PIN ASSIGNMENT HSCF24040

TOP VIEW

PIN FUNCTIONS HSCF24040

NAME	FUNCTION
VSS	Negative supply voltage
$\overline{CS}$	Chip select; active low
G1-G2	The digital inputs that control the DC gain of the SC filter
D0-D7	The digital inputs that control the RC filter bandedge, SC filter bandedge, and SC filter decimation rate.
$\overline{SYNC}$	This digital input conrols the sampling instant for the SC filter decimated output; active low.
CLKOUT	Master clock output capable of driving 1 standard TTL load. It is a buffered version of either CLKIN or the internally generated crystal oscillator output.
VDD	Positive supply voltage
$\overline{CNVRT}$	This digital output indicates that the SCOUT output has settled and can now be converted or sampled (drive capability is 1 standard TTL load); active low.
X1-X2	An external crystal is connected between these pins to generate an accurate clock for chip operation.
CLKIN	The master clock input. Forcing CLKIN to VSS enables the on-chip oscillator (external crystal).
GND	Ground
SCOUT	SC filter output
$\overline{PD}$	This digital input is used to power down the analog circuitry; active low
RCOUT	RC filter output
RCIN	RC filter input
SCIN	SC filter input (only valid when AA/$\overline{SM}$ is forced low)
$\overline{WR}$	Write strobe; active low
DS	Data strobe
AA/$\overline{SM}$	This digital input controls whether the input to the SC filter comes from RCOUT or SCIN
AS	Address strobe
A0	Register address select

LEADERSHIP IN DATA CONVERSION AND SIGNAL PROCESSING

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SPT112

VOLTAGE REGULATOR WITH RESET OUTPUT

FEATURES

- Low Dropout Voltage
- CMOS/TTL Compatible ON/OFF Switch
- Very Low Standby Current 180 μA (ON, No Load)
- Internal Thermal Shutdown
- Short Circuit Protection
- Very Low (0.1 μA) Current in OFF Mode
- Low Noise with External Bypass Capacitor
- 130 mA Current Capability

APPLICATIONS

- Battery Powered Systems
- Cellular Telephones
- Pagers
- Personal Communications Equipment
- Portable Instrumentation
- Portable Consumer Equipment
- Radio Control Systems
- Toys
- Low Voltage Systems

GENERAL DESCRIPTION

The SPT112XX is a low power, linear regulator with a built-in electronic switch. The internal electronic switch can be controlled by TTL or CMOS logic levels. The device is in the ON state when the control pin is pulled to a high logic level. A pin for a bypass capacitor is provided, which connects to the internal circuitry, to lower the overall output noise level.

An internal PNP pass-transistor is used in order to achieve low dropout voltage (typically 100 mV at 30 mA load current). The device has very low quiescent current (180 μA) in the ON mode with no load and 1 mA with 30 mA load. The quiescent current is typically 2.5 mA at 60 mA load. When the device is in standby mode (V_{CONT} = 0) , the quiescent current is typically 100 nA. An internal thermal shutdown circuit limits the junction temperature to below 150 °C. The load current is internally monitored and the device will shut down in the presence of a short circuit at the output.

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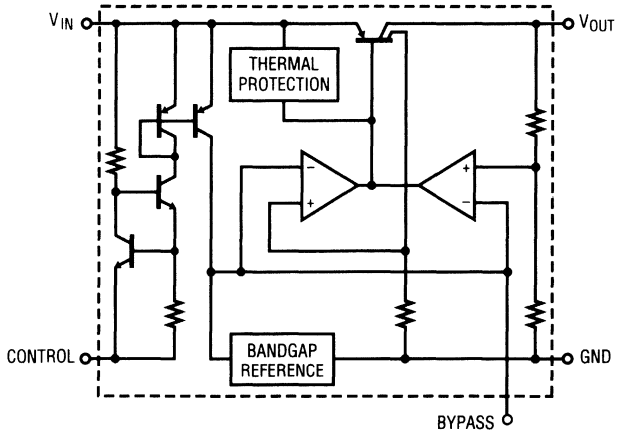
BLOCK DIAGRAM



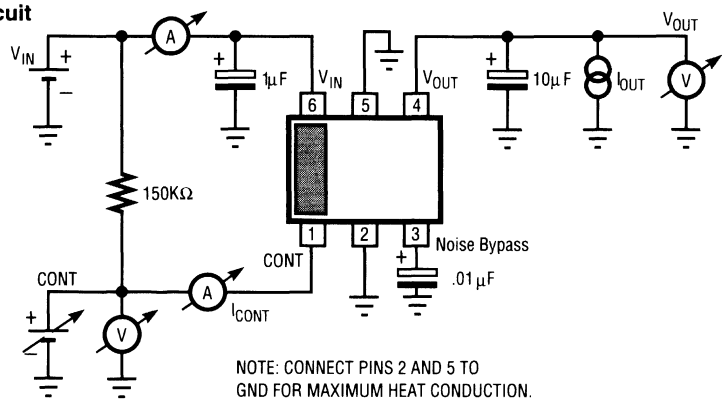
ELECTRICAL SPECIFICATIONS

T_A=+25 °C, unless otherwise specified.

PARAMETERS	TEST CONDITIONS	SYMBOL	MIN	TYP	MAX	UNITS
Supply Current 1	I_O=0 mA, Except I_{CONT}	I_{cc1}		180		µA
Supply Current 2	V_{IN}=8 V, Output OFF	I_{CC2}			100	nA
Output Voltage	$V_{IN}=V_O$+1 V, I_O=30 mA	V_O	-3	V_O	+3	%
Output Voltage			-100	V_O	+100	%
Dropout Voltage	I_O=30 mA	V_{DROP}		0.1		V
Output Current	Note 3	I_O	150	180		mA
Recommended I_O					130	mA
Line Regulation	$V_{IN}=V_O$+ (1~6 V)	Line Reg			0.12	%/V
Load Regulation	I_O=0~60 mA, Note 4	Load Reg			0.03	%/mA
Ripple Rejection	100 mVRMS, f=400 Hz, I_O=10 mA	RR		60		dB
Temperature Coefficient	V_O+1.5 V					
V_O Temperature Dependency	V_O=+1.5 V, T_A=-25 to +75 °C			0.2		mV/°C
Output Noise Voltage	10 Hz<80 kHz, I_O=10 mA	V_{NO}		0.2		µV(rms)
CONTROL TERMINAL SPECIFICATIONS						
Control Terminal Current	Output ON, V_{CONT} =2.4 V	I_{CONT1}		15	40	µA
Control Terminal Volt. I	Output ON	V_{CONT1}	2.4			V
Control Terminal Volt. I	Output OFF	V_{CONT2}			0.6	V
Output Rise Time	I_O=60 mA, V_{CONT} =0~2.4 V	T_R		0.2	1.0	msec
Bypass Terminal Voltage				1.25		V

Note 1: Power dissipation must be derated at rate of 1.6 mW/°C for operation at 25 °C and over. Power dissipation = 400 mW (When mounted as recommended.)
Note 2: Output side capacitor should have low ESR at low temperatures if used below 0 °C.
Note 3: I_O (Load Current) is the measured current when V_O drops 0.3 V with respect to (V_O at I_O = 30 mA).
Note 4: This measurement (pulse measurement) is with a constant T_J. The output change due to temperature change is not included.

Figure 1 - Test Circuit



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TYPICAL PERFORMANCE CHARACTERISTICS

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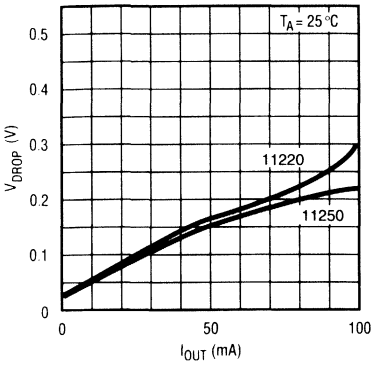
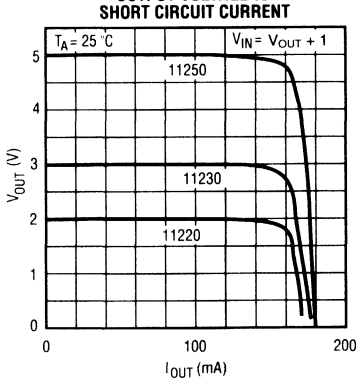
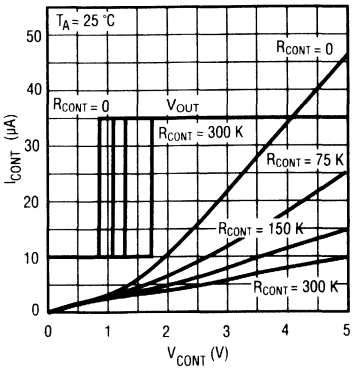
DROPOUT VOLTAGE vs LOAD CURRENT



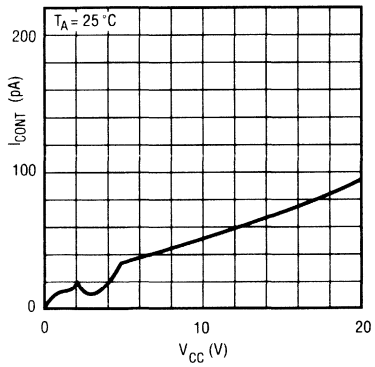
OUTPUT VOLTAGE vs SHORT CIRCUIT CURRENT



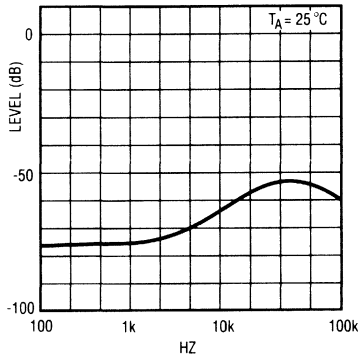
CONTROL TERMINAL CIRCUIT CURRENT vs CONTROL TERMINAL VOLTAGE



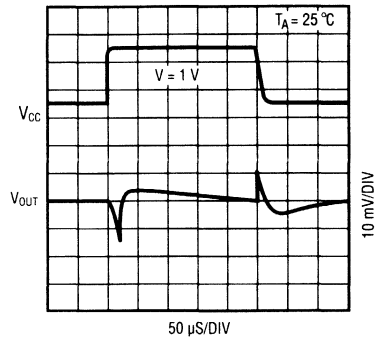
QUIESCENT CURRENT vs INPUT VOLTAGE



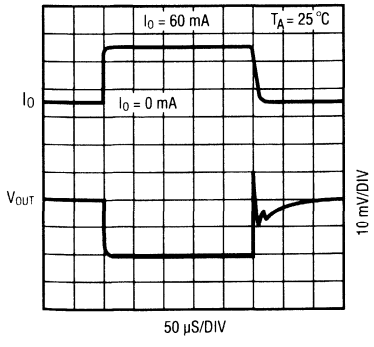
RIPPLE REJECTION



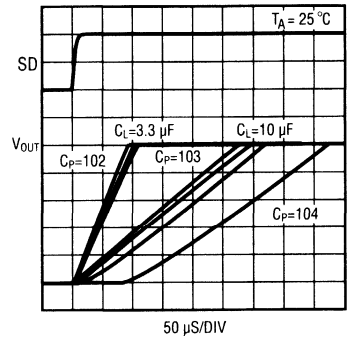
LINE TRANSIENT RESPONSE



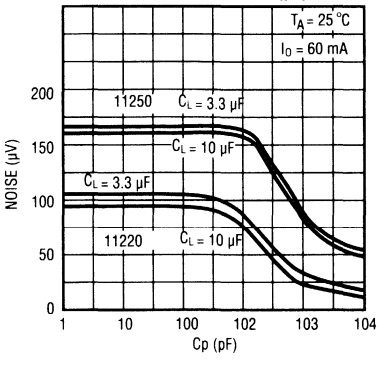
LOAD TRANSIENT RESPONSE



SHUTDOWN CONTROL (OFF-ON)



NOISE LEVEL vs BYPASS CAPACITOR(pF)



TYPICAL PERFORMANCE CHARACTERISTICS

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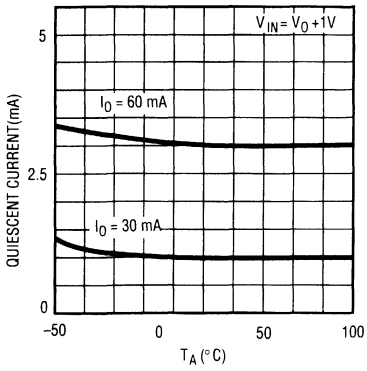
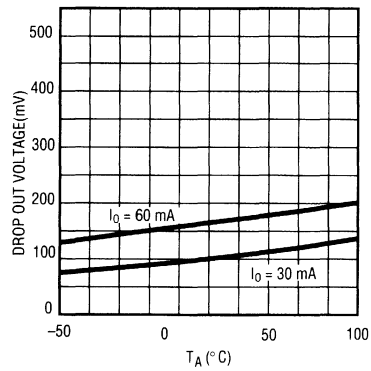
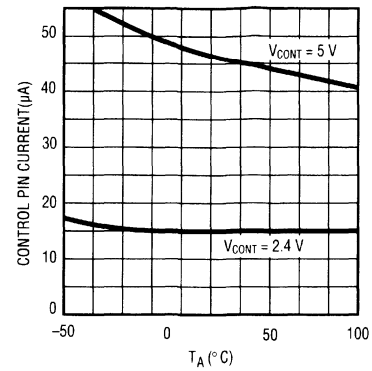
QUIESCENT CURRENT vs TEMPERATURE



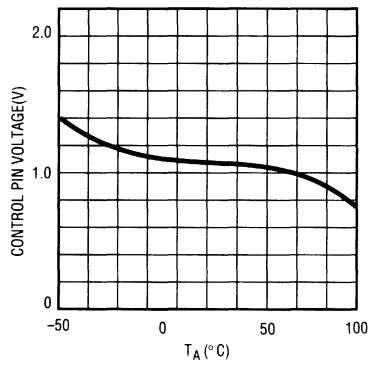
DROPOUT VOLTAGE vs TEMPERATURE



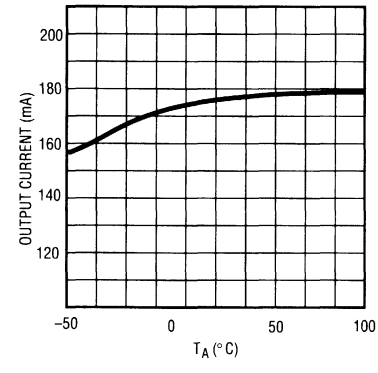
CONTROL PIN CURRENT vs TEMPERATURE



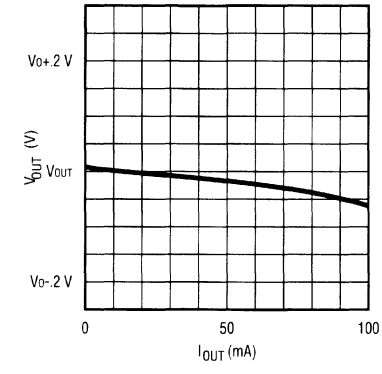
CONTROL PIN VOLTAGE vs TEMPERATURE



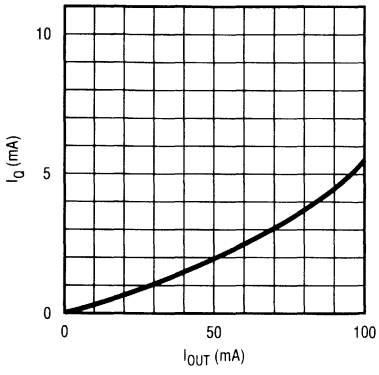
OUTPUT CURRENT vs TEMPERATURE



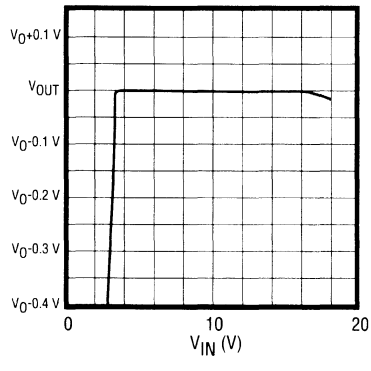
OUTPUT VOLTAGE vs OUTPUT CURRENT



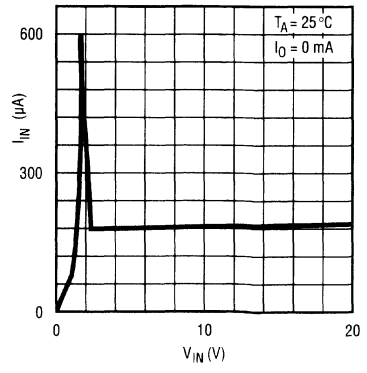
QUIESCENT CURRENT vs LOAD CURRENT



OUTPUT VOLTAGE vs INPUT VOLTAGE



INPUT CURRENT vs INPUT VOLTAGE



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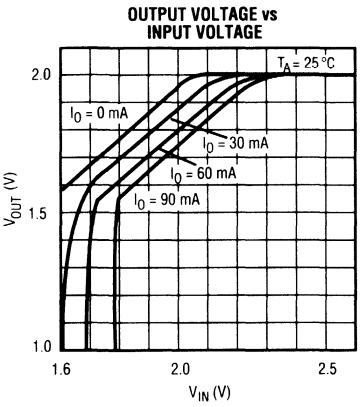
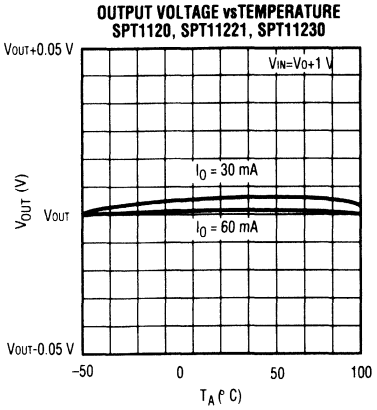
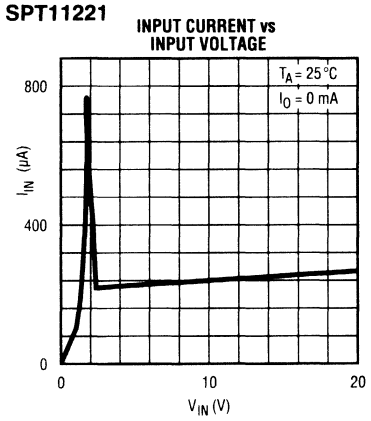
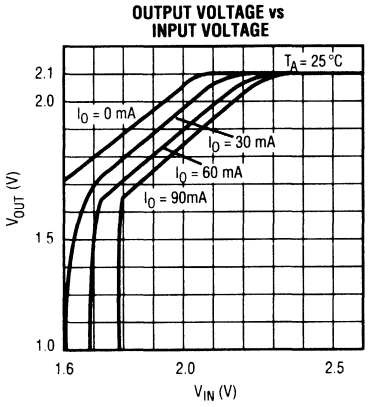


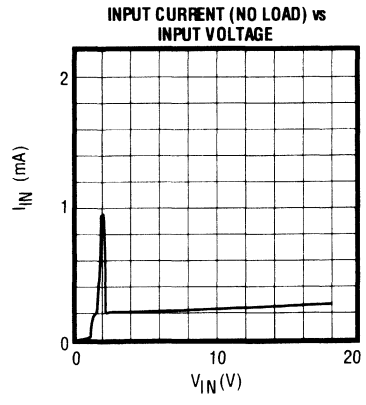


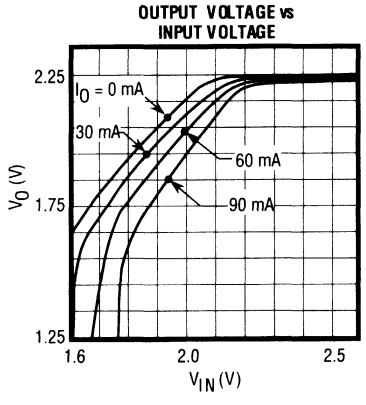
SPT11221

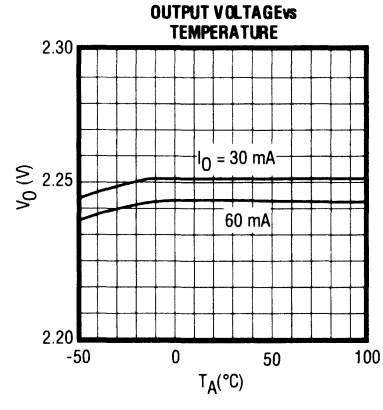




SPT11222

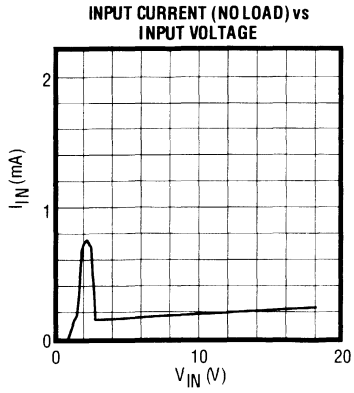


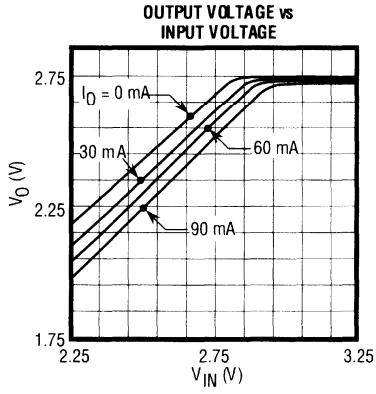


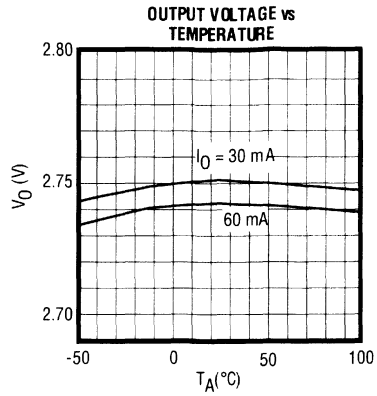


TYPICAL PERFORMANCE CHARACTERISTICS

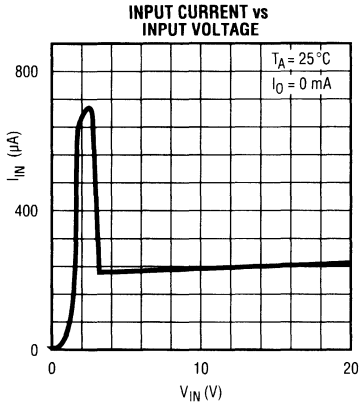
SPT11227

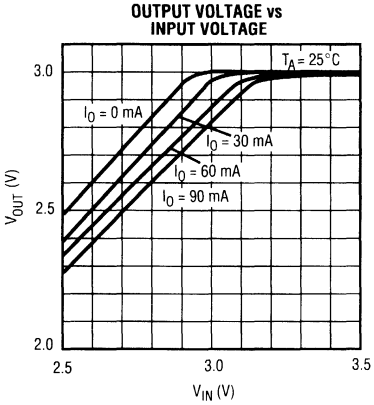




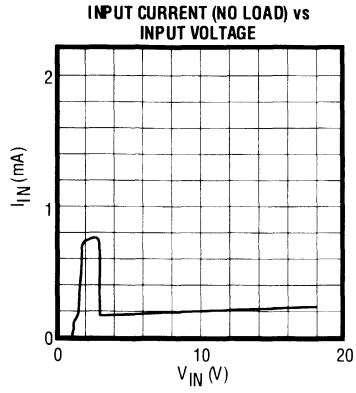


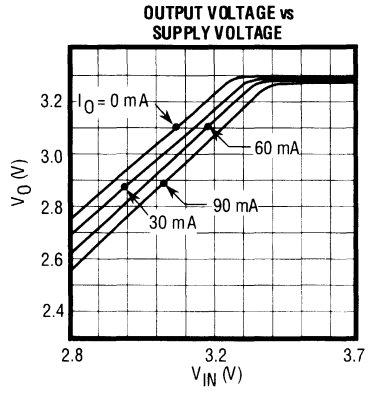
SPT11230

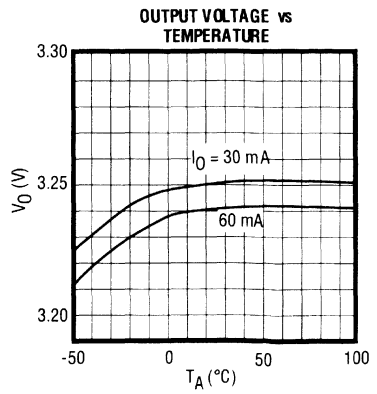




SPT11232







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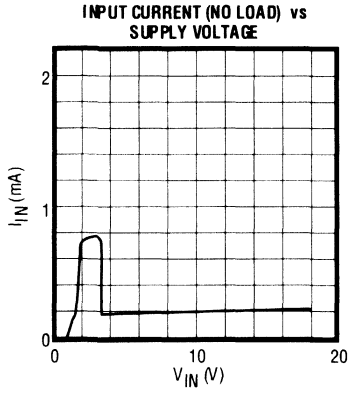
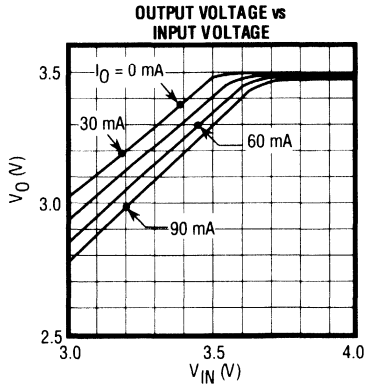
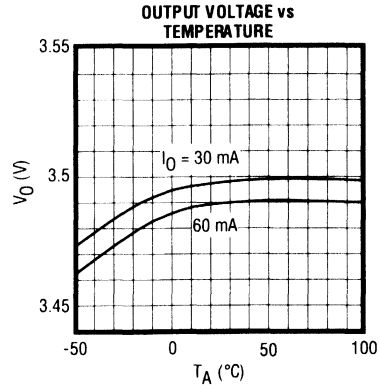
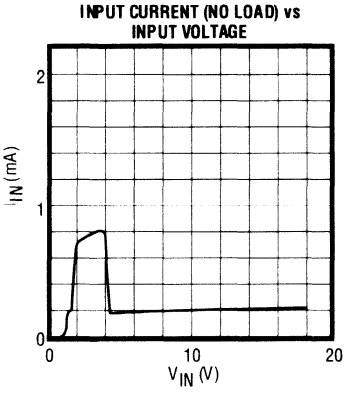
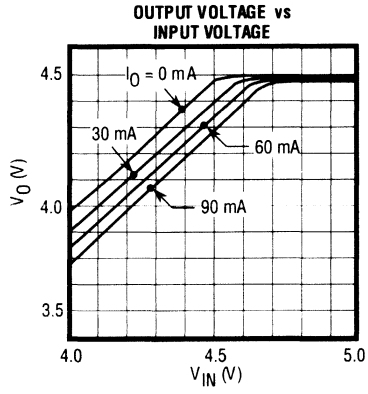


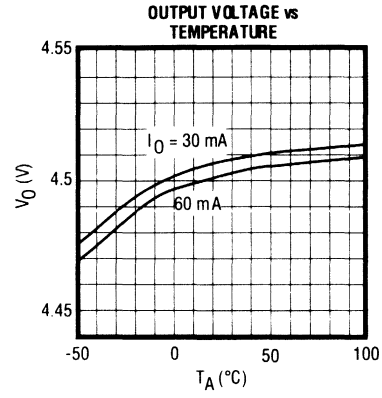




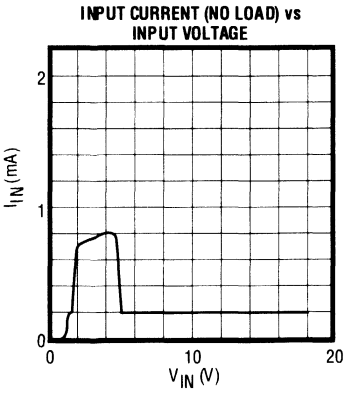
SPT11245

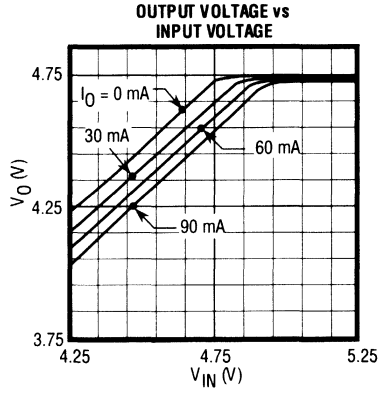


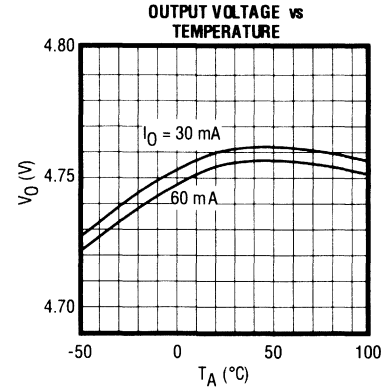




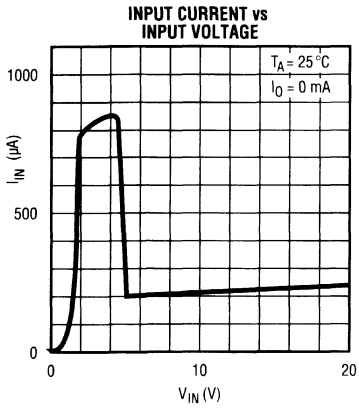
SPT11247

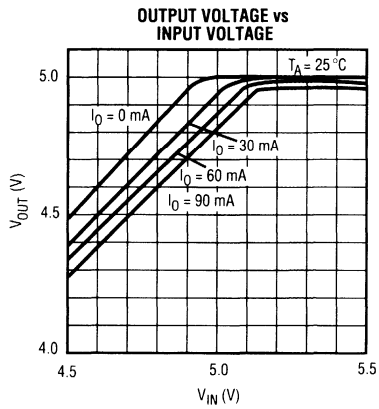


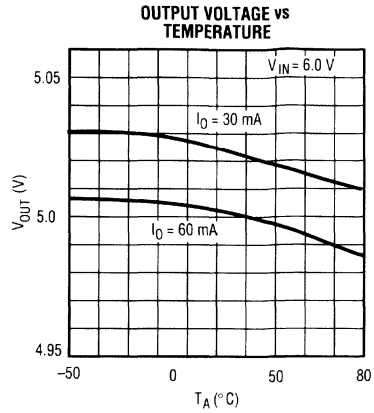




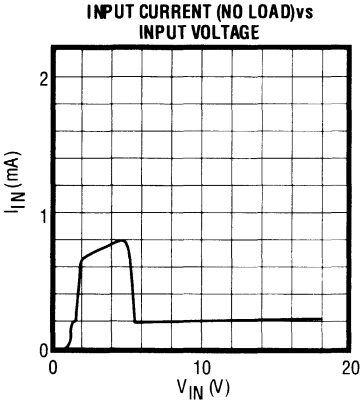
SPT11250

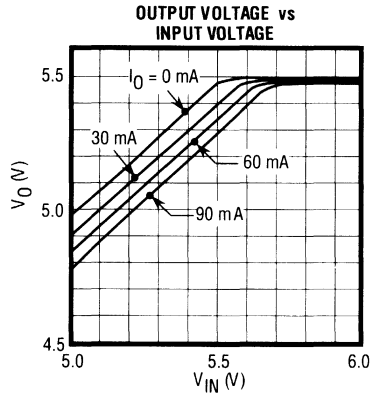


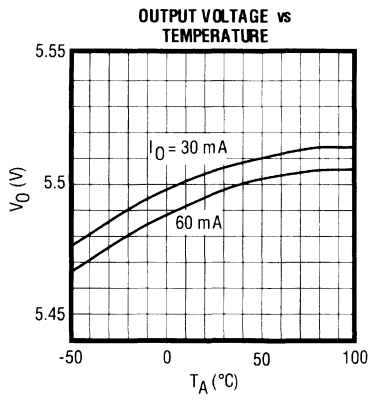




SPT11255







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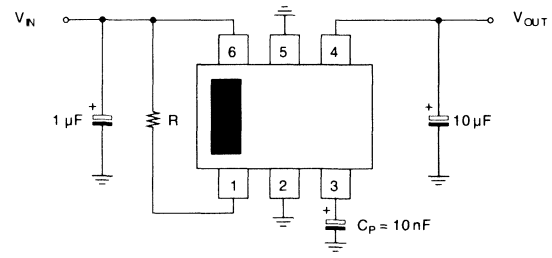
APPLICATIONS INFORMATION

DISABLING THE CONTROL PIN

Connect control terminal to V_{CC} through R. Higher resistance values are good for reducing quiescent current but can cause the regulator to drop out at a higher voltage. (0 Ω <R< 300 kΩ.) See figure 2.

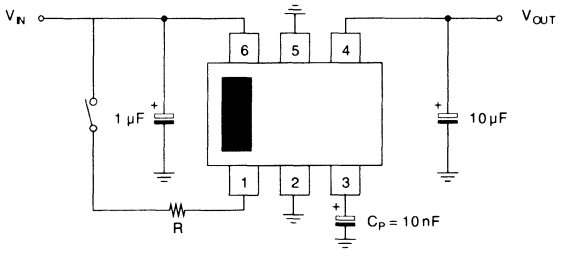
Figure 2



USING THE CONTROL FUNCTION

Turn on the regulator by setting the control pin voltage to the same level as V_{IN}. Turn off the regulator by grounding the control pin. See figure 3.

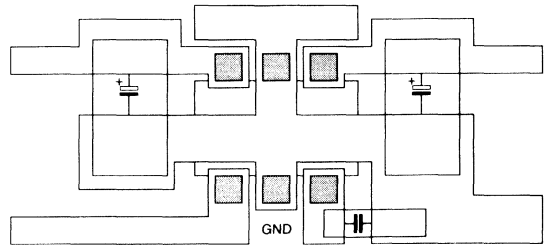
Figure 3



HEAT DISSIPATION

Make the copper pattern as large as possible to provide good heat dissipation (pin 5 is the heatsink).
P_D = 400 mW (When mounted as recommended)
See figure 4.

Figure 4



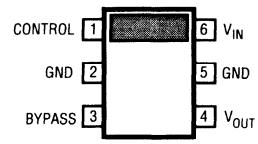
BYPASS CAPACITOR

Connect the bypass capacitor as close as possible to the GND terminal of IC (Pin 5,2), otherwise oscillation may occur. Use a 3.3 µF tantalum capacitor, or 5.6 µF electrolytic to ensure stability. (T_A = 25 C) For low temperatures, select a capacitor with low ESR at the desired temperature range. Use as large a capacitor as needed to meet transient, output impedance, and noise requirements. The noise bypass pin has high impedance, and it is sensitive to external noise if C_P is not used.

HANDLING MOLDED RESIN PACKAGES

All Plastic molded packages absorb some moisture from the air. If moisture absorption occurs prior to soldering the devise into the printed circuit board, increased separation of the lead from the plastic molding may occur, degrading the moisture barrier characteristics of the device.
This property of plastic molding compounds should not be overlooked, particularly in the case of very small packages, where the plastic is very thin.
In order to preserve the original moisture barrier properties of the package, devices are stored and shipped in moisture proof bags, filled with dry air. The bags should not be opened or damaged prior to the actual use of the devices. If this is unavoidable, the devices should be stored in a low relative humidity environment (40 to 65%) or in an enclosed environment with desiccant.

PIN ASSIGNMENT



LEADERSHIP IN DATA CONVERSION AND SIGNAL PROCESSING

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SPT114

VOLTAGE REGULATOR WITH ON/OFF SWITCH

FEATURES

- Low Dropout Voltage
- Electronic ON/OFF Switch
- Very Low Standby Current (ON, No Load)
- Internal Thermal Shutdown
- Short Circuit Protection
- Very Low (<100 nA) Current in OFF Mode
- Available on Tape and Reel
- Customized Versions Are Available

APPLICATIONS

- Battery Powered Systems
- Cellular Telephones
- Pagers
- Personal Communications Equipment
- Portable Instrumentation
- Portable Consumer Equipment
- Radio Control Systems
- Low Voltage Systems

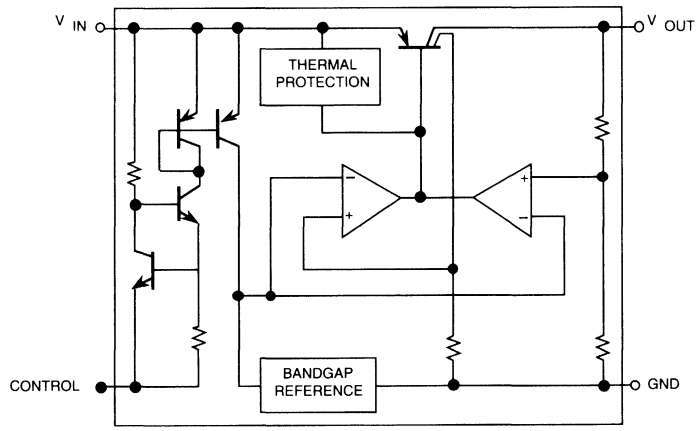
GENERAL DESCRIPTION

The SPT114 series of devices are low power, linear regulators. Each regulator can be turned ON and OFF by an internal electronic switch which is controlled by an external control signal.

The Internal PNP pass-transistor is used in order to achieve low dropout voltage (typically 200 mV at 50 mA load current). The device has very low quiescent current (500 μA) in the ON mode with no load and 2 mA with 30 mA load. The quiescent current is typically 4 mA at 60 mA load. An internal thermal shutdown circuit limits the junction temperature to below 150 °C. The load current is internally monitored and the device will shut down (no load current) in the presence of a short circuit at the output. The regulated output voltage may be specified in 0.5 V increments between 2.0 to 6.0 V. Additionally, 3.25 V and 8.0 V versions are also available.

The device is available in a plastic SOT-23L package. Tape and reel mounted devices are also available.

BLOCK DIAGRAM



SPT 4755 Forge Road, Co. Springs, CO 80907
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ABSOLUTE MAXIMUM RATINGS (BEYOND WHICH DAMAGE MAY OCCUR) 25[1] °C

Supply Voltage ..... 14 V
Output Voltage ..... V_{OUT} x1.15 V
Load Current ..... 180 mA
Power Dissipation (Note 2) ..... 200 mW

Storage Temperature Range ..... -55 to +150 °C
Operating Temperature Range ..... -40 to +85 °C
Lead Soldering Temp (10 sec) ..... +240 °C
Junction Temperature ..... +150 °C

ELECTRICAL SPECIFICATIONS

$T_A=T_{MIN}$ - T_{MAX} unless otherwise specified.

PARAMETERS	TEST CONDITIONS	SYMBOL	MIN	TYP	MAX	UNITS
Supply Voltage Range		V_{IN}	2.5		14	V
Supply Current 1	$V_{IN}=V_{OUT}$ + 1 V, I_O=0 mA	I_{IN1}		500	900	µA
Supply Current 2	$V_{IN}=V_{OUT}$ -(1 V to 0.1 V), I_O = 0 mA	I_{IN2}		1.0	2.5	mA
Supply Current 3	V_{IN}=10 V, V_{OUT} = OFF Mode	I_{IN3}				
	T_A=-20 °C to +70 °C			0.1	2.0	mA
	T_A=-40 °C to +85 °C			0.1	3.0	mA
Regulated Output Voltage	$V_{IN}=V_{OUT}$ + 1 V, I_{OUT}=30 mA	V_O				
	T_A=25 °C		-3.5		+3.5	%
			-100		+100	mV
	T_A=-20 °C to +70 °C		-4.5		+4.5	%
			-130		+130	mV
	T_A=-40 °C to +85 °C		-5.0		+5.0	%
			-140		+140	mV
Dropout Voltage 1	V_O=30 mV	V_{DROP}		0.12	0.3	V
Output Current	T_A=-20 °C to +70 °C	I_O		110		mA
	T_A=-40 °C to +85 °C			100		mA
Recommended Output Current		I_{OR}			70	mA
Line Regulation	V_{OUT} +1 V ≤ V_{IN} ≤ V_{OUT}+6.0 V	Line Reg		2	20	mV
Load Regulation	V_{IN} = V_O +1 V, I_O = 0-60 mA	Load Reg		35	110	mV
Control Pin Current		I_{CONT}		35	120	µA
Control Pin Voltage	Off Mode	V_{COFF}	V_{IN}-0.2 V		V_{IN}	V
Control Pin Voltage	On Mode	V_{CON}	0		V_{IN}-1.0 V	V
Ripple Rejection	100 mVRMS, f=400 Hz	RR		55		dB
	$V_{IN}=V_O$ + 1.5 V, I_O=10 mA					
V_O Temperature Coefficient	$V_{IN}=V_O$ + 1.5 V, I_{OUT}=10 mA	ΔV/ΔT		0.6		mV/°C
Output Noise Voltage	$V_{IN}=V_O$ + 1.5 V, I_O=10 mA	V_N				
	CL = 10 µF			180		mV_{RMS}

Note 1: Operation at any Absolute Maximum Rating is not implied. See Operating Conditions for proper nominal applied conditions in typical applications.
Note 2: Derates above T_A=25 °C at 1.6 mW/°C.

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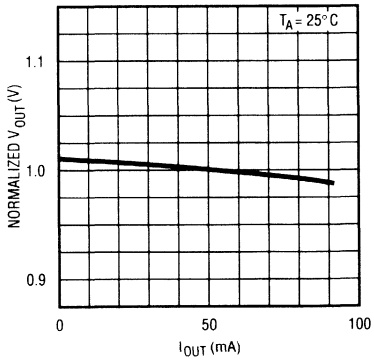
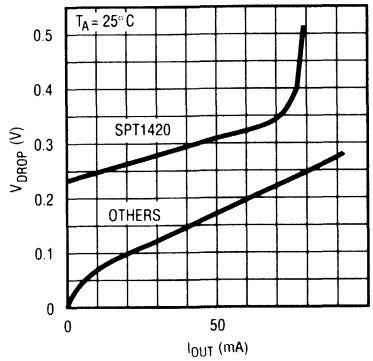
TYPICAL PERFORMANCE CHARACTERISTICS

PART NUMBER	OUTPUT VOLTAGE(V)
SPT11420	2.0
SPT11425	2.5
SPT11430	3.0
SPT11432	3.2
SPT11435	3.5
SPT11440	4.0
SPT11445	4.5
SPT11450	5.0
SPT11455	5.5
SPT11460	6.0
SPT11480	8.0

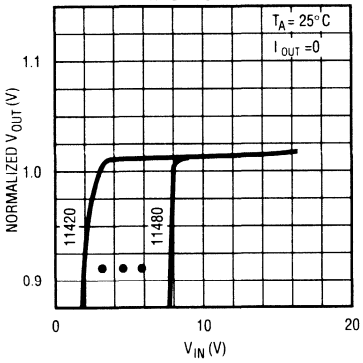
OUTPUT VOLTAGE vs OUTPUT CURRENT



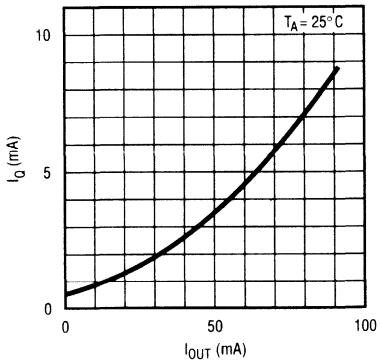
DROPOUT VOLTAGE vs LOAD CURRENT



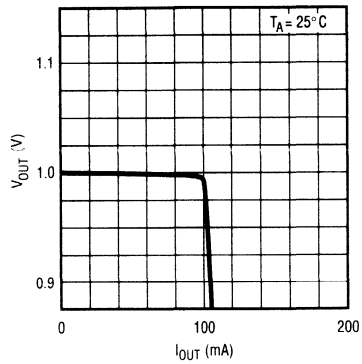
OUTPUT VOLTAGE vs INPUT VOLTAGE



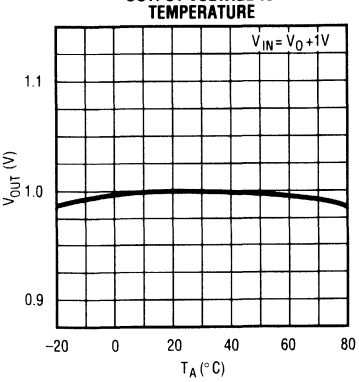
QUIESCENT CURRENT vs LOAD CURRENT



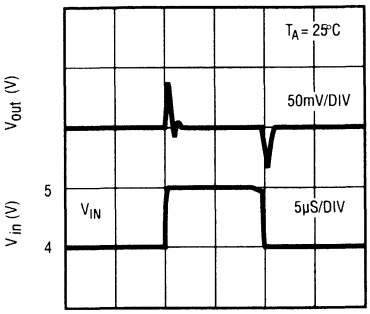
SHORT CIRCUIT PROTECTION



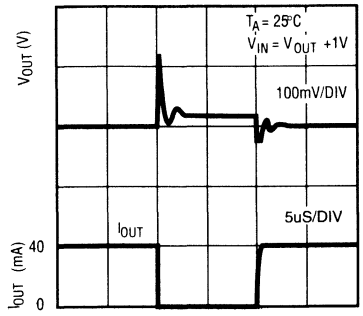
OUTPUT VOLTAGE vs TEMPERATURE



LINE TRANSIENT RESPONSE

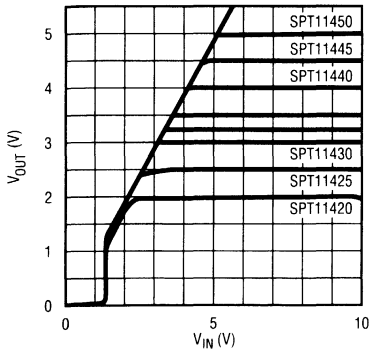


LOAD TRANSIENT RESPONSE

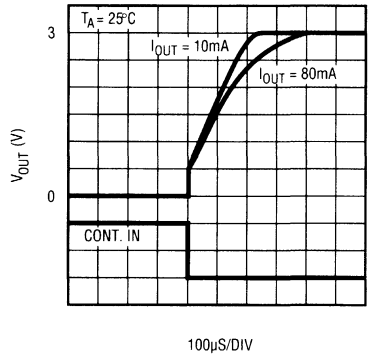


TYPICAL PERFORMANCE CHARACTERISTICS

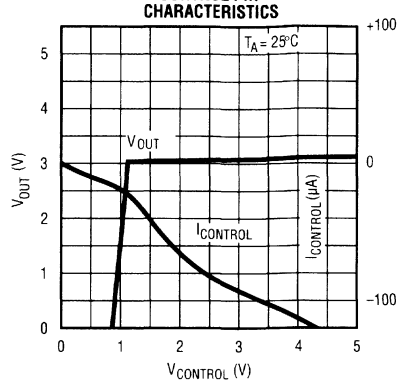
INPUT OUTPUT CHARACTERISTICS (SWITCH ON)



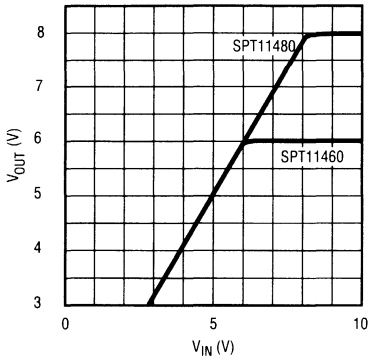
TURN ON TRANSIENT RESPONSE



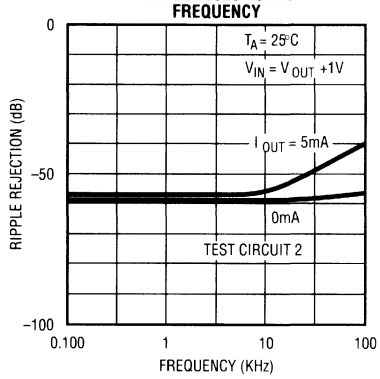
CONTROL PIN CHARACTERISTICS



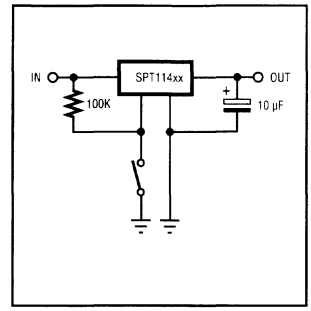
INPUT OUTPUT CHARACTERISTICS (SWITCH ON)



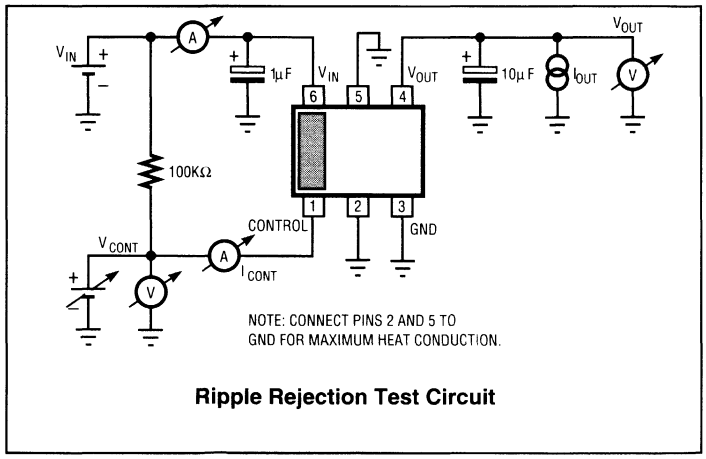
RIPPLE REJECTION vs FREQUENCY



Test Circuit 1



Test Circuit 2



Ripple Rejection Test Circuit

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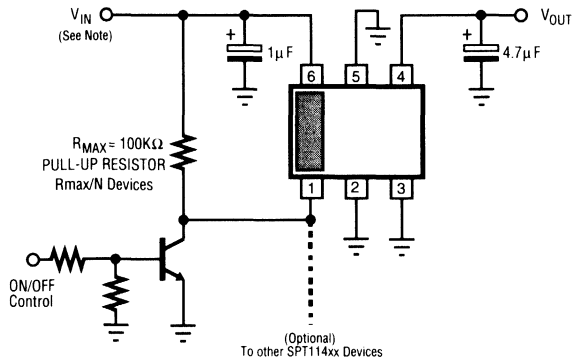
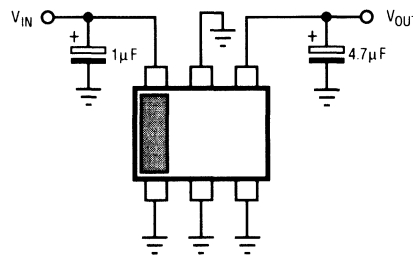
TYPICAL APPLICATIONS

CONTROL FUNCTION UTILIZED

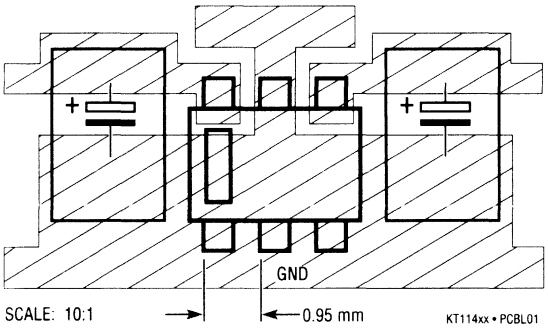


CONTROL FUNCTION NOT UTILIZED



Note: Parallel connection of control pins is allowed if all devices use identical input voltage.

PRINTED CIRCUIT BOARD LAYOUT



APPLICATION HINTS

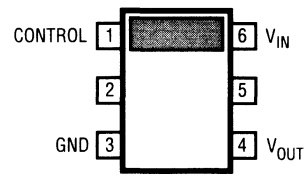
Maximize copper foil area connecting to all IC pins for optimum performance. Place input and output bypass capacitors close to the GND pin. For best transient behavior and lowest output impedance, use as large of a capacitor value as possible. The temperature coefficient of the capacitance and Equivalent Series Resistance (ESR) should be taken into account. These parameters can influence power supply noise and ripple rejection. In extreme cases, oscillation may occur. In order to maintain stability, the output bypass capacitor value should be minimum 2.2 µF in case of Tantalum electrolytic or 4.7 µF in case of Aluminium electrolytic.

HANDLING MOLDED RESIN PACKAGES

All plastic molded packages absorb some moisture from the air. If moisture absorption occurs prior to soldering the device into the printed circuit board, increased separation of the lead from the plastic molding may occur, degrading the moisture barrier characteristics of the device. Do not overlook this property of plastic molding compounds, paticularly with small packages in which the plastic is very thin.

In order to preserve the original moisture barrier properties of the package, devices are stored and shipped in moisture proof bags, filled with dry air. The bags should not be opened or damaged prior to the actual use of the devices. If this is unavoidable, the devices should be stored in a low relative humidity environment (40 to 65%) or in an enclosed environment with desicant.

PIN ASSIGNMENT



LEADERSHIP IN DATA CONVERSION AND SIGNAL PROCESSING

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SIGNAL PROCESSING TECHNOLOGIES

SPT115

VOLTAGE REGULATOR WITH ON/OFF SWITCH

FEATURES

- Low Noise and Dropout Voltage
- Pass Transistor Terminals Available
- Very Low Standby Current (ON, No Load)
- Very Low (<100 nA) Current in OFF Mode
- Small Outline Surface Mount Package
- Internal Thermal Shutdown
- Short Circuit Protection
- Available on Tape and Reel
- Customized Versions Available

APPLICATIONS

- Cordless Telephones
- Pagers
- Battery Powered Systems
- Personal Communications Equipment
- Portable Instrumentation
- Radio Control Systems
- Low Voltage Systems
- Portable Consumer Equipment

GENERAL DESCRIPTION

The SPT115 series devices are low power, linear regulators with electronic ON/OFF switches. Both active HIGH and active LOW control pins are provided.

An internal PNP pass-transistor is used in order to achieve low dropout voltage (typically 200 mV at 80 mA load current). The base of the internal pass transistor is available at pin 7 for parallel connection of an external pass transistor in case higher current or lower dropout voltage is required.

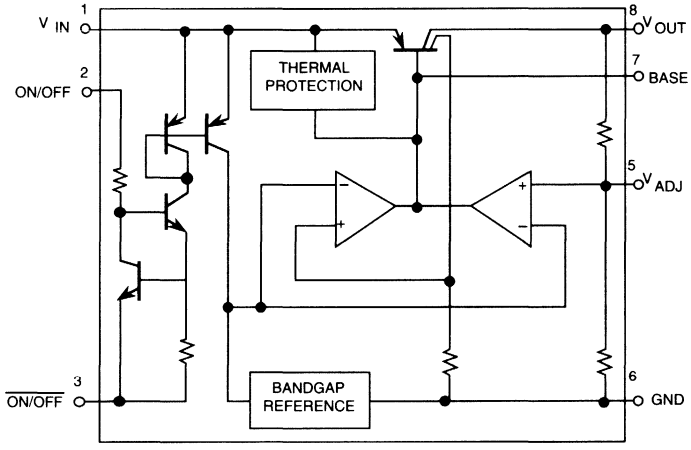
The regulated output voltage may be specified in 0.5 V increments between 2.5 to 5.5 V. Additionally, 3.2 V, 4.7 V and 8 V output versions are also available.

The devices operate at very low (500 µA) quiescent current with no load, 2 mA with 40 mA load, and 3 mA with 60 mA load. An internal thermal shutdown circuit limits the junction temperature to below 150 °C. The load current is internally monitored, and the device will shut down in the presence of a short circuit at the output.

The SPT115 is available in an 8-lead plastic surface mount package. Tape and reel mounted devices are also available.

7

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Beyond which damage may occur)[1] 25 °C

Supply Voltage ..... 14 V
Output Voltage ..... V_{OUT} x1.15 V
Load Current ..... 180 mA
Power Dissipation (Note 2) ..... 600 mW

Storage Temperature Range ..... -55 to +150 °C
Operating Temperature Range ..... -40 to +85 °C
Lead Soldering Temp (10 sec) ..... +260 °C
Junction Temperature ..... +150 °C

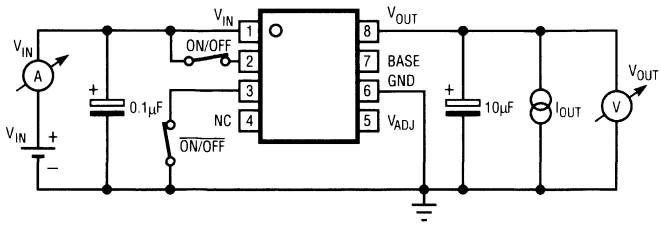
ELECTRICAL SPECIFICATIONS Unless otherwise specified, $T_A=T_{MIN}$ - T_{MAX}, Note 3

PARAMETERS	TEST CONDITIONS	SYMBOL	MIN	TYP	MAX	UNITS
Supply Voltage Range			2.5		14	V
Supply Current 1	$V_{CC} = V_{OUT}$ + 1 V, I_{OUT} = 0 mA	I_{IN1}		500	900	µA
Supply Current 2	OFF Mode, VIN = <10 V	I_{IN2}		0.1	2.0	µA
Regulated Output Voltage	$V_{IN} = V_{OUT}$ + 1 V, I_O = 30 mA	V_O				
	T_A = +25 °C		-3.5		+3.5	%
			-100		+100	mV
	T_A = -20 to +70 °C		-4.5		+4.5	%
			-120		+120	mV
	T_A = -40 to +85 °C		-5.0		+5.0	%
			-130		+130	mV
Dropout Voltage	I_{OUT} = 60 mA	V_{DROP}		170	350	mV
Output Current		I_O	100			mA
Line Regulation	V_{OUT} + 1.0 V≤V_{IN}≤V_{OUT}+6.0 V	Line Reg		5	50	mV
Load Regulation	I_{OUT} = 0 to 60 mA	LD_{REG}		30	120	mV
Ripple Rejection	$V_{IN} = V_{OUT}$ + 1.5 V, I_{OUT} = 10 mA f = 400 Hz, 100 mV RMS	V_{RIPPLE}		55		dB
V_{OUT} Temp Coefficient		ΔV/ΔT		±0.35		mV/°C
Output Noise Voltage	10 Hz< f< 100 kHz , I_O=10 mA	V_N			180	μV_{RMS}
Base Sink Current (Pin 7)				10		mA
Output On/Off Control						
High Level Control	Connect pin 3 to GND, Use pin 2	OFF			0.5	V
		ON	2.4		V_{IN}	V
Low Level Control	Connect pin 2 to V_{CC}, Use pin 3	OFF	V_{CC} - 0.2 V		VIN	V
		ON			V_{CC} - 2.4	V

Note 1: Operation at any Absolute Maximum Rating is not implied. See Operating Conditions for proper nominal applied conditions in typical applications.
Note 2: Derate above T_A=25 °C at 4.8 mW/°C.
Note 3: Some specifications may not apply to all versions of output voltage. Example: V_{OUT} tolerance is ±4% for SPT11520, STP11525 and SPT11530. Detailed specifications are available for each version.

TYPICAL PERFORMANCE CHARACTERISTICS AT 25 °C

TEST CIRCUIT 1



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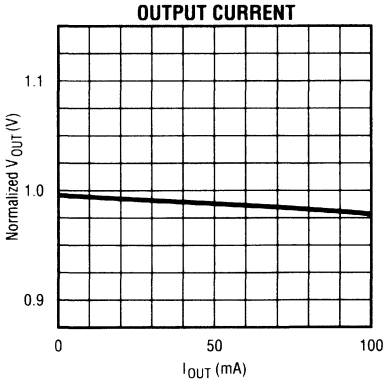
TYPICAL PERFORMANCE CHARACTERISTICS AT 25 °C

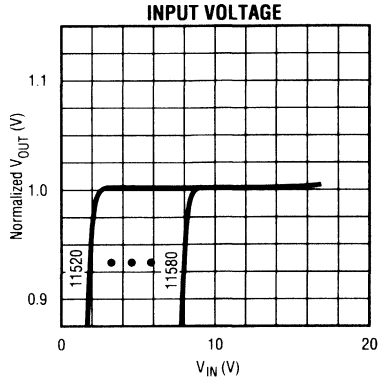
GRAPHS ASSOCIATED WITH TEST CIRCUIT 1

PART NUMBER	OUTPUT VOLTAGE(V)
SPT11520	2.0
SPT11525	2.5
SPT11530	3.0
SPT11532	3.2
SPT11535	3.5
SPT11540	4.0
SPT11545	4.5
SPT11547	4.7
SPT11550	5.0
SPT11555	5.5
SPT11580	8.0

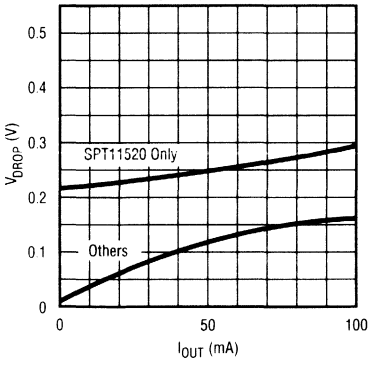
OUTPUT VOLTAGE vs OUTPUT CURRENT



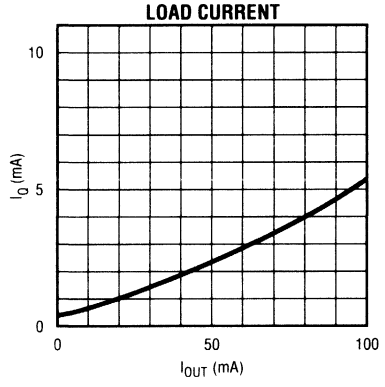
OUTPUT VOLTAGE vs INPUT VOLTAGE



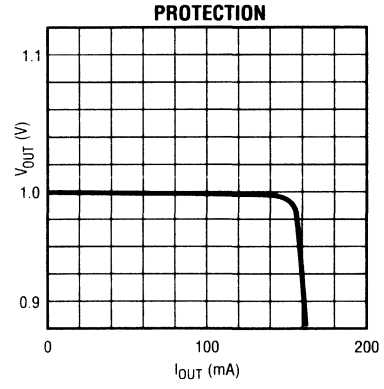
DROPOUT VOLTAGE vs LOAD CURRENT



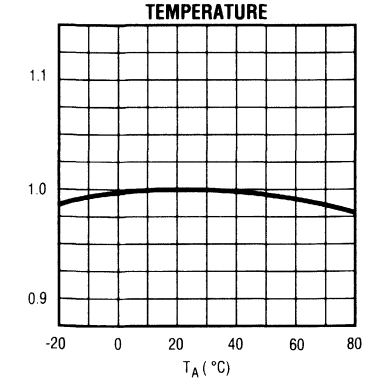
QUIESCENT CURRENT vs LOAD CURRENT



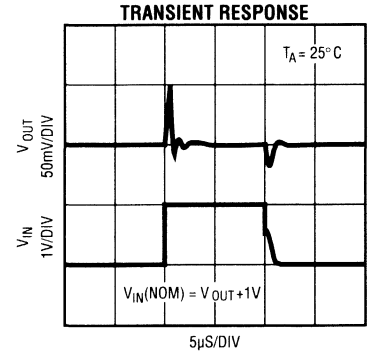
SHORT CIRCUIT PROTECTION



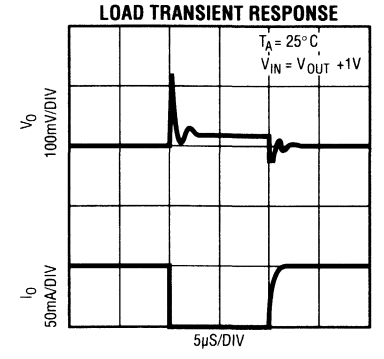
OUTPUT VOLTAGE vs TEMPERATURE



LINE TRANSIENT RESPONSE

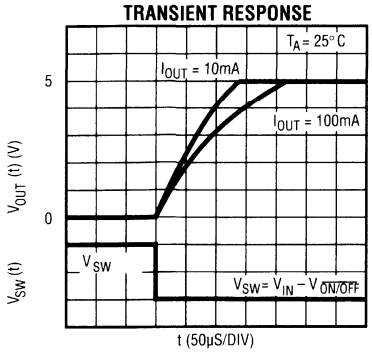


LOAD TRANSIENT RESPONSE

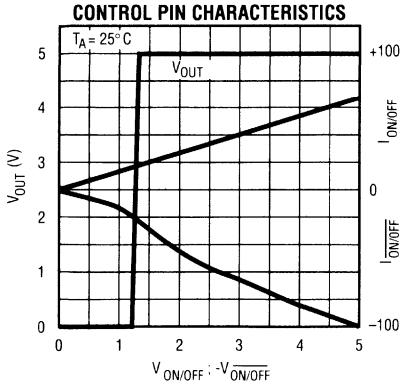


TYPICAL PERFORMANCE CHARACTERISTICS AT 25 °C

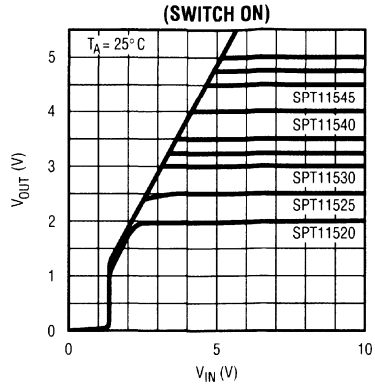
TURN ON TRANSIENT RESPONSE



CONTROL PIN CHARACTERISTICS

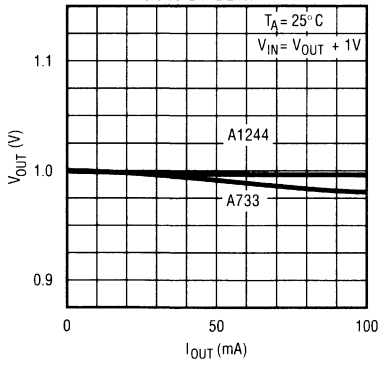


INPUT OUTPUT CHARACTERISTICS (SWITCH ON)

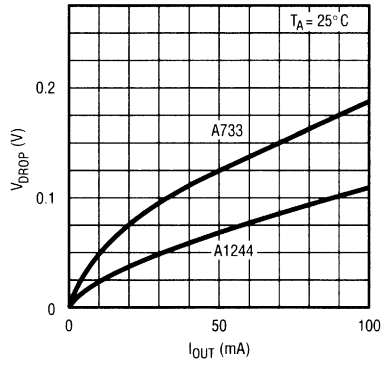


COMMON CHARACTERISTICS OF THE SPT11550 WITH EXTERNAL CURRENT BOOST TRANSISTOR (NEC 2SA733 OR TOSHIBA 2SA1244). SEE TYPICAL APPLICATIONS CIRCUIT ENTITLED ACTIVE HIGH CONTROL WITH CURRENT BOOST.

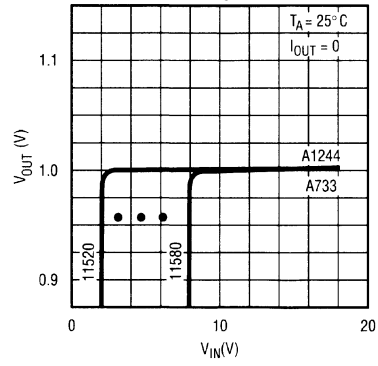
OUTPUT VOLTAGE vs OUTPUT CURRENT



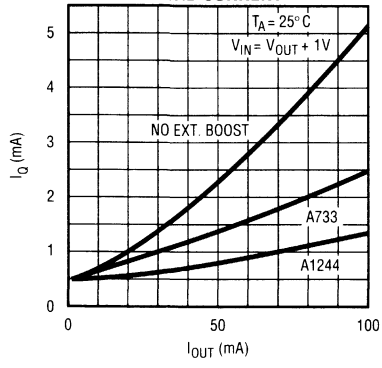
DROPOUT VOLTAGE vs LOAD CURRENT



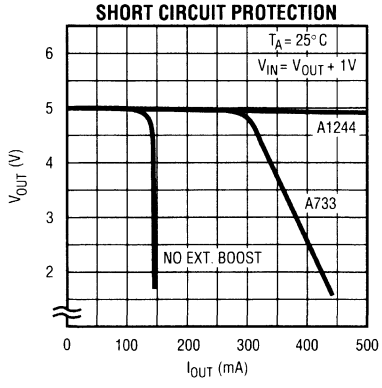
OUTPUT VOLTAGE vs INPUT VOLTAGE



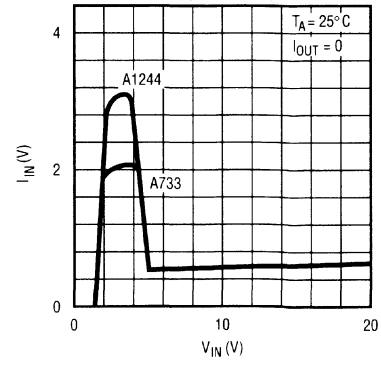
QUIESCENT CURRENT vs LOAD CURRENT



SHORT CIRCUIT PROTECTION



INPUT CURRENT vs INPUT VOLTAGE



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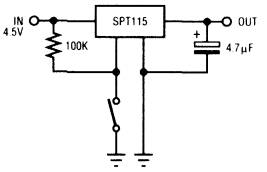
TYPICAL PERFORMANCE CHARACTERISTICS AT 25 °C

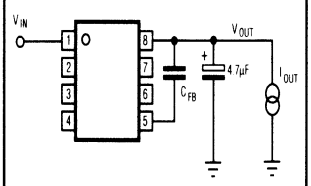
ADDITIONAL TEST CIRCUITS AND ASSOCIATED GRAPHS

TEST CIRCUIT 2



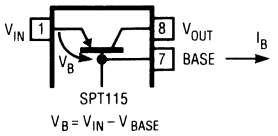
RIPPLE REJECTION TEST

TEST CIRCUIT 3



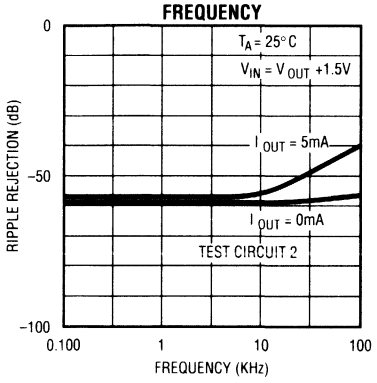
NOISE LEVEL TEST CIRCUIT

TEST CIRCUIT 4

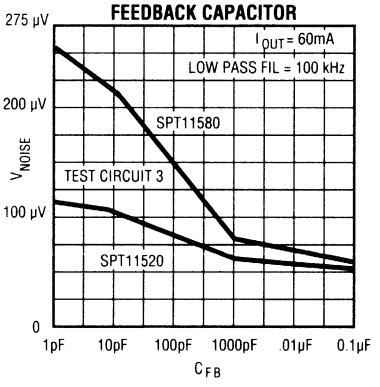


INTERNAL PASS TRANSISTOR

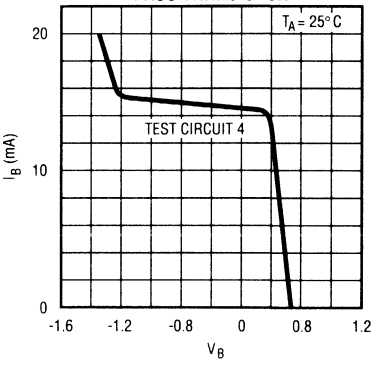
RIPPLE REJECTION vs FREQUENCY



NOISE LEVEL vs FEEDBACK CAPACITOR



INTERNAL PASS TRANSISTOR



APPLICATION HINTS

Maximize copper foil area connecting to all IC pins for optimum performance. Place input and output bypass capacitors close to the GND pin. For best transient behavior and lowest output impedance, use as large of a capacitor value as possible. The temperature coefficient of the capacitance and Equivalent Series Resistance (ESR) should be taken into account. These parameters can influence power supply noise and ripple rejection. In extreme cases, oscillation may occur. In order to maintain stability, the output bypass capacitor value should be minimum 1 µF in case of Tantalum electrolytic or 4.7 µF in case of Aluminium electrolytic at T_A= 25 °C.

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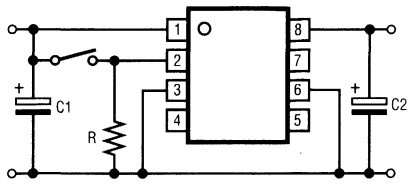
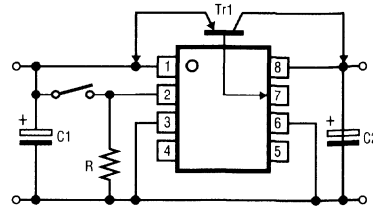
TYPICAL APPLICATIONS

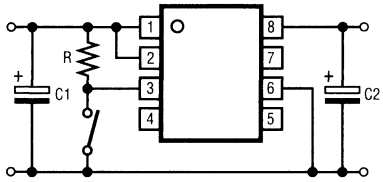
ACTIVE HIGH CONTROL



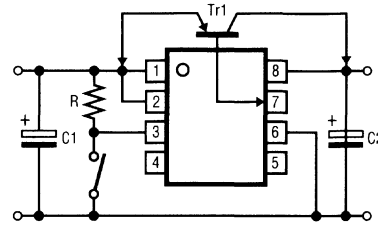
ACTIVE HIGH CONTROL WITH CURRENT BOOST



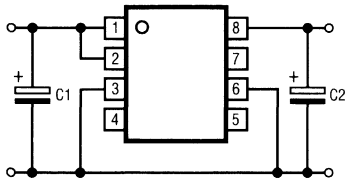
ACTIVE LOW CONTROL



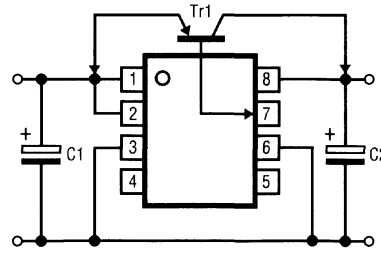
ACTIVE LOW CONTROL WITH CURRENT BOOST



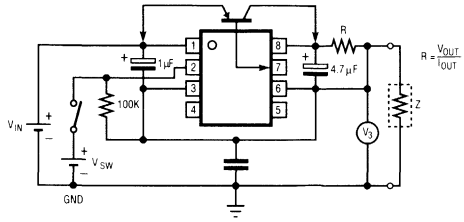
NO SWITCH CONTROL



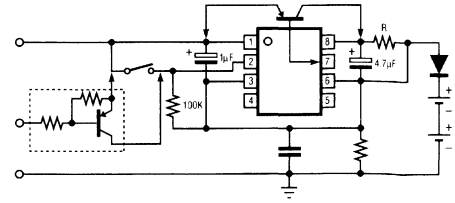
NO SWITCH CONTROL WITH CURRENT BOOST



CURRENT MODE REGULATOR WITH "ON/OFF" CONTROL AND CURRENT BOOST



BATTERY CHARGER WITH "ON/OFF" CONTROL AND CURRENT BOOST



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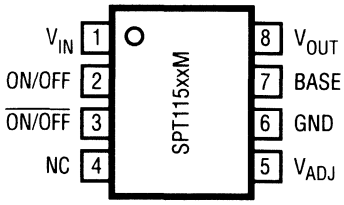
PIN ASSIGNMENTS



LEADERSHIP IN DATA CONVERSION AND SIGNAL PROCESSING

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SPT116

THREE TERMINAL VOLTAGE REGULATOR

FEATURES

- Low Dropout Voltage
- Very Low Standby Current (No Load)
- Good Load Regulation
- Internal Thermal Shutdown
- Short Circuit Protection
- 3% Output Voltage Accuracy
- Available On Paper Tape
- Customized Versions Are Available

APPLICATIONS

- Battery Powered Systems
- Portable Consumer Equipment
- Cordless Telephones
- Personal Communications Equipment
- Portable Instrumentation
- Radio Control Systems
- Low Voltage Systems

GENERAL DESCRIPTION

The SPT116 series devices are low power, linear 3-terminal regulators.

An internal PNP pass-transistor is used in order to achieve low dropout voltage (typically 200 mV at 80 mA load current).

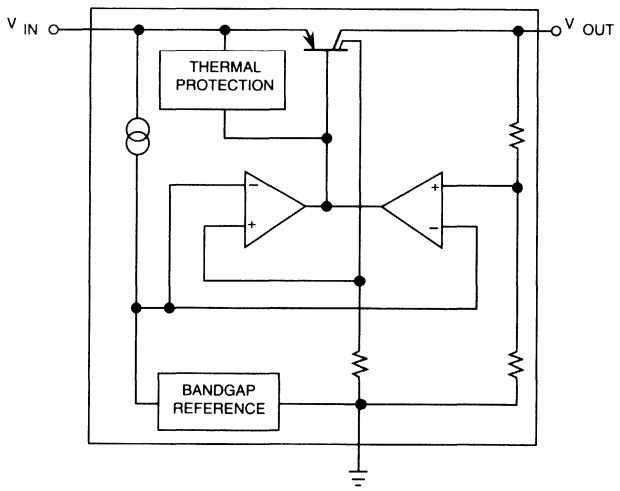
The regulated output voltage may be specified in 0.5 V increments between 2.0 to 5.5 V. The device has very low (400 µA) quiescent current with no load and 2 mA with 60 mA load.

An internal thermal shutdown circuit limits the junction temperature to below 150 °C. The load current is internally monitored and the device will shut down in the presence of a short circuit at the output.

The SPT116 series is available in plastic TO-92N and plastic tape and reel TO-92NT packages.

7

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Beyond which damage may occur)[1] 25 °C

Supply Voltage ..... 18 V
Output Voltage ..... V_{OUT} x1.15 V
Load Current (TO-92) ..... 180 mA
Load Current (U-Pack 3) ..... 250 mA
Power Dissipation (TO-92) Note 2 ..... 500 mW
Power Dissipation (U-Pack 3) ..... 600 mW
Storage Temperature Range ..... -55 to +150 °C
Operating Temperature Range ..... -40 to +85 °C
Lead Soldering Temp (10 sec) ..... +240 °C
Junction Temperature ..... +150 °C

ELECTRICAL SPECIFICATIONS (Unless otherwise specified, $T_A=T_{MIN}$ to T_{MAX}) Note 3

PARAMETERS	TEST CONDITIONS	SYMBOL	MIN	TYP	MAX	UNITS
Supply Voltage Range		V_{IN}	2.5		16	V
Supply Current 1	$V_{IN}=V_{OUT}$ + 1 V, I_{OUT} = 0 mA	I_{IN1}		400	800	µA
Supply Current 2	$V_{IN}=V_{OUT}$ + 1 V, I_{OUT} = 10 mA	I_{IN2}		0.8	2.0	mA
Regulated Output Voltage	$V_{IN}=V_{OUT}$ + 1 V, I_{OUT}=10 mA	V_O				
	T_A = 25 °C				±3.0	%
					±100	mV
	TO-92: T_A = -20 to +70 °C				±4.0	%
					±130	mV
	T_A = -40 to +85 °C				±5.0	%
					±150	mV
	U-Pack 3: T_A =-20 to +70 °C				±4.5	%
					±130	mV
	T_A =-40 to +85 °C				±5.0	%
					±140	mV
Dropout Voltage 1	I_{OUT}=0 mA, TO-92	V_{DROP1}		25	80	mV
	I_{OUT}=30 mA, U-Pack 3			80	150	mV
Dropout Voltage 2	I_{OUT}=60 mA, TO-92	V_{DROP2}		150	300	mV
	I_{OUT}=60 mA, U-Pack 3			130	280	mV
Dropout Voltage 3	I_{OUT}=100 mA, U-Pack 3	V_{DROP3}		170	330	mV
Output Current	$V_{IN}=V_{OUT}$ + 1 V, TO-92	I_{OUT}		130		mA
	$V_{IN}=V_{OUT}$ + 1 V, U-Pack 3			190		mA
Recommended	$V_{IN}=V_{OUT}$ + 1 V, TO-92	I_{OR}			100	mA
Output Current	$V_{IN}=V_{OUT}$ + 1 V, U-Pack 3				150	mA
Line Regulation	(V_{OUT} + 1.0 V) ≤V_{IN}≤(V_{OUT}+6.0 V)	LI_{REG}		2.0	30	mV
Load Regulation 1	I_{OUT}=1 to 30 mA, TO-92	LD_{REG1}		15	70	mV
	I_{OUT}=1 to 30 mA, U-Pack 3			15	60	mV
Load Regulation 2	I_{OUT}=1 to 60 mA, TO-92	LD_{REG2}		30	120	mV
	I_{OUT}=1 to 100 mA, U-Pack 3			40	140	mV
Ripple Rejection	$V_{IN}=V_{OUT}$ + 1.5 V, 100 mV/RMS					
	f=400 Hz	RR		55		dB
Temperature Coefficient	$V_{IN}=V_{OUT}$ + 1.5 V, I_{OUT}=10 mA					
	TO-92			±0.3		mV/°C
	U-Pack 3			±0.35		mV/°C
Output Noise Voltage	$V_{IN}=V_{OUT}$ + 1.5 V, I_{OUT}=10 mA, TO-92	V_N		150		μV_{RMS}
Quiescent Current	V_{IN}=6.0 V, I_{OUT}=60 mA, U-Pack 3	V_N		2	4.5	mA

Note 1: Operation at any Absolute Maximum Rating is not implied. See Operating Conditions for proper nominal applied conditions in typical applications.
Note 2: Derate above T_A=25 °C at 1.6 mW/°C.
Note 3: Due to the common format used here, some specifications may not apply to all versions of output voltage. Detailed specifications are available for each version.

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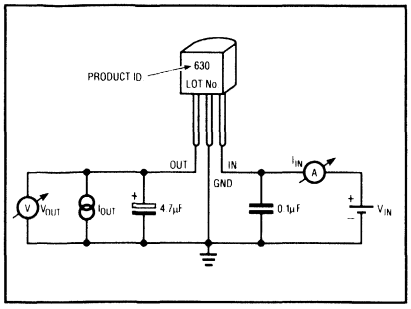
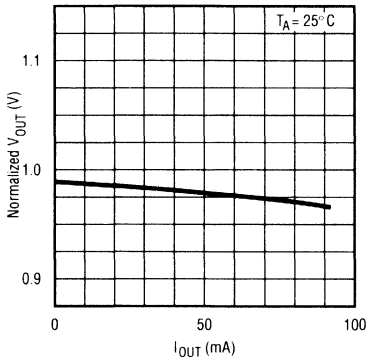
TYPICAL PERFORMANCE CHARACTERISTICS (TO-92 PACKAGE ONLY)

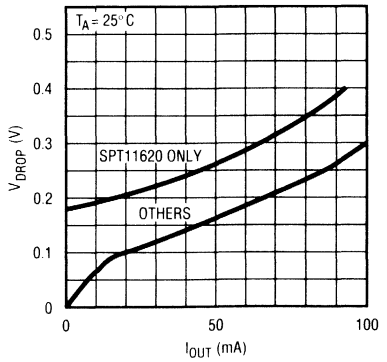
TEST CIRCUIT 1



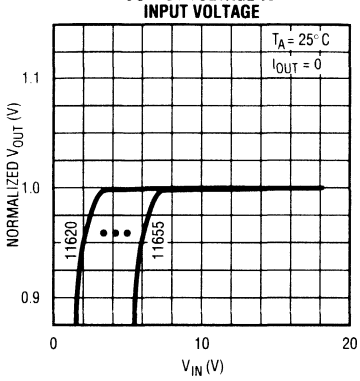
OUTPUT VOLTAGE vs OUTPUT CURRENT



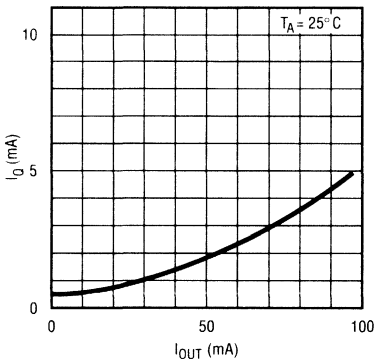
DROPOUT VOLTAGE vs LOAD CURRENT



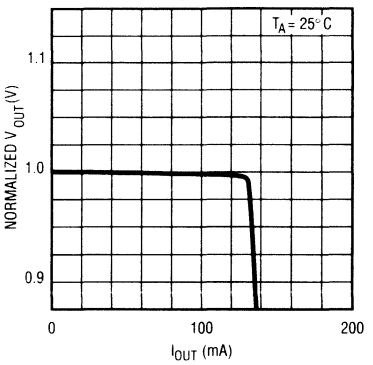
OUTPUT VOLTAGE vs INPUT VOLTAGE



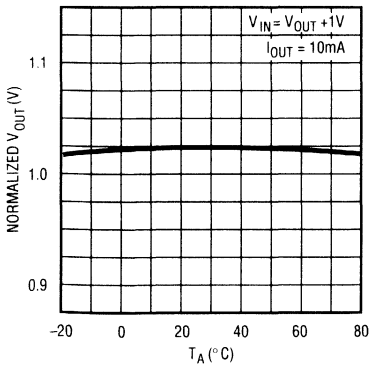
QUIESCENT CURRENT vs LOAD CURRENT



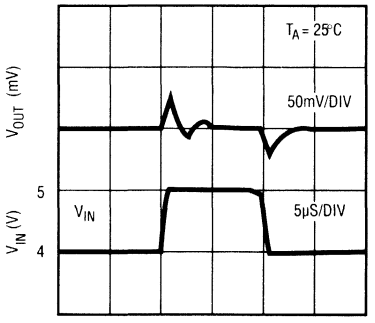
SHORT CIRCUIT PROTECTION



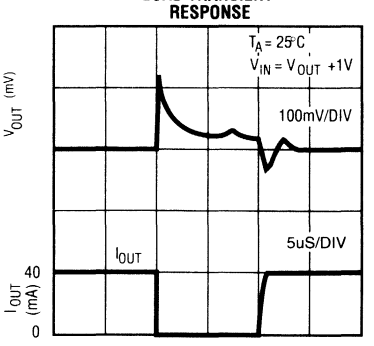
OUTPUT VOLTAGE vs TEMPERATURE



LINE TRANSIENT RESPONSE

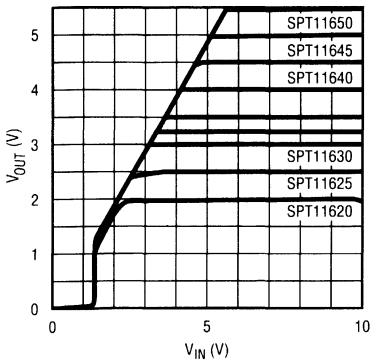


LOAD TRANSIENT RESPONSE

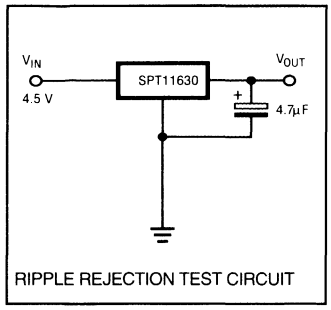


TYPICAL PERFORMANCE CHARACTERISTICS (TO-92 PACKAGE ONLY)

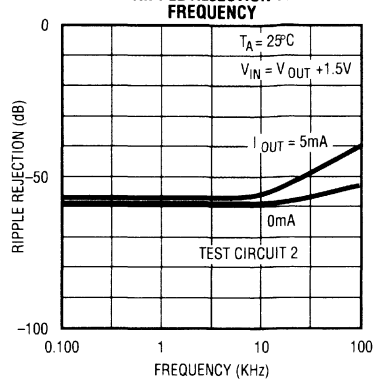
INPUT OUTPUT CHARACTERISTICS



TEST CIRCUIT 2

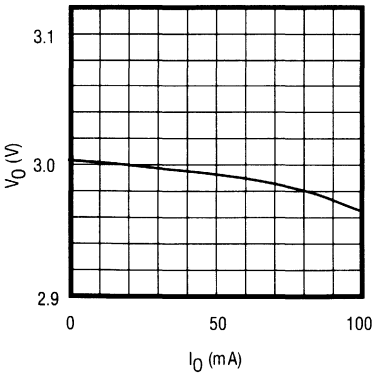


RIPPLE REJECTION vs FREQUENCY

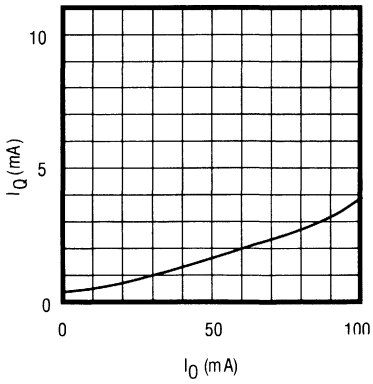


TYPICAL PERFORMANCE CHARACTERISTICS (U-PACK 3 PACKAGE ONLY)

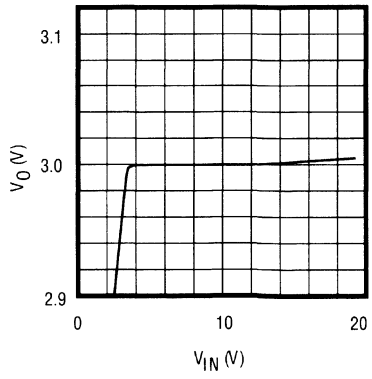
OUTPUT VOLTAGE vs. OUTPUT CURRENT



QUIESCENT CURRENT vs. LOAD CURRENT



OUTPUT VOLTAGE vs. INPUT VOLTAGE (1)



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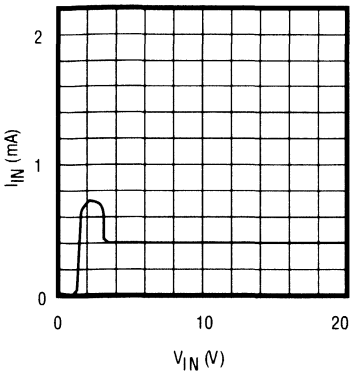
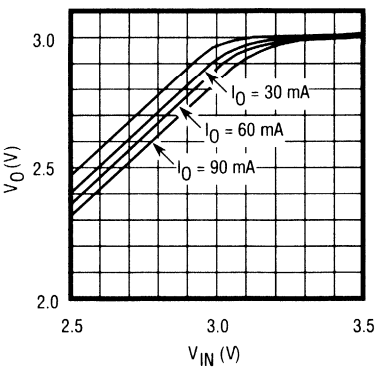
TYPICAL PERFORMANCE CHARACTERISTICS (U-PACK 3 PACKAGE ONLY)

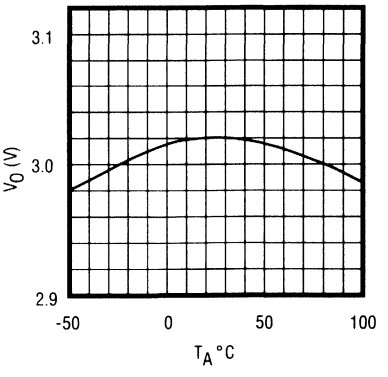
INPUT CURRENT vs. INPUT VOLTAGE



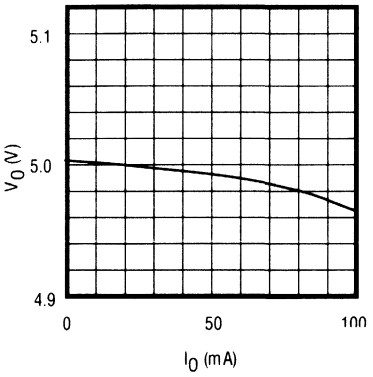
OUTPUT VOLTAGE vs. INPUT VOLTAGE (2)



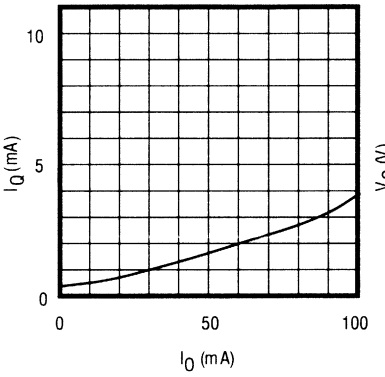
OUTPUT VOLTAGE vs. TEMPERATURE



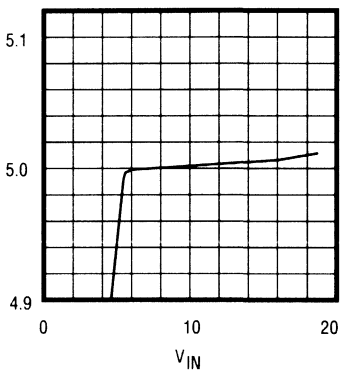
OUTPUT VOLTAGE vs. OUTPUT CURRENT



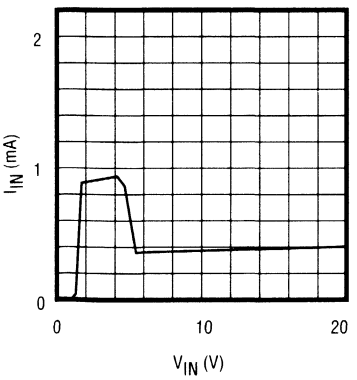
QUIESCENT CURRENT vs. LOAD CURRENT



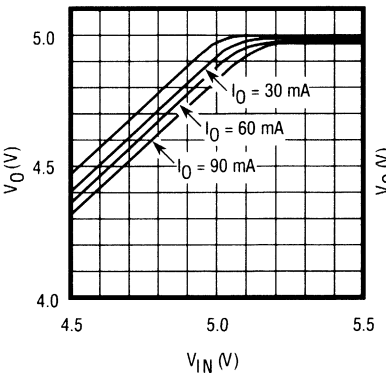
OUTPUT VOLTAGE vs. INPUT VOLTAGE (1)



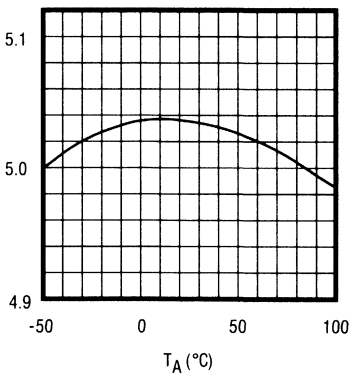
INPUT CURRENT vs. INPUT VOLTAGE



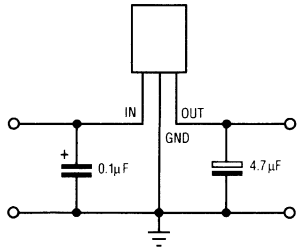
OUTPUT VOLTAGE vs. INPUT VOLTAGE (2)



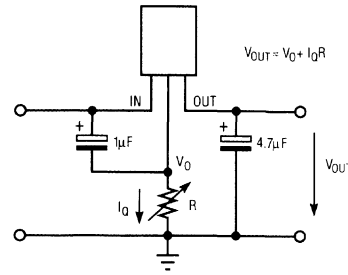
OUTPUT VOLTAGE vs. TEMPERATURE



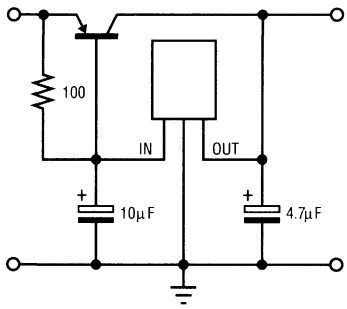
VOLTAGE REGULATOR CIRCUIT



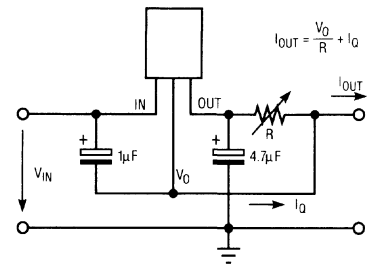
VOLTAGE BOOST CIRCUIT



CURRENT BOOST CIRCUIT



CURRENT REGULATOR CIRCUIT



APPLICATION HINTS

Maximize copper foil area connecting to all IC pins for optimum heat conduction. Place input and output bypass capacitors close to the GND pin.

For best transient behavior and lowest output impedance, use as large of a capacitor value as possible. The temperature coefficient of the capacitance and Equivalent Series Resistance (ESR) should be taken into account. These parameters can influence power supply noise and ripple rejection. In extreme cases, oscillation may occur. In order to maintain stability, the output bypass capacitor value should be minimum 1 µF in case of Tantalum electrolytic or 4.7 µF in case of Aluminium electrolytic at T_A=25 °C.

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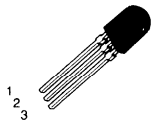
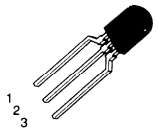
PIN ASSIGNMENTS

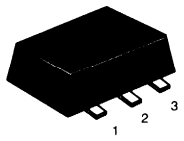
SPT116xxN



SPT116xxNT



SPT116xxU



PIN 1. OUTPUT
2. GROUND
3. INPUT

LEADERSHIP IN DATA CONVERSION AND SIGNAL PROCESSING

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SPT119

VOLTAGE REGULATOR WITH RESET OUTPUT

FEATURES

- Very Low Dropout Voltage
- Reset Output for Microprocessor
- Very Low Quiescent Current (No Load)
- Internal Thermal / Overload Shutdown
- Low Noise Voltage
- Input and Output Voltage Sense
- ±2.5% Output Voltage Accuracy
- CMOS or TTL ON/OFF Control
- Very High Speed Transient Response (TYP 50 µS) (Off/On)

APPLICATIONS

- Battery Powered Systems
- Cellular Telephones
- Pagers
- Personal Communications Equipment
- Portable Instrumentation
- Portable Consumer Equipment
- Radio Control Systems
- Remote Control Transmitters
- Low Voltage Systems

GENERAL DESCRIPTION

The SPT119 is a low power, linear regulator with on/off switch. Built-in input and output voltage comparators provide a reset logic LOW level whenever the input or output voltage falls outside internally preset limits. The internal electronic switch can be controlled by CMOS or TLL levels. The device is in the OFF state when the control pin is biased HIGH.

An internal PNP pass-transistor is used in order to achieve low dropout voltage (typically 200 mV at 50 mA load current). The device has very low quiescent current (130 µA) in the ON mode with no load and 2 mA with 30 mA load. The quiescent current is typically 4 mA at 60 mA load. The current consumption in the OFF mode is 65 µA. An internal thermal shutdown circuit limits the junction temperature to below 150 °C. The load current is internally monitored and the device will shut down (no load current) in the presence of a short circuit at the output. The regulated output voltage is accurate to within ±2.5 %. The output noise is very low at 100 dB down from V_{OUT} when an external noise bypass capacitor is used.

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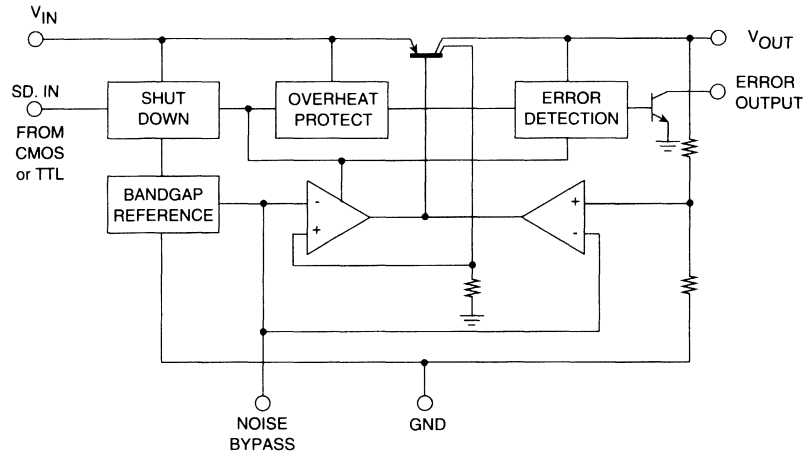
BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (BEYOND WHICH DAMAGE MAY OCCUR) 25[1] °C

Supply Voltage ..... 14 V
Output Voltage ..... V_{OUT} x1.15 V
Load Current ..... 180 mA
Power Dissipation (Note 2) ..... 200 mW

StorageTemperature Range ..... -55 to +150 °C
Operating Temperature Range ..... -40 to +85 °C
Lead Soldering Temp (10 sec) ..... +240 °C
Junction Temperature ..... +150 °C

ELECTRICAL SPECIFICATIONS

$T_A=T_{MIN}$ - T_{MAX} unless otherwise specified.

PARAMETERS	TEST CONDITIONS	SYMBOL	MIN	TYP	MAX	UNITS
Supply Voltage Range		V_{IN}	1.8		16	V
Supply Current 1	I_O=0 mA	I_{IN1}		140	300	µA
Supply Current 2	$V_{IN}=V_O$ -1 V, I_O = 0 mA	I_{IN2}		400	900	µA
Quiescent Current	I_{IO}=60 mA	I_Q		5	10	mA
Regulated Output Voltage	I_{OUT}=1 mA	V_O				
	T_A=25 °C		-2.5		+2.5	%
			-80		+80	mV
	T_A=-20 °C to +70 °C		-3.5		+3.5	%
			-110		+110	mV
	T_A=-40 °C to +85 °C		-4.0		+4.0	%
			-120		+120	mV
Dropout Voltage	I_O=30 mA	V_{DROP}		160	350	mV
Output Current	$V_{IN}=V_O$ + 1 V				100	mA
Line Regulation	$V_{IN}=(V_O+1\ V) \sim (V_O+10\ V)$, V_{IN}MAX	Line Reg		±5	±50	mV
Load Regulation	I_O=1-80 mA	Load Reg		25	150	mV
Ripple Rejection	$V_{IN}=V_O$ + 1.5 V	RR		68		dB
V_O Temperature Coefficient	I_{OUT}=10 mA, $V_{IN}=V_O$ + 1.0 V	$\Delta V/\Delta T$		±0.2		µV/°C
Output Noise Voltage	10 Hz ≤f≤100 kHz					
	C_L = 10 µF, C_P=0.01 µF	V_N		50		μV_{RMS}

Note 1: Operation at any Absolute Maximum Rating is not implied. See Operating Conditions for proper nominal applied conditions in typical applications.
Note 2: Derates above T_A=25 °C at 1.6 mW/°C.

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ELECTRICAL SPECIFICATIONS

$T_A=T_{MIN}$ - T_{MAX} unless otherwise specified.

TEST PARAMETERS	CONDITIONS	SYMBOL	MIN	TYP	MAX	UNITS
Low Voltage Detector		V_{DET}		V_{OUT} x 0.95		V
V_{DET} Error Range			-4	V_{DET}	+4	%
Saturation Voltage	I_{FLAG}=100 µA	V_{SAT}		0.2	0.4	V
OFF Time Current		I_{OFF}		65	150	µA
Control Pin Current 1	V_{CONT}=5 V	$I_{CONT}1$		25	100	µA
Control Pin Current 2		$I_{CONT}2$		45	150	µA
Control Voltage 1	V_{OUT}ON	$V_{CONT}1$			0.8	V
Control Voltage 2	V_{OUT}OFF	$V_{CONT}2$	2.4			V
Transient	OFF/ON, C_L=0.1µF C_P=0.1 µF, I_O=30 mA			50		µsec

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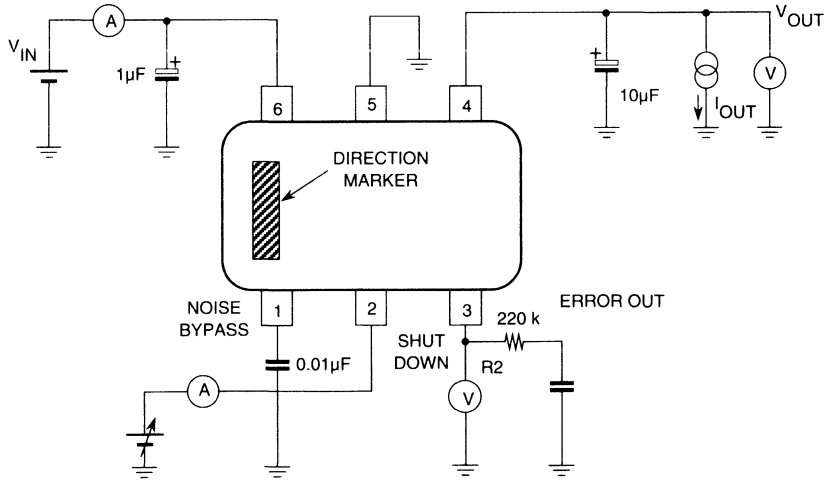
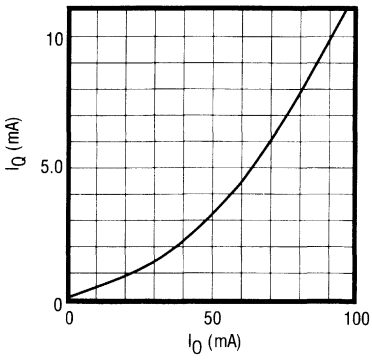
Figure 1 - Test Circuit



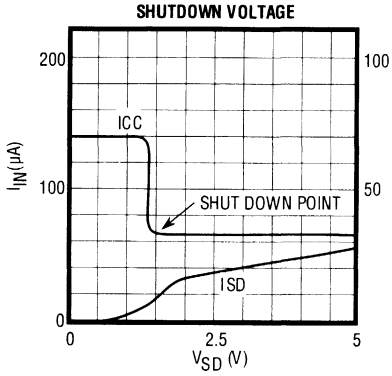
TYPICAL PERFORMANCE CHARACTERISTICS

SPT119XX (Refers to Both 11948 and 11950)

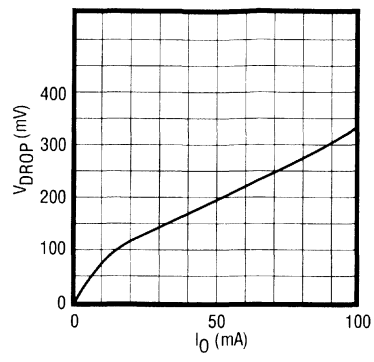
QUIESCENT CURRENT vs OUTPUT CURRENT



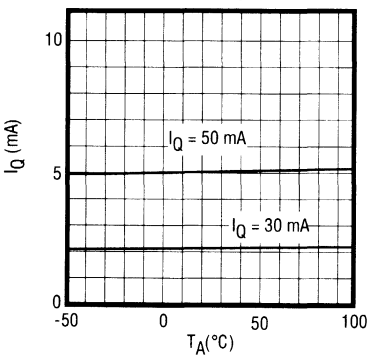
INPUT CURRENT vs SHUTDOWN VOLTAGE



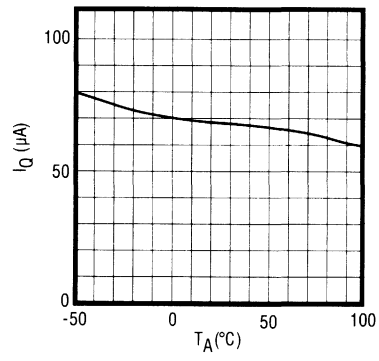
DROPOUT VOLTAGE vs OUTPUT CURRENT



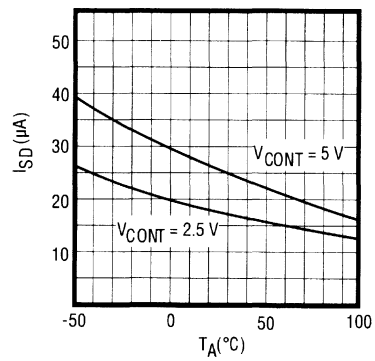
QUIESCENT CURRENT vs TEMPERATURE



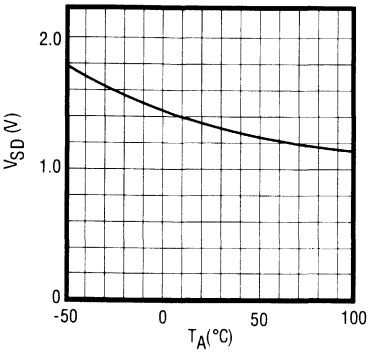
QUIESCENT CURRENT (OFF MODE) vs TEMPERATURE



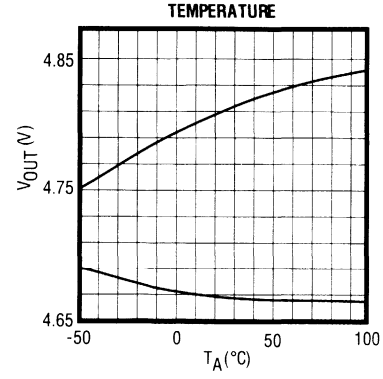
SHUTDOWN PIN INPUT CURRENT vs TEMPERATURE



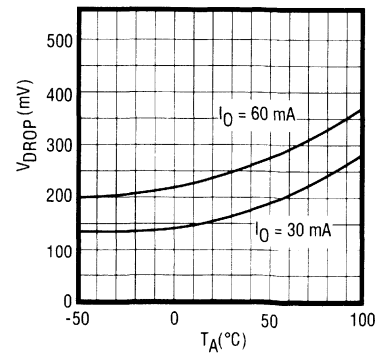
SHUTDOWN VOLTAGE (OUTPUT OFF) vs TEMPERATURE



LOW VOLTAGE DETECT (HYSTERESIS) vs TEMPERATURE



DROPOUT VOLTAGE vs TEMPERATURE



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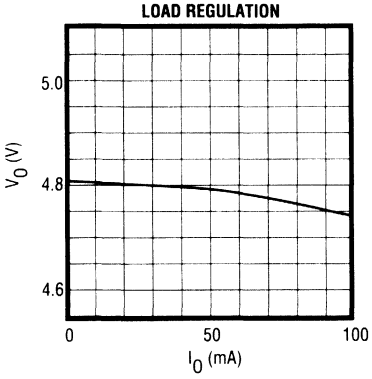
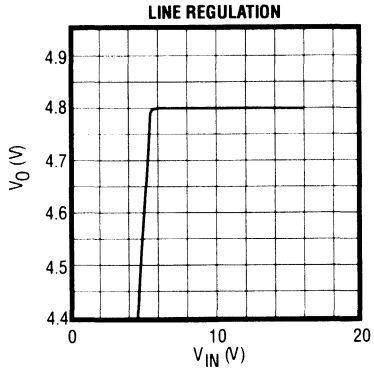
TYPICAL PERFORMANCE CHARACTERISTICS

SPT11948

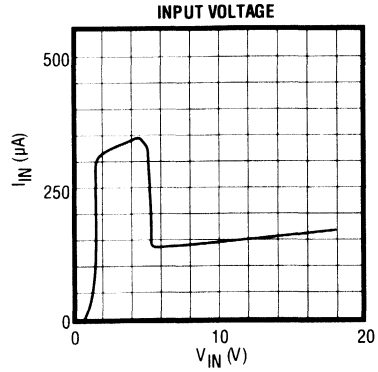
LOAD REGULATION



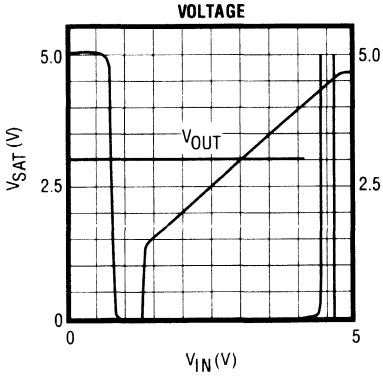
LINE REGULATION



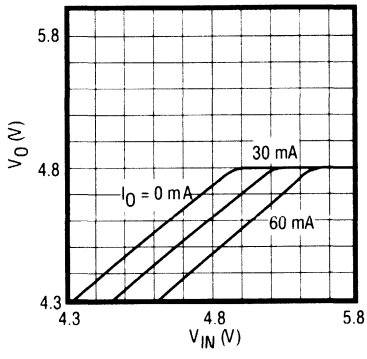
INPUT CURRENT (NO LOAD) vs INPUT VOLTAGE



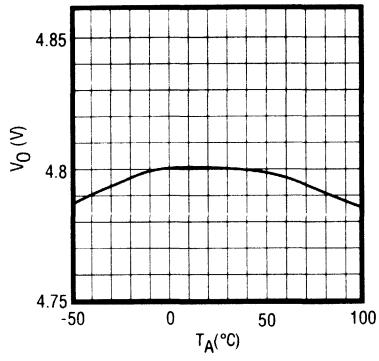
LOW VOLTAGE DETECTOR vs INPUT VOLTAGE



OUTPUT VOLTAGE vs. INPUT VOLTAGE

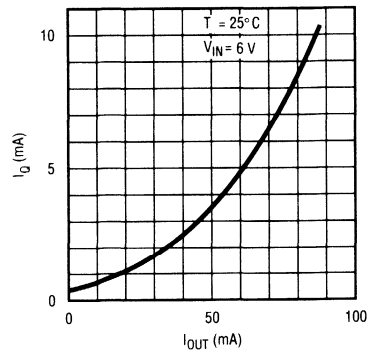


OUTPUT VOLTAGE vs TEMPERATURE

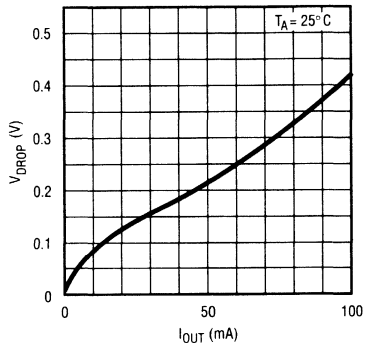


SPT11950

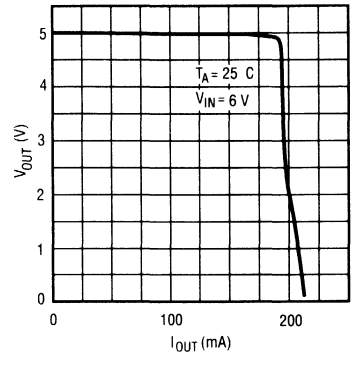
QUIESCENT CURRENT vs LOAD CURRENT



DROPOUT VOLTAGE vs LOAD CURRENT



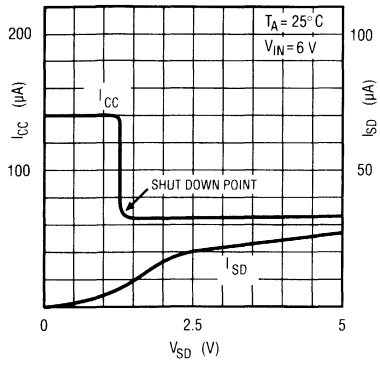
SHORT CIRCUIT CURRENT vs OUTPUT VOLTAGE



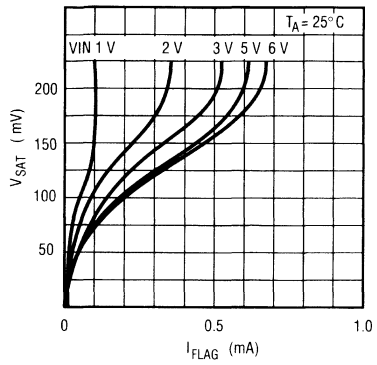
TYPICAL PERFORMANCE CHARACTERISTICS

SPT11950

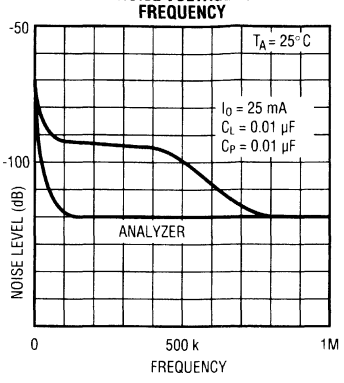
SUPPLY CURRENT AND SHUT DOWN VOLTAGE SHUT DOWN CURRENT vs SHUT DOWN VOLTAGE



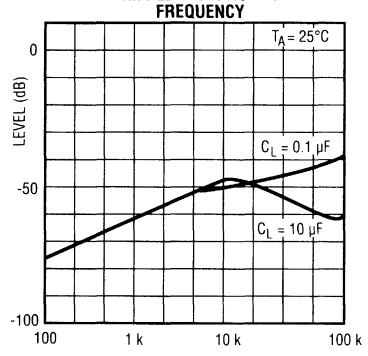
SATURATION VOLTAGE vs ERROR OUTPUT CURRENT

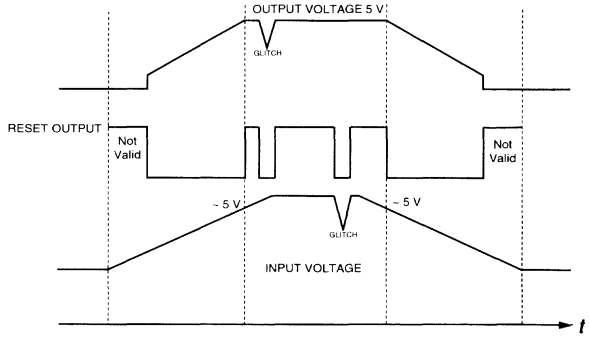


NOISE VOLTAGE vs FREQUENCY



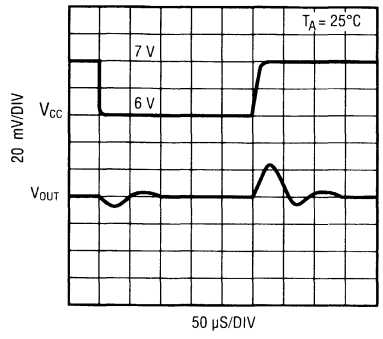
RIPPLE REJECTION vs FREQUENCY



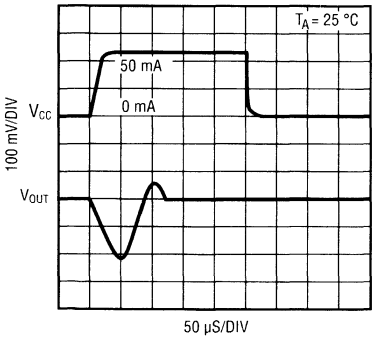


TIMING DIAGRAM PRINCIPLE OF OPERATION

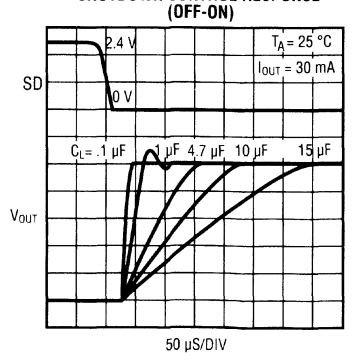
LINE TRANSIENT RESPONSE



LOAD TRANSIENT RESPONSE



SHUTDOWN CONTROL RESPONSE (OFF-ON)



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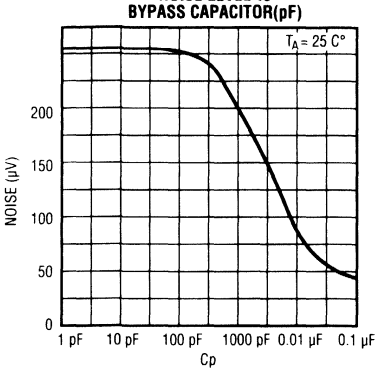
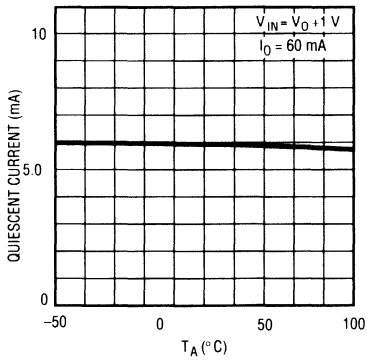
TYPICAL PERFORMANCE CHARACTERISTICS

SPT11950

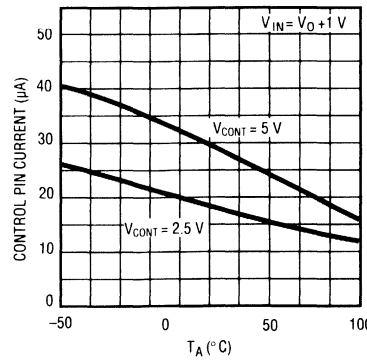
NOISE LEVEL vs BYPASS CAPACITOR(pF)



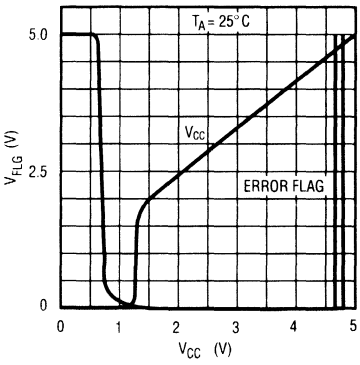
QUIESCENT CURRENT vs TEMPERATURE



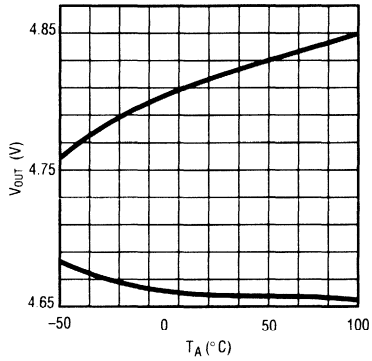
CONTROL PIN CURRENT vs TEMPERATURE



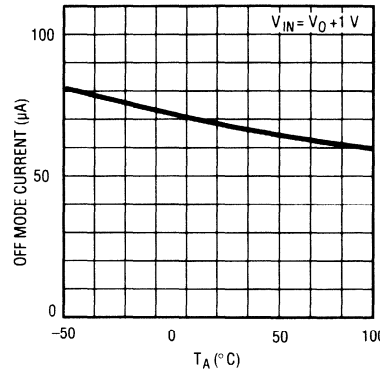
ERROR DETECT vs INPUT VOLTAGE



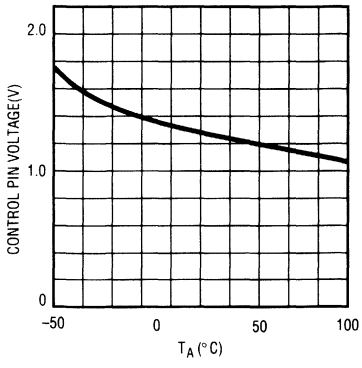
LOW VOLTAGE DETECT (HYSTERESIS) vs TEMPERATURE



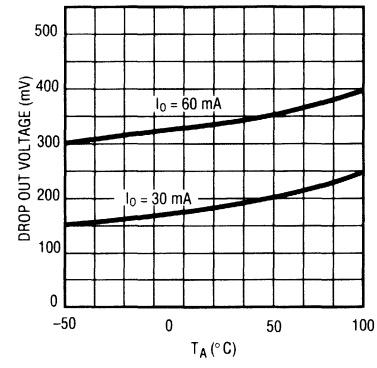
OFF MODE CURRENT vs TEMPERATURE



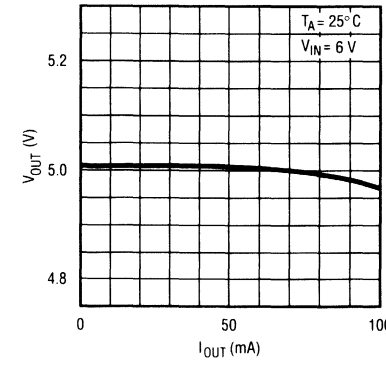
CONTROL PIN VOLTAGE vs TEMPERATURE



DROPOUT VOLTAGE vs TEMPERATURE



OUTPUT VOLTAGE vs OUTPUT CURRENT



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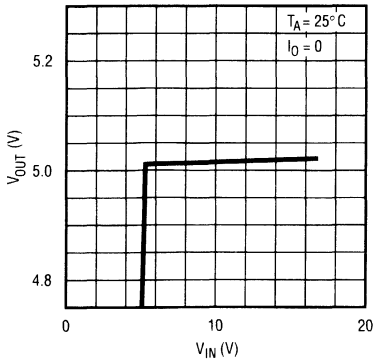
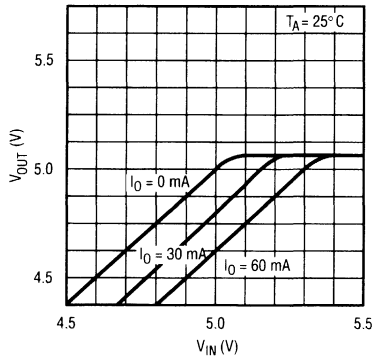
TYPICAL PERFORMANCE CHARACTERISTICS

SPT11950

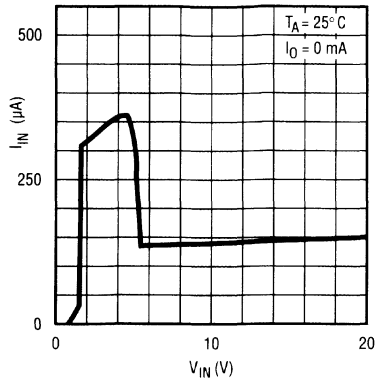
OUTPUT VOLTAGE vs INPUT VOLTAGE



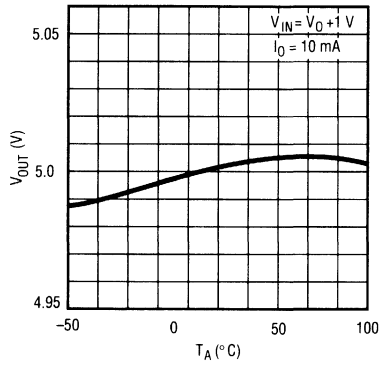
OUTPUT VOLTAGE vs INPUT VOLTAGE



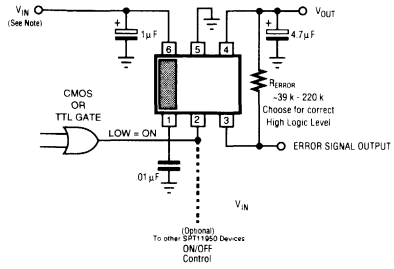
INPUT CURRENT vs INPUT VOLTAGE



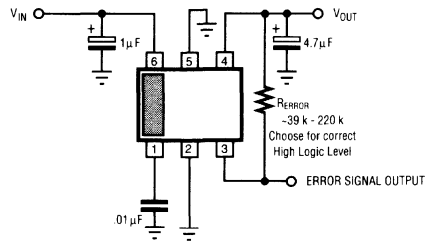
OUTPUT VOLTAGE vs TEMPERATURE



CONTROL FUNCTION UTILIZED



CONTROL FUNCTION NOT UTILIZED



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Application Hints

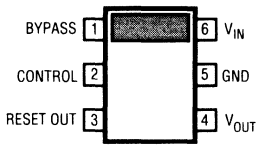
The power dissapation of the SPT119 can be increased to 400 mW when mounted to the PC board as shown at left.. Maximize copper foil area connecting to all IC pins for optimum performance. Place input and output bypass capacitors close to the GND pin. For best transient behavior and lowest output impedance, use as large a capacitor value as possible. The temperature coefficient of the capacitance and Equivalent Series Resistance (ESR) should be taken into account. These parameters can influence power supply noise and ripple rejection. In extreme cases, oscillation may occur. In order to maintain stability, the output bypass capacitor value should be minimum 0.1 μF for Tantalum electrolytic or .22 μF for Aluminum electrolytic.

Handling Molded Resin Packages

All plastic molded packages absorb some moisture from the air. If moisture absorption occurs prior to soldering the device into the printed circuit board, increased separation of the lead from the plastic molding may occur, degrading the moisture barrier characteristics of the device. This property of plastic molding compounds should not be overlooked, particularly in the case of very small packages, where the plastic is very thin.

In order to preserve the original moisture barrier properties of the package, devices are stored and shipped in moisture proof bags filled with dry air. The bags should not be opened or damaged prior to the actual use of the devices. If this is unavoidable, the devices should be stored in a low relative humidity environment (40 to 65%) or in an enclosed environment with desiccant.

PIN ASSIGNMENT



LEADERSHIP IN DATA CONVERSION AND SIGNAL PROCESSING

4755 Forge Road, Co. Springs, CO 80907
PH: (719) 528-2300; Fax: (719) 528-2370 SPT

SIGNAL PROCESSING TECHNOLOGIES

SPT120

ADJUSTABLE LOW DROPOUT REGULATOR

FEATURES

- Low Supply Current
- Low Power Shutdown Mode
- Low Noise Output
- Low Drop Out Voltage
- Extremely Small Package
- Extemely High Stability
- High Speed On/Off Transient (Typ. 50 μS)

APPLICATIONS

- Portable Instrumentation
- Cordless Telephones
- Pagers
- Toys
- Cellular Phones
- Test Equipment

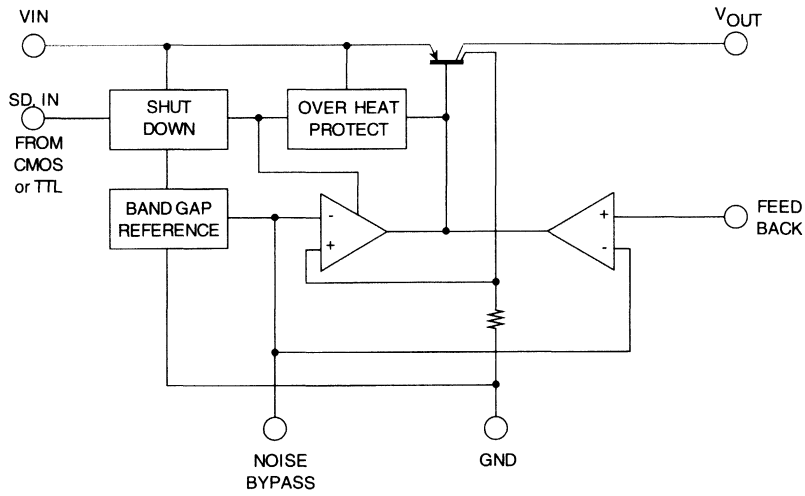
GENERAL DESCRIPTION

The SPT120 is a low dropout voltage regulator with external voltage adjustment. The output can be set between 1.5 V and 6 V by an external pair of resistors in a divider configuration. The device has a bypass pin for an external capacitor to reduce output noise to a typical 50 μV(rms). In addition a shutdown pin is provided that is active high (a high level turns on the output). In the off mode (control pin low) the device draws only 65 μA of quiescent current.

The SPT120 is available in a SOT-23L surface mount package.

7

BLOCK DIAGRAM



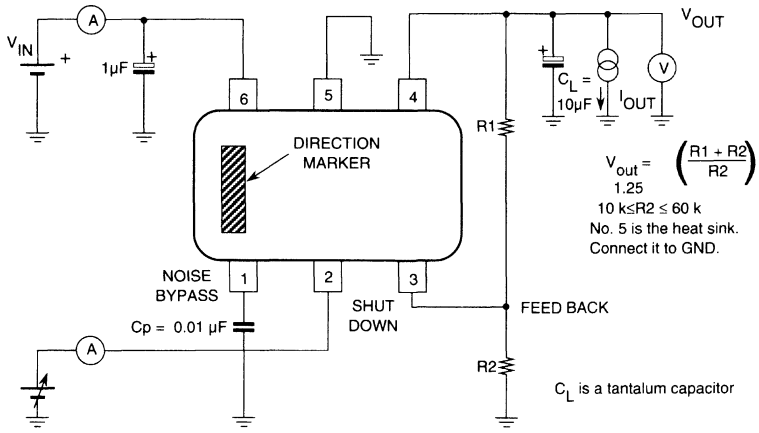
ELECTRICAL SPECIFICATIONS

T_A=+25 °C, V_{IN}=(V_O+1), unless otherwise specified.

PARAMETERS	TEST CONDITIONS	SYMBOL	MIN	TYP	MAX	UNITS
Supply Current 1	I_O=0 mA	I_{CC1}		140	300	µA
Supply Current 2	I_O = 0 mA	I_{CC2}		400	900	µA
Supply Current 3	Shutdown Mode	I_{CC3}		65	150	µA
Output Voltage		V_O	1.5		6.0	V
Dropout Voltage	I_O=30 mA			160	350	mV
Output Current	NOTE 1	I_O			100	mA
Input Stability	V_{IN}=(V_O+1)~(V_O+10) ≤V_{CC} MAX	Line Reg		±5	±50	mV
Load Stability	I_O=1~80 mA	Load Reg		25	150	mV
Ripple Elimination Ratio	C_L=10 µF, 400 Hz	RR		68		dB
Output Noise Voltage	10 Hz<f< 100 kHz, C_L=10 µF	V_{NO}		50		µV(RMS)
Standard Voltage		V_{REF}		1.25		V
Voltage Error		ΔV_{REF}	-2		+2	%
SHUTDOWN MODE						
Shutdown Voltage 1	V_{OUT} - ON	V_{CONT1}			0.8	V
Shutdown Voltage 2	V_{OUT} - OFF	V_{CONT2}	2.4			V
OFF Status Current		I_{OFF}		65	130	µA
Control Current 1	V_{CONT}=5 V	I_{CONT1}		25	100	µA
Control Current 2	V_{CONT}=16 V	I_{CONT2}		45	150	µA
Trise	OFF→ON I_{OUT}=30 mA, C_L=0.1 µF			50		µsec

Note 1: Power dissapation must be derated at the rate of 1.6 mW/°C for operation at T_A = 25°C and above. The power dissapation will increase to 400 mW when the device is mounted on to a PC board that has adequate copper pads to conduct heat away from the device.

Figure 1 - Test Circuit



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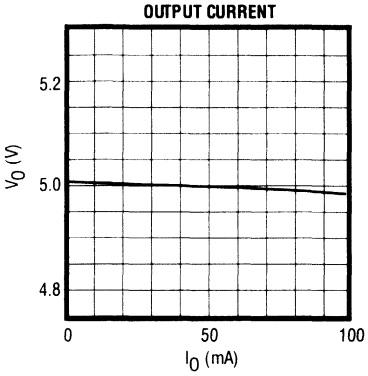
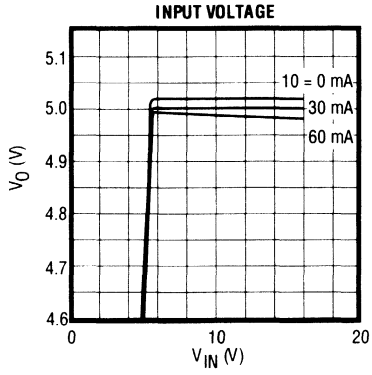
TYPICAL PERFORMANCE CHARACTERISTICS

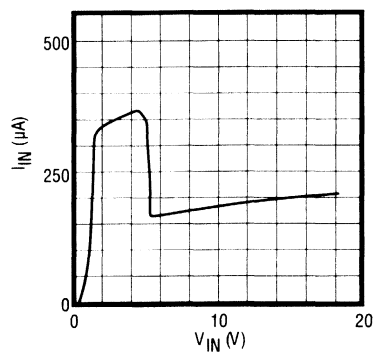
OUTPUT VOLTAGE vs. OUTPUT CURRENT



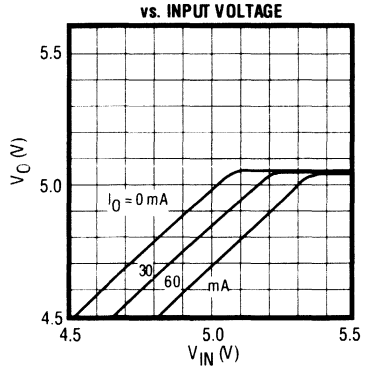
OUTPUT VOLTAGE vs. INPUT VOLTAGE



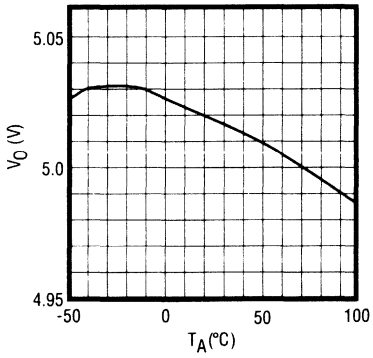
INPUT CURRENT (NO LOAD) vs. INPUT VOLTAGE



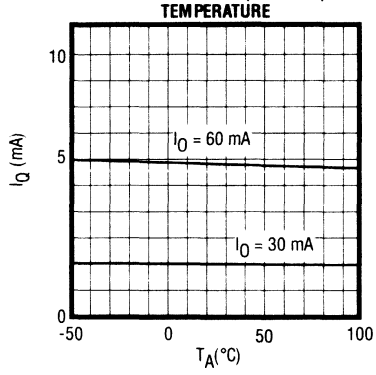
OUTPUT VOLTAGE CHARACTERISTICS vs. INPUT VOLTAGE



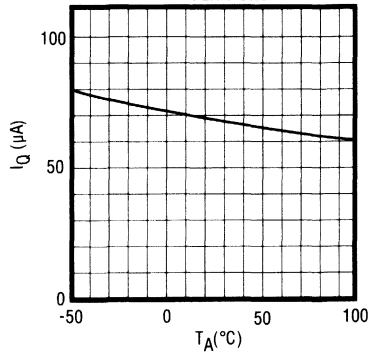
OUTPUT VOLTAGE vs. TEMPERATURES



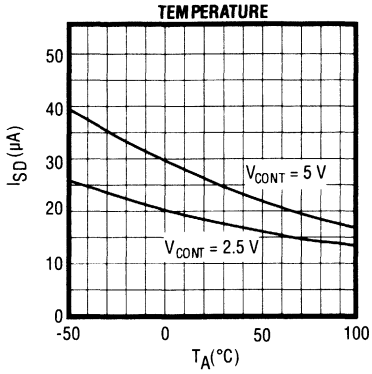
QUIESCENT CURRENT (ON MODE) vs. TEMPERATURE



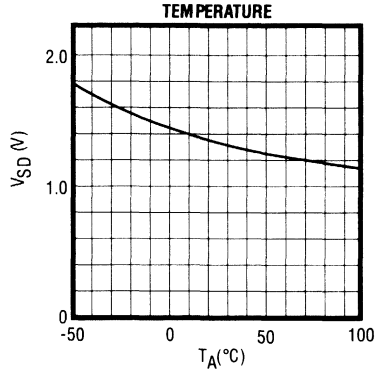
QUIESCENT CURRENT (OFF MODE) vs. TEMPERATURE



CONTROL PIN CURRENT vs. TEMPERATURE

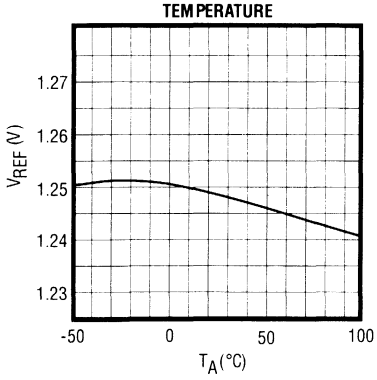


CONTROL PIN VOLTAGE vs. TEMPERATURE

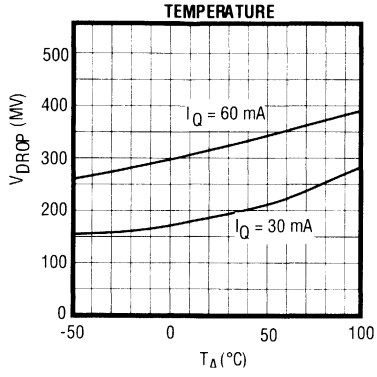


TYPICAL PERFORMANCE CHARACTERISTICS

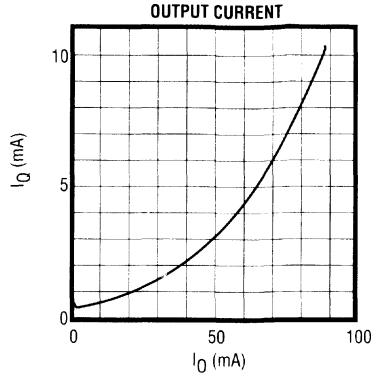
REFERENCE VOLTAGE vs. TEMPERATURE



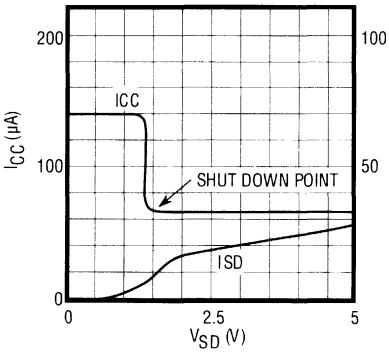
DROP OUT VOLTAGE vs. TEMPERATURE



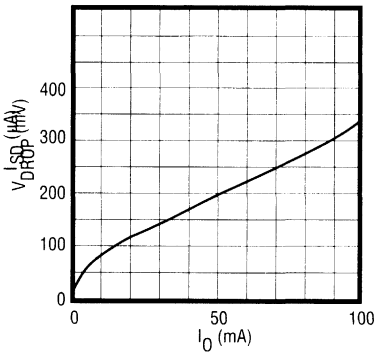
QUIESCENT CURRENT vs. OUTPUT CURRENT



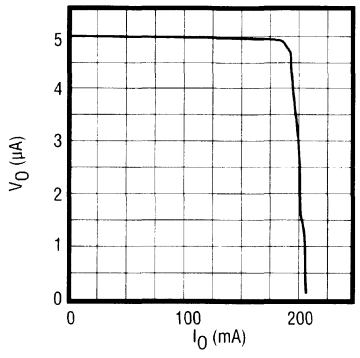
SHUTDOWN CURRENT vs. SHUTDOWN VOLTAGE



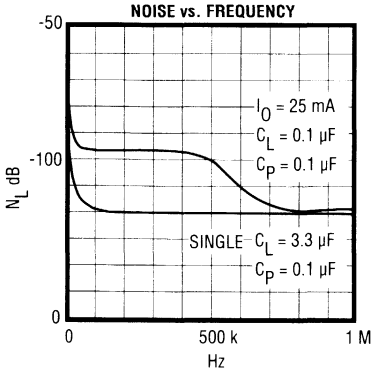
DROPOUT VOLTAGE vs. OUTPUT CURRENT



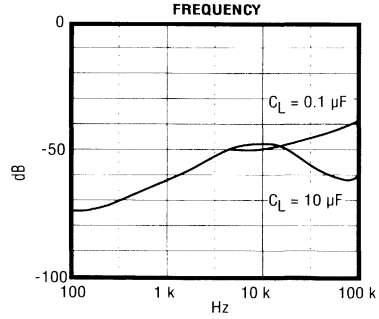
OUTPUT VOLTAGE vs. OUTPUT CURRENT

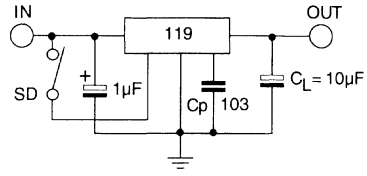


NOISE vs. FREQUENCY



RIPPLE REJECTION vs FREQUENCY





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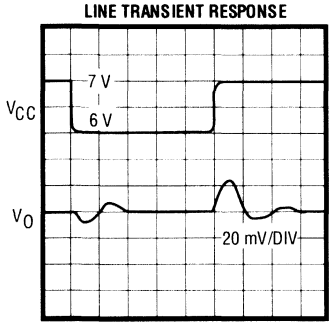
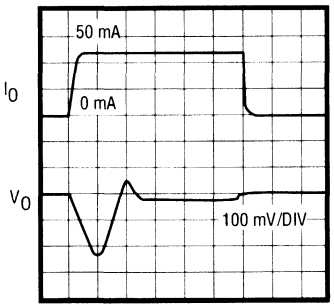
TYPICAL PERFORMANCE CHARACTERISTICS

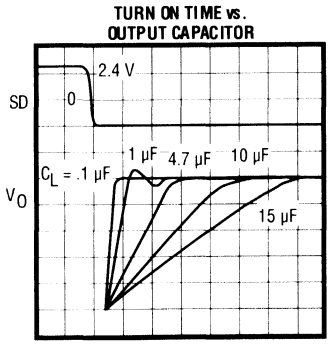
LINE TRANSIENT RESPONSE



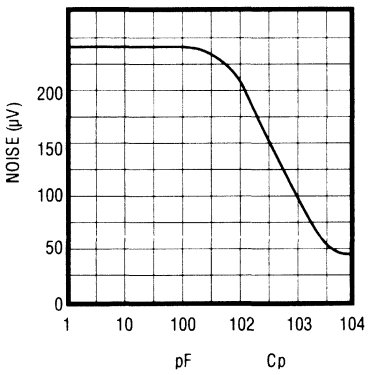
LOAD TRANSIENT RESPONSE

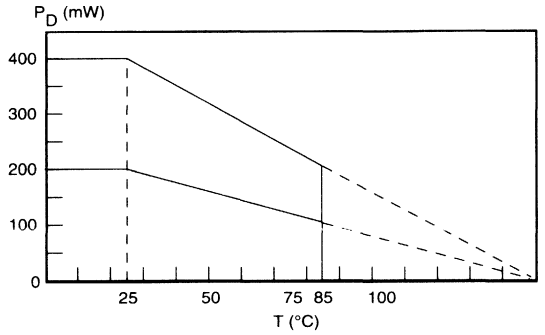


TURN ON TIME vs. OUTPUT CAPACITOR

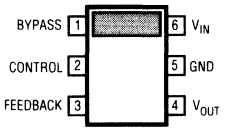


NOISE vs. BYPASS CAPACITOR VALUE





PIN ASSIGNMENT



LEADERSHIP IN DATA CONVERSION AND SIGNAL PROCESSING

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GENERAL PRODUCT INFORMATION 1
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DIGITAL-TO-ANALOG CONVERTERS 4
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Section 8 RF Amplifiers

SPT201	High Frequency (1 GHz)	8-5
SPT202	High Frequency (270 MHz)	8-11
SPT203	High Frequency (500 MHz)	8-17

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SPT
SIGNAL PROCESSING TECHNOLOGIES

SPT201

RF AMPLIFIER

PRELIMINARY INFORMATION

FEATURES

- 1,000 MHz Bandwidth
- 10 dB Insertion Gain
- Single 6-10 V Supply
- Input and Output Impedances Matched to 50 Ohm Systems
- Surface-Mount Packages
- Available on Tape-and-Reel

APPLICATIONS

- RF Communications
- Telecommunications
- Local Area Networks
- Personal Communications Equipment
- Portable Instrumentation
- Portable Consumer Equipment
- Radio Control Systems

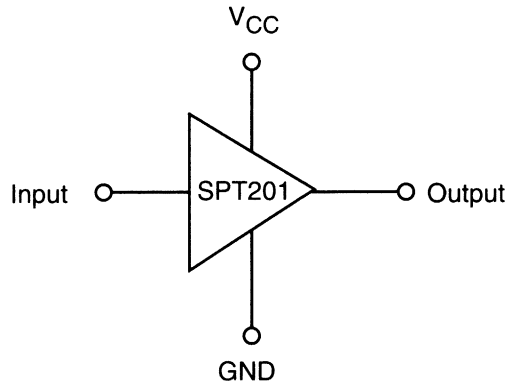
GENERAL DESCRIPTION

The SPT201 is a high-frequency amplifier with an insertion gain of 10 dB. The -3 dB bandwidth is 1000 MHz. Normally, the device operates on a 10 V single supply, and it requires no external components other than input and output decoupling capacitors. When an RF choke is connected between the output and V_{CC}, the device can operate on a single 6 volt supply with no performance degradation. The SPT201 has a 1 dB compression point of +5 dBm at the output and a total power supply consumption of 28 mA. Pin configuration has been optimized for convenient ground plane connections and the use of controlled impedance lines.

The device is available in a plastic U-PACK-5 package.

8

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Beyond which damage may occur)[1]

Supply Voltage	12.0 V	Operating Temperature Range	-40 to +85 °C
Power Dissipation	1 W	Lead Soldering Temperature (10 sec.)	240 °C
Storage Temperature Range	-55 to +150 °C	Junction Temperature	150 °C

[1] Operation at any Absolute Maximum Rating is not implied. See Electrical Specifications for proper nominal applied conditions in typical applications. Application of multiple maximum rating conditions at the same time may damage the device.

ELECTRICAL SPECIFICATIONS

T_A = +25 °C, V_{CC} = +10 V unless otherwise specified.

PARAMETERS	TEST CONDITIONS	SYMBOL	MIN	TYP	MAX	UNITS
Supply Voltage Range		V_{CC}	9.5	10	10.5	V
Supply Current		I_{CC}	23	25	30	mA
Forward Gain		S_{21}	9	10	11	dB
Reverse Gain	F=500 MHz	S_{12}		-17		dB
Input Reflection	F=500 MHz	S_{11}		-13		dB
Output Reflection	F=500 MHz	S_{22}		-15		dB
Bandwidth	(-3 dB)	BW	900	1,000		MHz
Power Out at 1 dB Compression	F=100 MHz	P_{-1dB}		+5		dBm
Third Order Intercept Point	F=100 MHz	IP_3		+15		dBm

Note 1: Derate above T_A=25 °C at 8 mW/°C. Maximize pad under GND and V_{CC} terminals for good head conduction.

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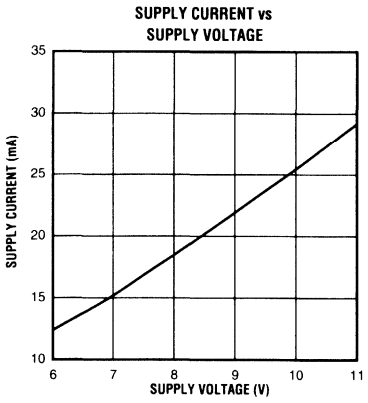
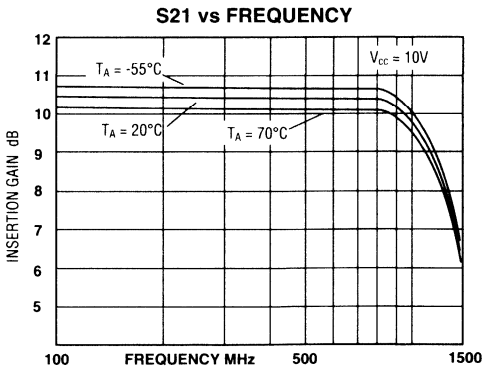
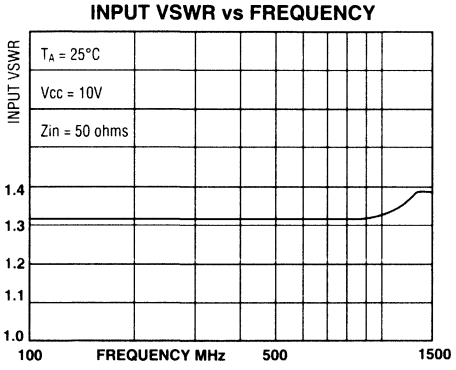
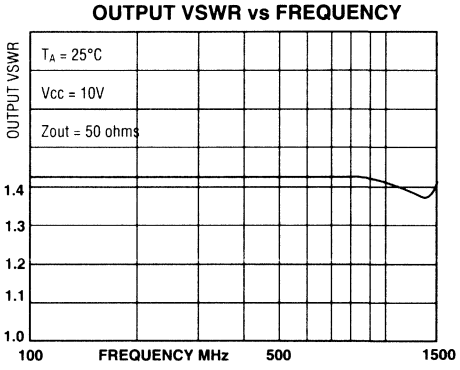
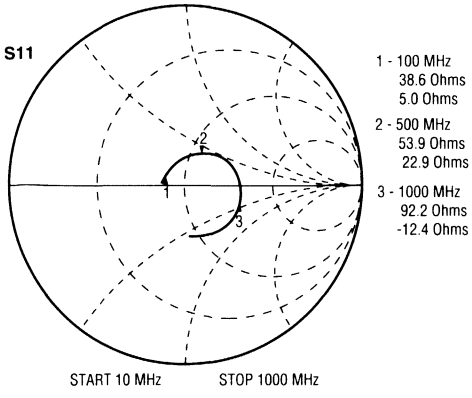
TYPICAL PERFORMANCE CHARACTERISTICS

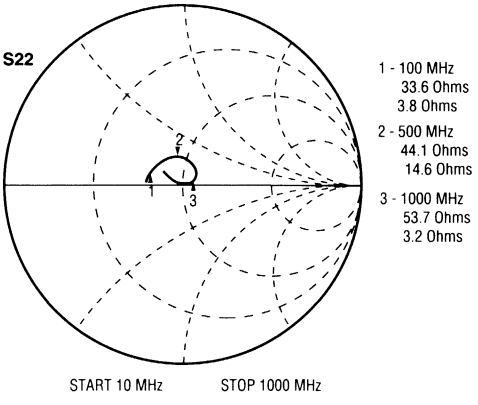






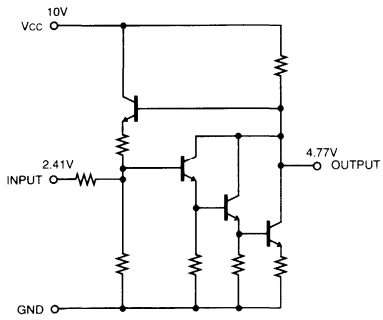






APPLICATIONS INFORMATION

Figure 1 - Equivalent Schematic



As shown in figure 1, internal DC bias voltages appear at the device input and output terminals, therefore DC coupling is only permitted when the external circuitry does not modify the internal bias voltages. Use of capacitive coupling on the input/output terminals is recommended for most applications. For wideband applications a .1 µF monolithic ceramic capacitor works well down to 100 kHz. The input/output coupling capacitor value must be chosen to give an impedance of:

$$\frac{Xc}{2\pi fC} = 1 << 50 \text{ Ohms} \quad \text{at the frequency of interest.}$$

Figure 2 shows connection for lower voltage operation. When an RF choke is connected between Vcc and the Output, the device can operate with no performance degradation down to 6 volts. If the frequency of operation is high, an inductor with high self resonance is required. In the example below the coil is wound on a Fair-Rite #2664666611 core and five turns of #30 wire is used. Although current consumption remains essentially the same, power dissipation is reduced due to the lower operating voltage. A monolithic .1 µF ceramic bypass capacitor is required on the Vcc pin as close as possible to pin 1.

Figure 2 - Connection for Operation at 6 Volts

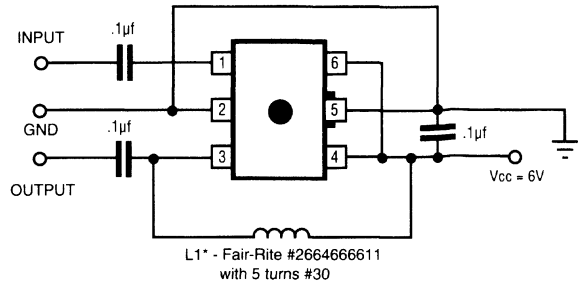
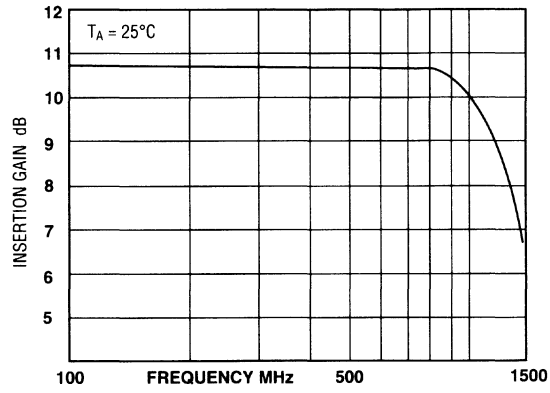


Figure 3 shows the response curve with the SPT201 operating at 6 volts and connected as in Figure 2.

Figure 3 - S21 vs Frequency at 6 Volt Operation



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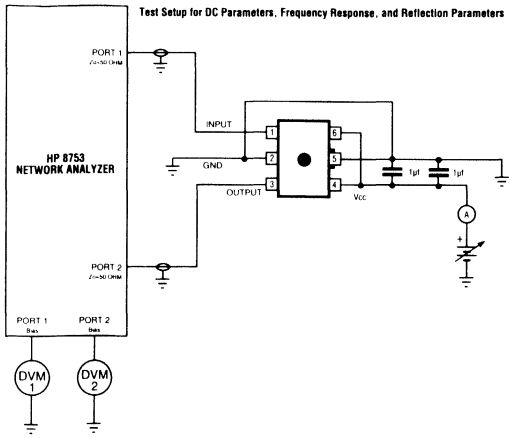
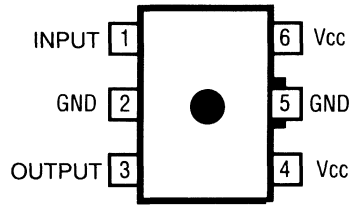
TEST CIRCUIT



PIN ASSIGNMENTS



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LEADERSHIP IN DATA CONVERSION AND SIGNAL PROCESSING

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SIGNAL PROCESSING TECHNOLOGIES

SPT202

RF AMPLIFIER

PRELIMINARY INFORMATION

FEATURES

- 270 MHz Bandwidth
- 15 dB Insertion Gain
- +11 dBm 1dB Compression
- Input and Output Impedances Matched to 50 Ohm System
- 40 dB Isolation
- Surface-Mount Packages
- Available on Tape-and-Reel

APPLICATIONS

- RF Communications
- Telecommunications
- Local Area Networks
- Personal Communications Equipment
- Instrumentation
- Consumer Equipment
- Radio Control Systems

GENERAL DESCRIPTION

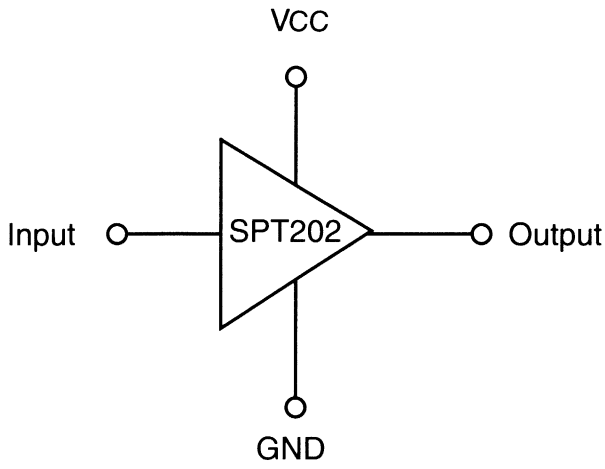
The SPT202 is a high-frequency class A/B amplifier with an insertion gain of 15 dB. The -3 dB bandwidth is 270 MHz. Typically, the device operates on a 6 to 9 V single supply, and it requires no external components other than input and output decoupling capacitors.

The SPT202 has a 1 dB compression point of +11 dBm at the output and a total power supply consumption of 36 mA. Output to input isolation (reverse gain) is 40 dB, which is one of the highest available in the industry. Pin configuration has been optimized for convenient ground plane connections and the use of controlled impedance lines.

The device is available in a plastic U-PACK-5 package.

8

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Beyond which damage may occur)[1]

Supply Voltage	12.0 V	Operating Temperature Range	-40 to +85 °C
Power Dissipation	1,000 mW	Lead Soldering Temperature (10 sec.)	240 °C
Storage Temperature Range	-55 to +150 °C	Junction Temperature	150 °C

[1]Operation at any Absolute Maximum Rating is not implied. See Electrical Specifications for proper nominal applied conditions in typical applications. Application of multiple maximum rating conditions at the same time may damage the device.

ELECTRICAL SPECIFICATIONS

T_A = +25 °C, Z_S=Z_L=50 Ω, V_{CC} = +9 V unless otherwise specified.

PARAMETERS	TEST CONDITIONS	SYMBOL	MIN	TYP	MAX	UNITS
Operating Voltage Range		V_{CC}	6.0	9.0	10.5	V
Supply Current		I_{CC}	30	36	43	mA
Forward Gain	F=100 MHz	S_{21}	14	15		dB
Reverse Gain	F=100 MHz	S_{12}		-40		dB
Input Reflection	F=100 MHz	S_{11}		-20		dB
Output Reflection	F=100 MHz	S_{22}		-17		dB
Bandwidth	(-3 dB)	BW	250	270		MHz
Power Out at 1 dB Compression	F=100 MHz	P_{OUT}		+11		dBm
Third Order Intercept Point	F=100 MHz	IP_3		+20		dBm

Note 1: Derate above T_A=25 °C at 8 mW/°C. Maximize pad under device.

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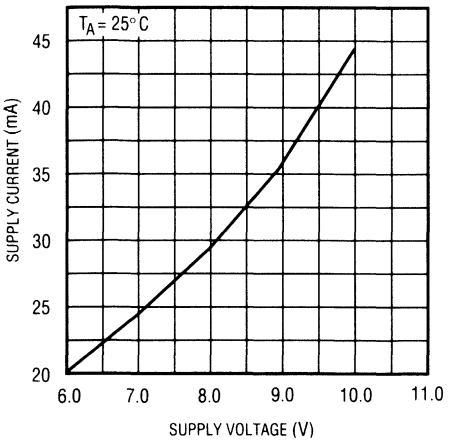
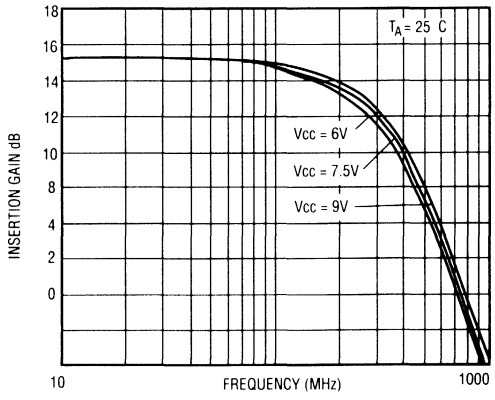
TYPICAL PERFORMANCE CHARACTERISTICS

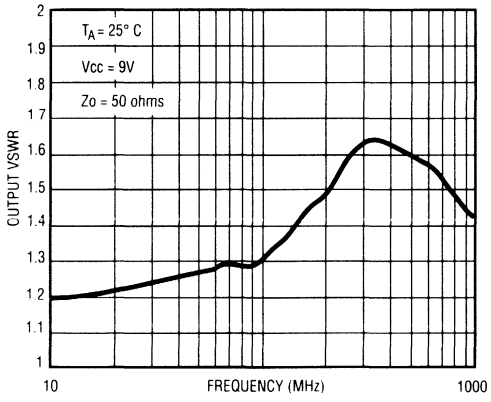
SUPPLY CURRENT vs SUPPLY VOLTAGE



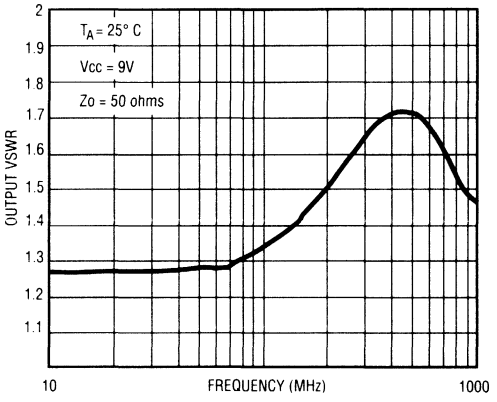
S21 vs FREQUENCY



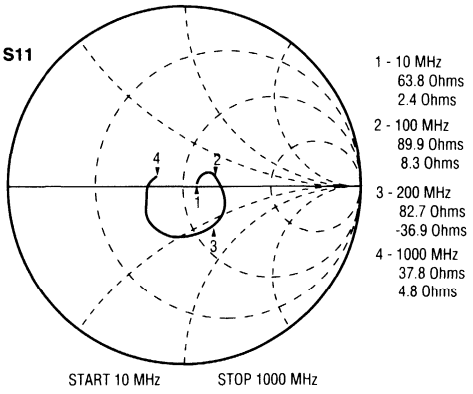
INPUT VSWR vs FREQUENCY



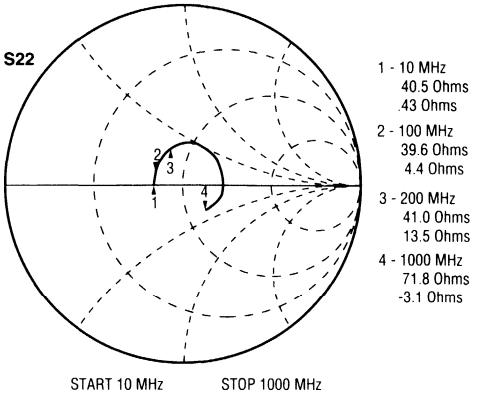
OUTPUT VSWR vs FREQUENCY



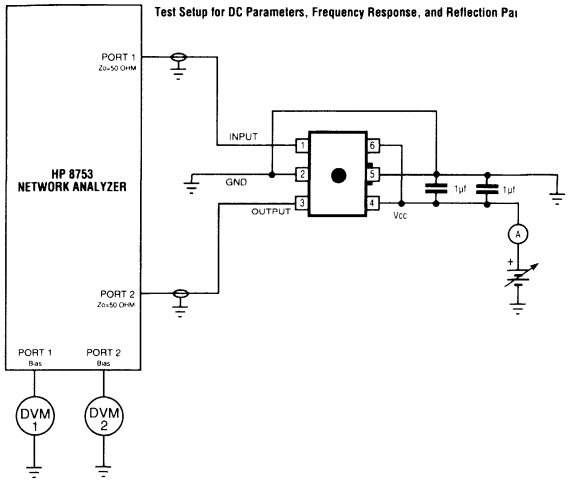
S11



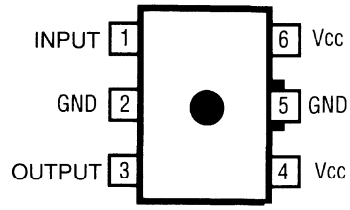
S22



TEST CIRCUIT



PIN ASSIGNMENTS



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LEADERSHIP IN DATA CONVERSION AND SIGNAL PROCESSING

4755 Forge Road, Co. Springs, CO 80907
PH: (719) 528-2300; Fax: (719) 528-2370 SPT

SIGNAL PROCESSING TECHNOLOGIES

SPT203

RF AMPLIFIER

PRELIMINARY INFORMATION

FEATURES

- 500 MHz Bandwidth
- 5.0 dB Noise Figure
- 23 dB Insertion Gain
- +4 dBm 1 dB Compression Point
- Adaptive Impedance Matching (Input and Output Impedances Matched to 50 or 75 ohms)
- Surface-Mount Packages
- Available on Tape-and-Reel

APPLICATIONS

- RF Communications
- Telecommunications
- Local Area Networks
- Personal Communications Equipment
- Portable Instrumentation
- Portable Consumer Equipment
- Radio Control Systems

GENERAL DESCRIPTION

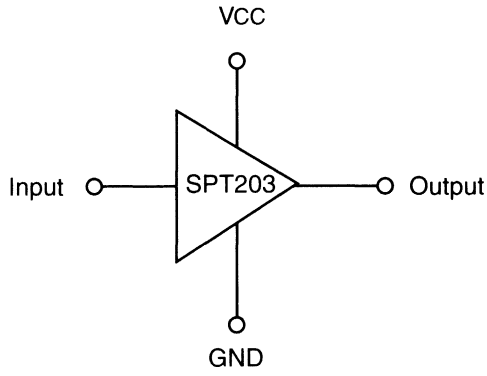
The SPT203 is a high-frequency amplifier with an insertion gain of 23 dB. The -3 dB bandwidth is 500 MHz. The device operates on a 6 V single supply, and it requires no external components other than input and output decoupling capacitors. A unique feature of this device is its ability to achieve good impedance matching in 50 and 75 Ω systems. This happens because the external source and termination impedances have an effect on the internal feedback network in such a way that input and output impedances will adapt to the external source and termination impedances.

The SPT203 has a 1 dB compression point of +4 dBm at the output and a total power supply consumption of 23 mA. Pin configuration has been optimized for convenient ground plane connections and the use of controlled impedance lines.

The device is available in plastic U-PACK-5 and MFP-8 plastic surface-mount packages.

8

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Beyond which damage may occur)[1]

Supply Voltage ..... 12.0 V
Power Dissipation (MFP-8)[2] ..... 600 mW
Power Dissipation (U-PACK-5)[3] ..... 1,000 mW

Storage Temperature Range ..... -55 to +150 °C
Operating Temperature Range ..... -40 to +85 °C
Lead Soldering Temperature (10 sec.) ..... 240 °C
Junction Temperature ..... 150 °C

[1]Operation at any Absolute Maximum Rating is not implied. See Electrical Specifications for proper nominal applied conditions in typical applications. Application of multiple maximum rating conditions at the same time may damage the device.
[2]Derate above T_A=25 °C at 4 mW/°C.
[3] Derate above T_A=25 °C at 8 mW/°C. Maximize pad size under GND and V_{CC} terminals for good heat conduction.

ELECTRICAL SPECIFICATIONS

T_A = +25 °C, V_{CC} = +6 V unless otherwise specified.

PARAMETERS	TEST CONDITIONS	SYMBOL	MFP-8 MIN	MFP-8 TYP	MFP-8 MAX	U-PACK-5 MIN	U-PACK-5 TYP	U-PACK-5 MAX	UNITS
Operating Voltage Range		V_{CC}	4.5	6.0	6.5		6.0		V
Supply Current		I_{CC}	20	23	28		23		mA
Forward Gain	F=100 MHz	S_{21}	21	23	25		23		dB
Reverse Gain	F=100 MHz	S_{12}		-30			-30		dB
Input Reflection	F=100 MHz	S_{11}		-17			-17		dB
Output Reflection	F=100 MHz	S_{22}		-25			-25		dB
Third Order Intercept Point	F=100 MHz	IP_3		+12			+12		dBm
Noise Figure	F=100 MHz	NF		+5.0			+5.0		dB
Bandwidth	(-3 dB)	BW	450	500			470		MHz
Power Out at 1 dB Compression	F=100 MHz	P_{OUT}		+4.0			+4.0		dBm

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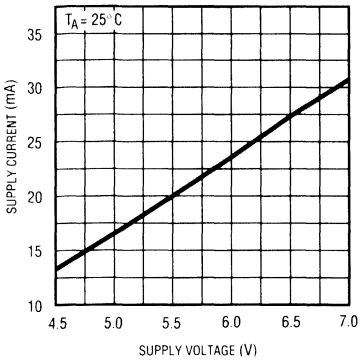
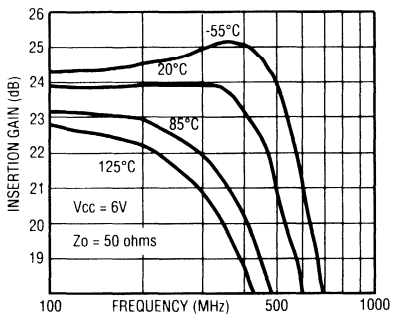
TYPICAL PERFORMANCE CHARACTERISTICS

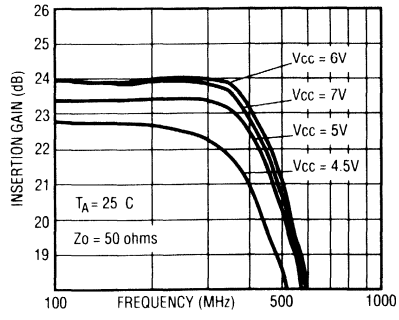
SUPPLY CURRENT vs SUPPLY VOLTAGE



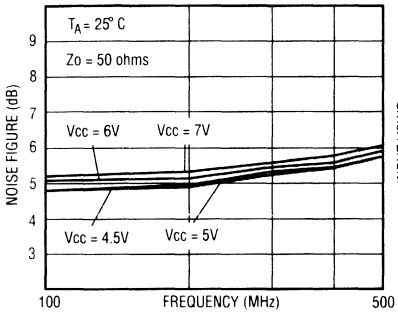
S21 vs FREQUENCY



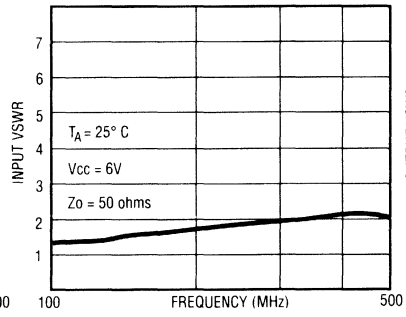
S21 vs FREQUENCY



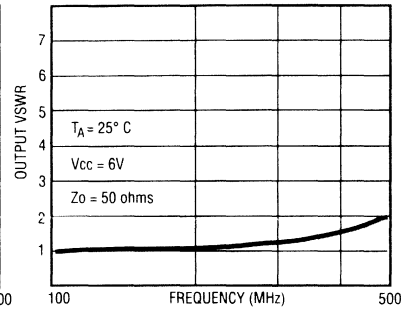
NOISE FIGURE vs FREQUENCY



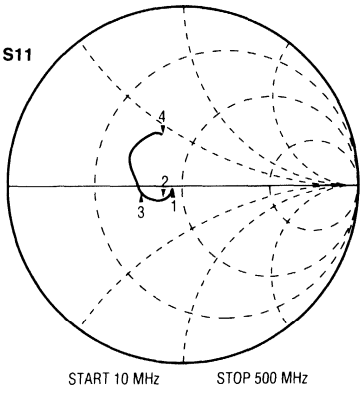
INPUT VSWR vs FREQUENCY



OUTPUT VSWR vs FREQUENCY



S11



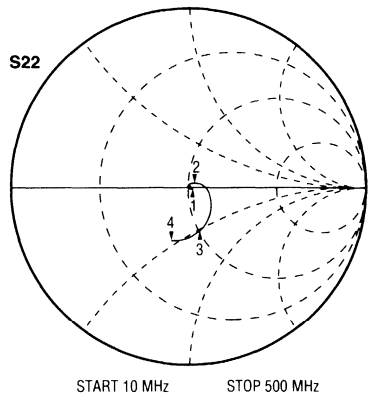
1 - 10 MHz
44.2 Ohms
-1.3 Ohms

2 - 100 MHz
39.4 Ohms
-6.7 Ohms

3 - 200 MHz
30.4 Ohms
-2.4 Ohms

4 - 500 MHz
34.6 Ohms
21.3 Ohms

S22



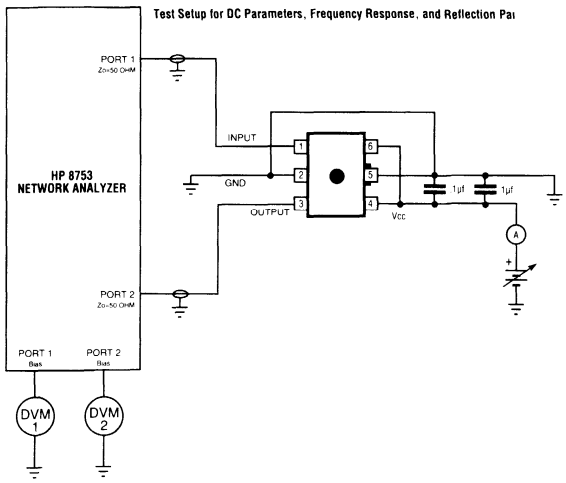
1 - 10 MHz
51.2 Ohms
-1.4 Ohms

2 - 200 MHz
54.0 Ohms
1.7 Ohms

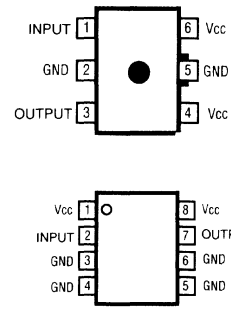
3 - 400 MHz
50.5 Ohms
-25.1 Ohms

4 - 500 MHz
34.4 Ohms
-23.2 Ohms

TEST CIRCUIT



PIN ASSIGNMENTS



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LEADERSHIP IN DATA CONVERSION AND SIGNAL PROCESSING

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GENERAL PRODUCT INFORMATION 1
ORDERING INFORMATION 2
ANALOG-TO-DIGITAL CONVERTERS 3
DIGITAL-TO-ANALOG CONVERTERS 4
COMPARATORS 5
FILTERS 6
VOLTAGE REGULATORS 7
RF AMPLIFIERS 8
POWER CONVERSION PRODUCTS 9
EVALUATION BOARDS 10
APPLICATION NOTES 11
QUALITY ASSURANCE 12
PACKAGE OUTLINES 13
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Section 9 Power Conversion Products

SPT84819 Power Factor Controller/PWM Combo 9-5

9

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SIGNAL PROCESSING TECHNOLOGIES

SPT84819

POWER FACTOR CONTROLLER PWM COMBO

PRELIMINARY INFORMATION

FEATURES

- Reduced Overall Current Consumption
- Reduced Start-Up Current
- Slow Start Following Current Limit Shutdown
- Boost Mode Power Factor Control
- Current or Voltage Mode PWM
- Peak Current Sensing PFC Control
- Typical Power Factor > .996
- Current Limit and Over Voltage Protection
- Programmable Ramp Compensation
- Electrostatic Discharge Protection
- Pin Compatible with the ML4819

APPLICATIONS

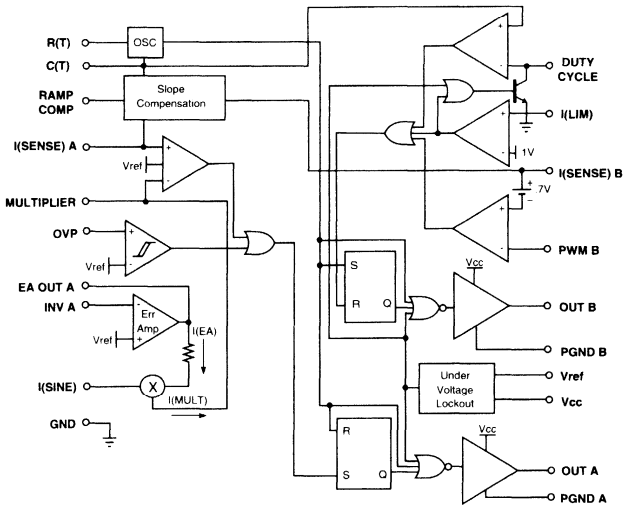
- Switching Power supplies with PFC
- Computers
- Work Stations
- Telecommunications Equipment
- Office Equipment
- Medical Electronics
- IEC-555 Power Supplies

DESCRIPTION

The SPT84819 is a complete boost mode Power Factor Control (PFC) circuit which also includes a PWM controller. The PFC circuit and PWM controller share the same oscillator and are synchronized. The outputs of the controller provide high current (>1 A peak) and high slew rate for excellent control of MOSFET gates. The PFC section utilizes peak current sensing control circuitry, with a current sense transformer or a SENSE FET device as a sense element. This non-dissapative method of current sensing improves overall efficiency. The PWM section includes cycle by cycle current limiting, precise duty cycle limiting for single ended converters, and slope compensation. Special care has been taken to provide high system noise immunity. The device has under voltage lockout circuitry with 6 V hysteresis, wide common mode range current sense comparators and precision duty cycle limiting circuit for the PWM section.

9

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Beyond which damage may occur)[1]

Supply Voltage ..... 35 V
Output Current, Source or Sink (Pin 14,16) DC ..... 1.0 A
Output Energy (Capacitive Load Per Cycle) ..... 5 µj
Multiplier I(SINE) Input Pin 6 ..... 1.2 mA
Analog Inputs ..... -0.3 V to 5.5 V
Storage Temperature Range ..... -65 to +150 °C

Operating Temperature Range
(SPT84819D) ..... 0 to +70 °C
(SPT84819DA) ..... -40 to +85 °C
Lead Soldering Temp. (10sec.) ..... 260 °C
Junction Temperature ..... 150 °C
Thermal Resistance, Plastic Dip ..... 65 °C/W

Operation at any Absolute Maximum Rating is not implied. See Electrical Specifications for proper nominal applied conditions in typical applications. Application of multiple maximum rating conditions at the same time may damage the device.

ELECTRICAL SPECIFICATIONS

R_T = 14 KΩ, C_T = 1000 pF, T_A= Operating Temperature Range; V_{CC} = 15 V (Note 2)

TEST PARAMETERS	CONDITIONS	SYMBOL	SPT84819D MIN	SPT84819D TYP	SPT84819D MAX	SPT84819DA MIN	SPT84819DA TYP	SPT84819DA MAX	UNITS
Oscillator									
Initial Accuracy	T_J = 25°C	$f_{INTL(OSC)}$	90	97	104	90	97	104	kHz
Voltage Stability	12 V< V_{CC} < 25 V	$\Delta f_{V(OSC)}$		3			3		%
Temperature Stability		$\Delta f_{T(OSC)}$		2			2		%
Total Variation	Line, Temp	$\Delta f_{(OSC)}$	88		106	84		110	kHz
Ramp Valley		$V_{RV(OSC)}$		.9			.9		V
Ramp Peak		$V_{RP(OSC)}$		4.3			4.3		V
R(T) Pin Voltage		$V_{RT(OSC)}$	4.8	5.0	5.3	4.78	5.0	5.3	V
Discharge Current	T_J=25 °C, V_{PIN20}=2 V	$I_{D(OSC)}$	7.5	8.4	9.3	7.5	8.4	9.3	mA
(Pin 10 Open)	V_{PIN20} = 2 V		7.2	8.4	9.5	7.0	8.4	10.0	mA
Duty Cycle Comp.									
Input Offset Voltage		$V_{OS(DCC)}$	-15		+15				mV
Input Bias Current		$I_{B(DCC)}$		-0.7	-10		-0.7	-10	µA
Duty Cycle	V_{PIN7} = V_{REF} /2	$\partial_{(DCC)}$	42	45	48.5	40	45	49	%
Reference Section									
Output Voltage	I_O = 1 mA, T_J = 25 °C	$V_{(REF)}$	4.95	5.00	5.05	4.95	5.00	5.05	V
Line Regulation	12 V < V_{CC} < 25 V	$LI_{REG(REF)}$		2	35		2	65	mV
Load Regulation	1 mA< I_O< 20 mA	$LD_{REG(REF)}$		8	25		8	30	mV
Temperature Stability		$_{\Delta}V_{T(REF)}$		.4			.4		%
Total Variation	Line, Load, Temp	$_{\Delta}V_{TOT(REF)}$	4.9		5.1	4.75		5.25	V
Output Noise Voltage	10 Hz to 10 kHz	$V_{N(REF)}$		50			50		µV
Long Term Stability	T_J =125 °C, 1000hrs (Note 1)	$V_{LT(REF)}$		5	25		5		mV
Short Circuit Current	V_{REF} = 0 V	$I_{SC(REF)}$	-30	-85	-180	-25	-85	-185	mA
Error Amp Section									
Input Offset Voltage		$V_{OS(EA)}$	-15		+15				mV
Input Bias Current		$I_{B(EA)}$		-0.1	-1.0		-0.1	-1.0	µA
Open Loop Gain	1 V< V_{PIN4} < 5 V	$A_{V(OL,EA)}$	60	75			75		dB
PSRR	12 V< V_{CC}< 25 V	$PSRR_{(EA)}$	60	90			90		dB
Output Sink Current	V_{PIN4}=1.1 V, V_{PIN5}=5.2 V	$I_{SINK(EA)}$	2	12		1.5	12		mA
Output Source Current	V_{PIN4}=5.0 V,V_{PIN5}=4.8 V	$I_{SOURCE(EA)}$	-0.5	-1.0		-0.35	-1.0		mA
Output High Voltage	I_{PIN4} = -0.5 mA, V_{PIN5}= 4.8 V	$V_{OH(EA)}$	6.5		7.0		6.3	7.0	V
Output Low Voltage	I_{PIN4}= 2 mA, V_{PIN5}= 5.2 V	$V_{OL(EA)}$		0.7	1.1		0.7	1.2	V
Unity Gain Bandwidth		$BW_{(EA)}$		1.0			1.0		MHz

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SPT

ELECTRICAL SPECIFICATIONS

R_T = 14 kΩ, C_T = 1000 pF, T_A= Operating Temperature Range; V_{CC} = 15 V (Note 2)

PARAMETERS	TEST CONDITIONS	SYMBOL	SPT84819D MIN	SPT84819D TYP	SPT84819D MAX	SPT84819DA MIN	SPT84819DA TYP	SPT84819DA MAX	UNITS
Multiplier									
I(SINE) Input Voltage	I(SINE) = 500 µA	$V_{ISINE(M)}$	0.4	.7	0.9	.4	.7	1.1	V
Output Current (pin 3)	I(SINE)=500 µA, PIN5=V_{REF}-20 mV	$I_{OUT(M)}$	450	495	520	450	495	520	µA
	I(SINE)=500 µA, PIN5=V_{REF}+20mV			0	10		0	40	µA
	I(SINE)=1 mA, PIN5=V_{REF}-20 mV		920	990	1035	920	990	1035	µA
Bandwidth		$BW_{(M)}$		200			200		kHz
PSRR	12 V < V_{CC} <25 V	$PSRR_{(M)}$		70			70		dB
Slope Compensator									
RAMP COMP V_{PIN} 12		$V_{R(SC)}$		V_{PIN20} -1			V_{PIN20} -1		V
I_{OUT} Pin 1 or Pin 9	I_{PIN12} = 100 µA (NOTE 3)	$I_{R(SC)}$	45	48	51	40	48	55	µA
OVP Comparator									
Input Offset Voltage		$V_{OS(OVP)}$	-15		+15				mV
Hysteresis	Output Off	$V_{H(OVP)}$	100	120	130	70	120	150	mV
Input Bias Current		$I_{B(OVP)}$		-0.15	-3		-0.15	-3.0	µA
Propagation Delay		$\Delta t_{(OVP)}$		150			150		ns
I(SENSE) Comp. A, B									
Input CMR	V_{PIN5} = V_{REF} - 20mV	$V_{CMR(SENSE)}$	-0.2		5.5	-0.2		5.5	V
Input Offset Voltage	I(SENSE) A	$V_{OS(SENSE)}$	-15		+15				mV
	I(SENSE) B		+0.4	0.7	+0.9	0.38	0.7	0.92	V
Input Bias Current		$I_{B(SENSE)}$		-0.7	-10		-0.7	-10	µA
Input Offset Current		$I_{OS(SENSE)}$	-1		+1				µA
Propagation Delay		$\Delta t_{(SENSE)}$		150			150		ns
I(limit A) Trip Point	V_{PIN3} = 5.5 V	$I_{LIM(SENSE)}$	4.8	5	5.2	4.75	5	5.25	V
I(LIM) Comparator									
I(LIMIT) Trip Point		$V_{TRIP(LIM)}$	0.95	1.0	1.05	0.9	1.0	1.10	V
Input Bias Current		$I_{B(LIM)}$		-0.7	-10		-0.7	-10	µA
Propagation Delay				150			150		ns
Output Section A,B									
Output Voltage Low	I_{OUT} = -20mA	$V_{OH(O)}$		0.1	0.4		0.1	0.5	V
	I_{OUT} = -200mA			1.6	2.2		1.6	2.3	V
Output Voltage High	I_{OUT} = 20mA		13	13.5		12.5	13.5		V
	I_{OUT} = 200mA		12	13.4		11.5	13.4		V
V_{OUT} Low in UVLO	I_{OUT} = -1mA, V_{CC} = 8V	$V_{ULVO(O)}$		0.65	0.8		0.65	1.0	V
Output Rise/Fall Time	C_L = 1000pF	$t_{R(O)}$; $t_{F(O)}$		50			50		ns
Undervoltage Lockout									
Start-Up Threshold		$V_{ST(UVLO)}$	15	16	17	14.5	16	17.5	V
Shutdown Threshold		$V_{SD(UVLO)}$	9	10	11	8.5	10	11.5	V
V_{REF} Good Threshold		$V_{RG(UVLO)}$		4.4			4.4		V
Supply Current	Start-Up, V_{CC} = 14V	I_{TOT}		0.27	0.5		0.27	0.6	mA
	Operating T_J = 25°C			25	35		25	45	mA

Note 1: Parameter is not 100% tested in production but guaranteed by design.

Note 2: V_{CC} is raised above the startup threshold first to activate the IC, then returned to 15 V.

Note 3: PWM comparator bias currents are subtracted from this reading.

GENERAL DESCRIPTION

OSCILLATOR

The SPT84819 oscillator charges the external capacitor (C_T) with a current (I_{SET}) equal to $5/R_{SET}$. When the capacitor voltage reaches the upper threshold, the comparator changes state and the capacitor discharges to the lower threshold through Q1. While the capacitor is discharging, the clock pulse is high.

The Oscillator period can be described by the following relationship: $T_{OSC} = T_{RAMP} + T_{DEADTIME}$

where: $T_{RAMP} = \frac{C_V \times V_\Delta}{I_{SET}}$ and: $T_{DEADTIME} = \frac{C_V \times V_\Delta}{(8.4\,mA - I_{SET})}$

The maximum duty cycle of the PWM section can be limited by setting a threshold on pin 7. When the (C_T) ramp is above the threshold at pin 7, the PWM output is held off and the PWM flip-flop is set:

$$D_{LIMIT} = \frac{D_{OSC} \text{ X } (Y_{PIN7} - 0.9)}{3.4}$$

Where:
D_{LIMIT} = Desired duty cycle
D_{OSC} = Oscillator duty cycle

Figure 1 - Oscillator Block Diagram

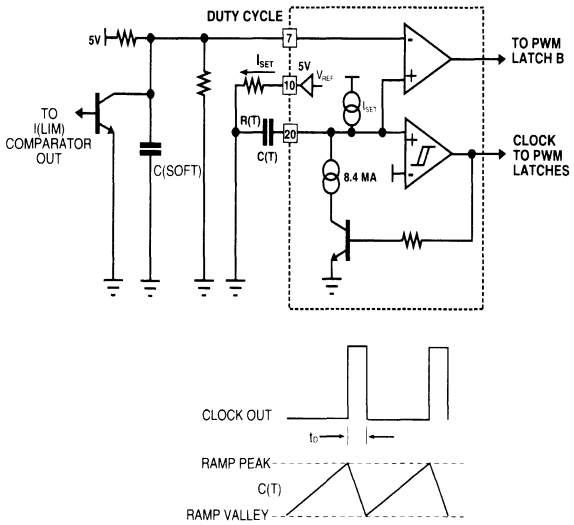


Figure 2 - Oscillator Timing Resistance vs. Frequency

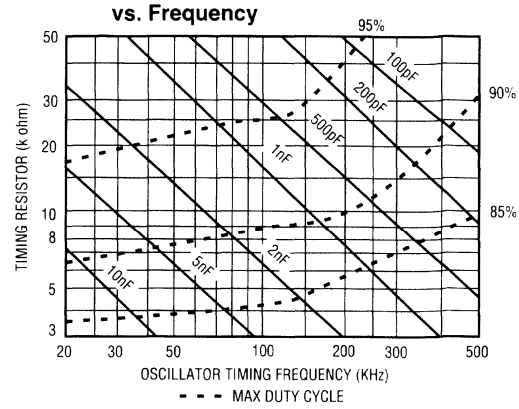
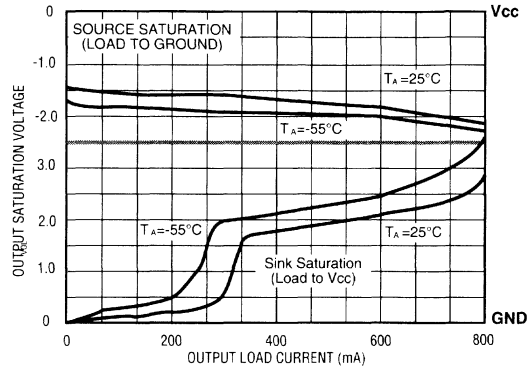


Figure 3 - Output Saturation Voltage vs. Output Current



A capacitor from pin 7 to ground can be used for soft start when the current limit threshold (pin 11) is exceeded.

ERROR AMPLIFIER

The SPT84819 error amplifier is a high open loop gain, wide bandwidth amplifier.

Figure 4 - Error Amplifier

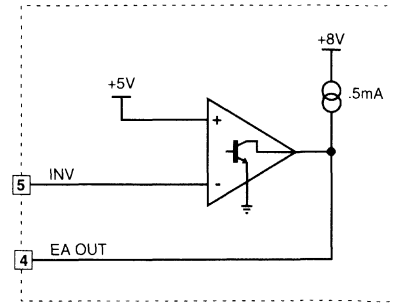


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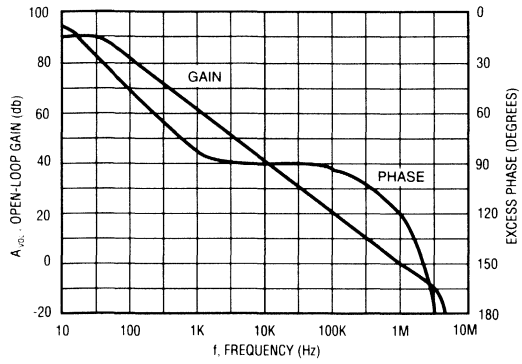
Figure 5 - Error Amp Open-Loop Gain and Phase vs. Frequency



MULTIPLIER

The SPT84819 multiplier is a linear current input multiplier to provide high immunity to the disturbances caused by high power switching. The rectified line input sine wave is converted to a current via a dropping resistor. In this way, small amounts of ground noise produce an insignificant effect on the reference to the PWM comparator.

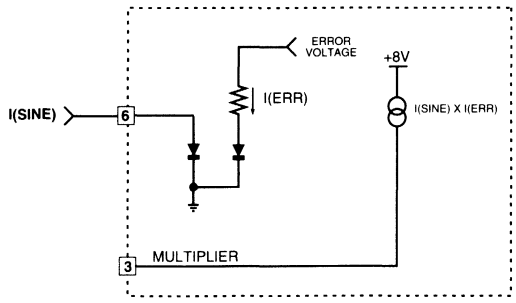
The output of the multiplier is a current proportional to :

$$I_{OUT} \propto I(SINE) \times I(EA)$$

Where: I(SINE) is the current in the dropping resistor, and I(EA) is a factor which varies from 0 to 1 proportional to the output of the error amplifier. When the error amplifier is saturated high, the output of the multiplier is approximately equal to the I(SINE) input current.

The multiplier output current is converted into the reference voltage for the PWM comparator through a resistor to ground on the multiplier output (pin 3).

Figure 6 - Multiplier Block Diagram



SLOPE COMPENSATION

Slope compensation is accomplished by adding 1/2 of the current flowing out of pin 12 to pin 1 (for the PFC section). The amount of slope compensation is equal to:

$$(I_{PIN12}/2) \times R_L$$

Where: R_L is the impedance to ground on pin 1 or pin 9.
Since most of the PWM applications will be limited to 50% duty cycle, slope compensation should not be needed for the PWM section. This can be defeated by using a low impedance load to the current sense on pin 9.

Figure 7 - Slope Compensation

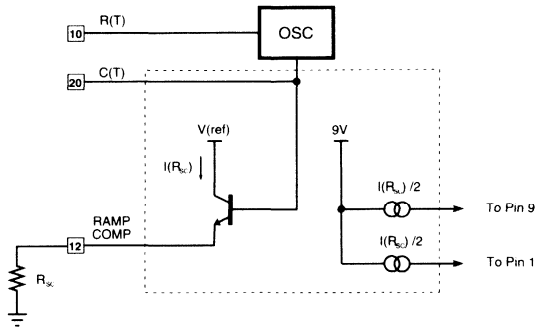
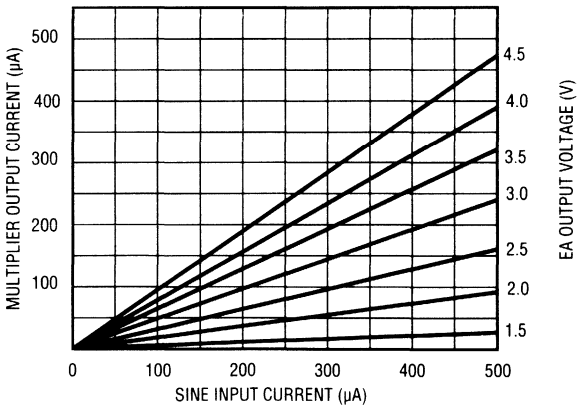


Figure 8 - Multiplier Linearity



UNDER VOLTAGE LOCKOUT

On power up the SPT84819 remains in the UVLO condition; output low and quiescent current low. The IC becomes operational when V_{CC} reaches 16 V. When V_{CC} drops below 10 V, the UVLO condition is imposed. During the UVLO condition, the 5 V V_{REF} pin is "off," making it usable as a "flag."

Figure 9 - Under Voltage Lockout

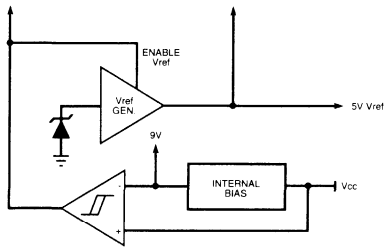


Figure 10 - Total Supply Current vs. Supply Voltage

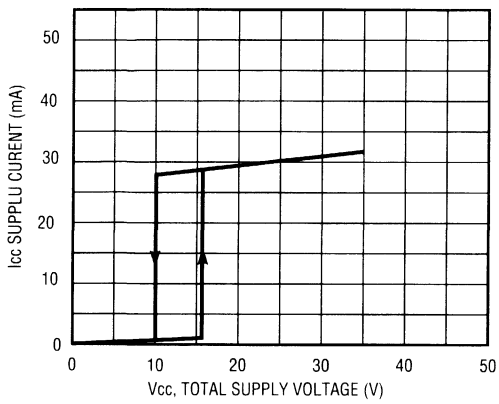


Figure 11 - Total Supply Current vs. Temperature

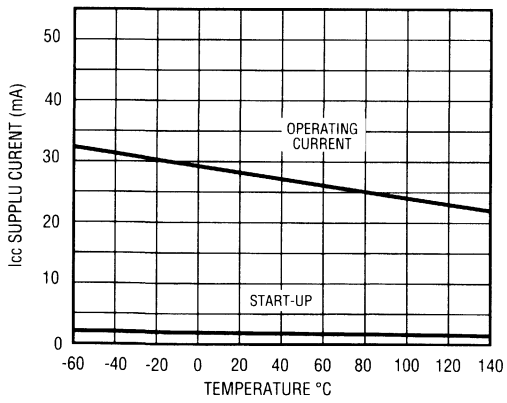
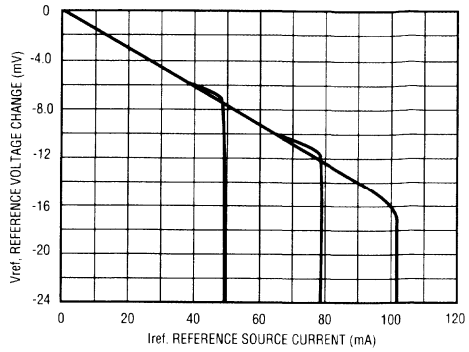


Figure 12 - Reference Load Regulation



APPLICATIONS

POWER FACTOR SECTION

The power factor section is a boost mode pre-regulator that provides approximately 380 volts DC for the PWM section. It utilizes peak current sensing to give a typical corrected power factor of .996 over all load conditions. The following calculations refer to the applications circuit.. The component designators in the equations below refer to the following components in the schematic in figure 14.

$$R_T = R15,\ C_T = C6$$

INPUT INDUCTOR (L1) SELECTION

The central component in the regulator is the input boost inductor. The value of this inductor controls various critical operational aspects of the regulator. If the value is too low, the input current distortion will be high and will result in low power factor and increased noise at the input. This will require more input filtering. In addition, when the value of the inductor is low the inductor dries out (runs out of current) at low currents. Thus the power factor will decrease at lower power levels and/or higher line voltages. If the inductor value is too high for a given operating current, the required size of the inductor core will be large and/or the required number of turns will be high. Balance must be reached between distortion and core size. Another condition where the inductor can dry out is analyzed below where it is shown to be maximum duty cycle dependent.

For the boost converter at steady state:

$$V_{OUT} = \frac{V_{IN}}{1 - D}$$

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Where D_{ON} is the duty cycle ($T_{ON}/(T_{ON} + T_{OFF})$. The input boost inductor will dry out when the following condition is satisfied:

$$V_{IN}(t) < V_{OUT} \times (1 - D_{ON})$$

$$V_{INDRY} = (1 - D_{ON\,(max)}) \times V_{OUT}$$

V_{INDRY}: Voltage where the inductor dries out

V_{OUT}: Output DC Voltage

Effectively, the above relationship shows that the resetting volt-seconds are more that setting volts-seconds. In energy transfer terms, this means that less energy is stored in the inductor during the ON time than it is asked to deliver during the OFF time. The net result is that the inductor dries out. The recommended maximum duty cycle is 95% at 100 kHz to allow time for the input inductor to dump its energy to the output capacitors.

For example:

if: $V_{OUT} = 380$ V and
$D_{ON\,(max)} = 0.95$

then substituting in (3) yields $V_{INDRY} = 20$ V . The effect of drying out is an increase in distortion at low voltages.

For a given output power, the instantaneous value of the input current is a function of the input sinusoidal voltage waveform, i.e. as the input voltage sweeps from zero volts to a maximum value equal to its peak so does the current.

The load of the power factor regulator is usually a switching power supply which is essentially a constant power load. As a result, an increase in the input voltage will be offset by a decrease in the input current.

By combining the ideas set forth above, some ground rules can be obtained for the selection and design of the input inductor:

Step 1: Find minimum operating current.

$$I_{IN}(min)PEAK = \frac{1.414 \times P_{IN}(min)}{V_{IN}(max)}$$

$V_{IN(max)} = 260$ V

$P_{IN(min)} = 50$ W

then: $I_{IN(min)} = 0.272$A

Step 2: Choose a minimum current at which point the inductor current will be on the verge of drying out. For this example 40% of the peak current found in step 1 was chosen. Then:

$$I_{LDRY} = 100 \text{ mA}$$

Step 3: The value of the inductance can now be found using previously calculated data.

$$L1 = \frac{V_{INDRY} \times D_{ON(max)}}{L_{INDRY} \times f_{OSC}}$$

$$= \frac{20 \text{ V} \times 0.95}{100 \text{ mA} \times 100 \text{ kHz}} = 2 \text{ mH}$$

The inductor can be allowed to decrease in value when the current sweeps from minimum to maximum value. This allows the use of smaller core sizes. The only requirement is that the ramp compensation must be adequate for the lower inductance value of the core so that there is adequate compensation at high current.

Step 4: The presence of the ramp compensation will change the dry out point, but the value found above can be considered a good starting point. Based on the amount of power factor correction, the above value of L1 can be optimized after a few iterations.

Gapped Ferrites, Molypermalloy, and Powered Iron cores are typical choices for core material. The core material selected should have a high saturation point and acceptable losses at the operating frequency.

One ferrite core that is suitable at around 200 W is the T157-18 made by Micrometals. Two of these toroids are stacked with 140 turns of AWG #20 to provide 2 millihenries at 2 amps DC.

9

OSCILLATOR COMPONENT SELECTION

The oscillator timing components can be calculated by using the following expression:

$$f_{OSC} = \frac{1.36}{R_T \, C_T}$$

For example:

Step 1: At 100 kHz with 95% duty cycle $T_{OFF} = 500$ ns calculate C_T using the following formula:

$$C_T = \frac{T_{OFF} \times I_{DIS}}{V_{OSC}} = 1000 \text{ pF}$$

Step 2: Calculate the required value of the timing resistor.

$$R_T = \frac{1.36}{f_{OSC} \times C_T} = \frac{1.36}{100 \text{ kHz} \times 1000 \text{ pF}} = 13.6 \text{ k}\Omega$$

Choose $R_T = 14$ kΩ

CURRENT SENSE AND SLOPE (RAMP) COMPENSATION COMPONENT SELECTION

Slope compensation in the SPT84819 is provided internally. A current equal to $V_{C(T)}/2(R18)$ is added to I(SENSE) A (pin 1). This is converted to a voltage by R10, adding slope to the sensed current through T1. The amount of slope compensation should be at least 50% of the downslope of the inductor current during the off time as reflected on pin 1. Note that slope compensation is a requirement only if the inductor current is continuous and the duty cycle is more than 50%. The highest inductor downslope is found at the point of inductor discontinuity:

$$\frac{d_{IL}}{dt} = \frac{V_b - V_{INDRY}}{L} = \frac{380\ V - 20\ V}{2\ mH}$$

The downslope as reflected to the input of the PWM comparator is given by:

$$S_{PWM} = \frac{V_b - V_{INDRY}}{L1} \times R11/Nc$$

Where Nc is the turns ratio of the current transformer (T1) used. In general, current transformers simplify the sensing of switch currents especially at high power levels where the use of sense resistors is complicated by the amount of power they have to dissipate. Normally the primary side of the transformer consists of a single turn and the secondary consists of several turns of either enameled magnet wire or insulated wire. We have used a standard Beckman Industrial HM31-20100 current sense transformer. The rectifying diode at the output of the current transformer can be a 1N4148 for secondary currents up to 75 mA average. Sense FETs or resistive sensing can also be used to sense the switch current, the sensed signal has to be amplified to the proper level before it is applied to the IC.

The value of ramp compensation (SC_{PWM}) as seen at pin1 is:

$$SC_{PWM} = \frac{2.5 \times R9}{R15 \times C6 \times R18}$$

The required value for R18 can be found by:

$$SC_{PWM} = A_{SC} \times S_{PWM}$$

where A_{SC} is the amount of slope compensation and solving for R18

The value of R9 (pin2) depends on the selection of R2 (pin6)

$$R2 = \frac{V_{IN(max)\ PEAK}}{Isine(PEAK)} = \frac{260 \times 1.414}{0.72\ mA} = 510\ k\Omega$$

$$R9 > \frac{V_{CLAMP} \times R2}{V_{IN(min)\ PEAK}} = \frac{4.8 \times 510\ K}{80 \times 1.414} \approx 22\ k\Omega$$

Choose R9 = 27 kΩ

The peak inductor current can be found approximately by:

$$Ipeak = \frac{1.414 \times P_{OUT}}{V_{IN(min)RMS}} = \frac{1.414 \times 200}{90} = 3.14\ A$$

The selection of Nc which depends on the maximum switch current, assume 4A for this example is 80 turns,

$$R11 = \frac{V_{CLAMP} \times Nc}{I_{PEAK}} = \frac{4.8 \times 80}{4} \approx 100\ Ohms$$

Where R11 is the sense resistor, and Vclamp is the current clamp at the inverting input of the PWM comparator. The clamp is internally set to 5 V. In actual application it is a good idea to assume a value less than 5 V to avoid unwanted current limiting action due to component tolerances. In the application Vclamp was chosen as 4.8 V. Having calculated R11 the value S_{PWM} and of R18 can now be calculated:

$$S_{PWM} = \frac{380\ V - 20}{2\ mH} \times \frac{100}{80} = 0.225\ V/\mu s$$

$$R18 = \frac{2.5 \times R9}{A_{SC} \times S_{PWM} \times R_T \times C_T}$$

$$R18 = \frac{2.5 \times 27\ K}{0.7 \times (.225 \times 10\ ) \times 14\ K \times 1\ nF} \approx 30\ k\Omega$$

Choose R18 = 33 kΩ
The following values were used for calculation:
R9 = 27 kΩ, Asc = 0.7, Rt = 14 kΩ, Ct = 1nF

VOLTAGE REGULATION COMPONENTS

The value of the regulation loop components are calculated based on the operating output voltage. Note that safety regulations require the use of sense resistors that have adequate voltage rating. As a rule, if 1/4 watt resistors are available, two should be used in series. The input bias current of the error amplifier is approximately 0.5 µA, therefore the current available from the voltage sense resistors should be significantly higher than this value. Since two 1/4 watt resistors have to be used, the total power rating is 1/2 W. The operating power is set to be 0.4 W, then with 380 V output voltage, the value can be calculated as follows:

$R5 = (380V)^2/0.4\ W = 360\ k\Omega$
Therefore choose two 178 kΩ 1/4 W 1% resistors connected in series. Then R6 can be calculated as below:

$$R6 = \frac{V_{REF} \times R5}{V_b - V_{REF}} = \frac{5\ V \times 357\ K}{380\ V - 5\ V} = 4.76\ k\Omega$$

Choose 4.75 kΩ 1%

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One more critical component in the voltage regulation loop is the feedback capacitor for the error amplifier. The voltage loop bandwidth should be set such that it rejects the 120 Hz ripple which is present at the output. If this ripple is not adequately attenuated, it will cause distortion of the input current waveform. Typical bandwidths range anywhere from a few Hz to 15 Hz. The main compromise is between transient response and distortion. The feedback capacitor can be calculated using the following formula:

$$C8 = \frac{1}{3.142 \times R5 \times BW} =$$

$$C8 = \frac{1}{3.162 \times 357\,K \times 2\,Hz} = 0.45\,\mu F$$

OVERVOLTAGE PROTECTION (OVP)

The OVP loop should be set so that there is no interaction with the voltage control loop. Typically it should be set to a level where the power components are safe to operate. Ten to fifteen volts above Vout seems to be adequate. This sets the maximum transient output voltage to about 395 V.

By choosing the high voltage side resistor of the OVP circuit the same way as above, (R7 = 356 kΩ) then R8 can be calculated as:

$$R8 = \frac{V_{REF} \times R7}{V_{OVP} - V_{REF}} = \frac{5\,V \times 357\,K}{395\,V - 5\,V} = 4.576\,k\Omega$$

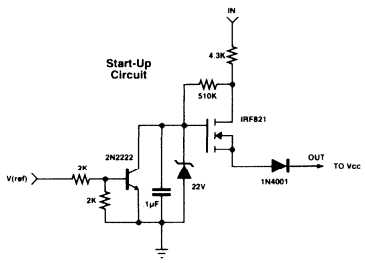
Choose 4.53 kΩ 1%

Note that R5, R6, R7, and R8 should be 1% or better tolerance.

OFF- LINE START-UP AND BIAS SUPPLY GENERATION

The start-up circuit can either be a "bleed resistor" type (39K, 2W) or the circuit shown below. The bleed resistor method offers the advantage of simplicity and lowest cost, but may cause excessive turn-on time at low line voltage.

Figure 13 - Start-Up Circuit



When the voltage on V_{CC} (pin 15) exceeds 16 V, the IC starts up. The energy stored on C10 supplies the IC with running power until the supplemental winding on the output transformer can provide power to sustain operation.

PWM SECTION

The PWM section uses current mode control. Current is sensed through R24 and filtered for high frequency noise and leading edge transients by R23 and C14. The main regulation loop is through PWM B. The TL431 in the secondary serves as both a voltage reference and error amplifier, with isolation provided by an opto-coupler which give a current command signal on pin 8. Loop compensation is provided by R29 and C20. The output voltage is set by:

$$V_{OUT} = 2.5\,x\,(1 + \frac{R29}{R28})$$

The control loop is compensated using standard techniques.

Current is limited to a threshold of 2A(1 V on R24). The duty cycle is limited in this circuit to below 50% to prevent output transformer core saturation. The maximum duty cycle limit of 45% is set using a threshold of Vref/2 on pin 7.

The circuit can be modified for voltage mode operation by using the slope current that appears on pin 9.

The ramp amplitude appearing on pin 9 can be shown as:

$$V_R = \frac{I(R18)}{2}\ X\ R(V)$$

where R18 is the slope compensation resistor. Since this circuit operates with a constant input voltage, (as provided by the PFC section), voltage feed-forward is unnecessary.

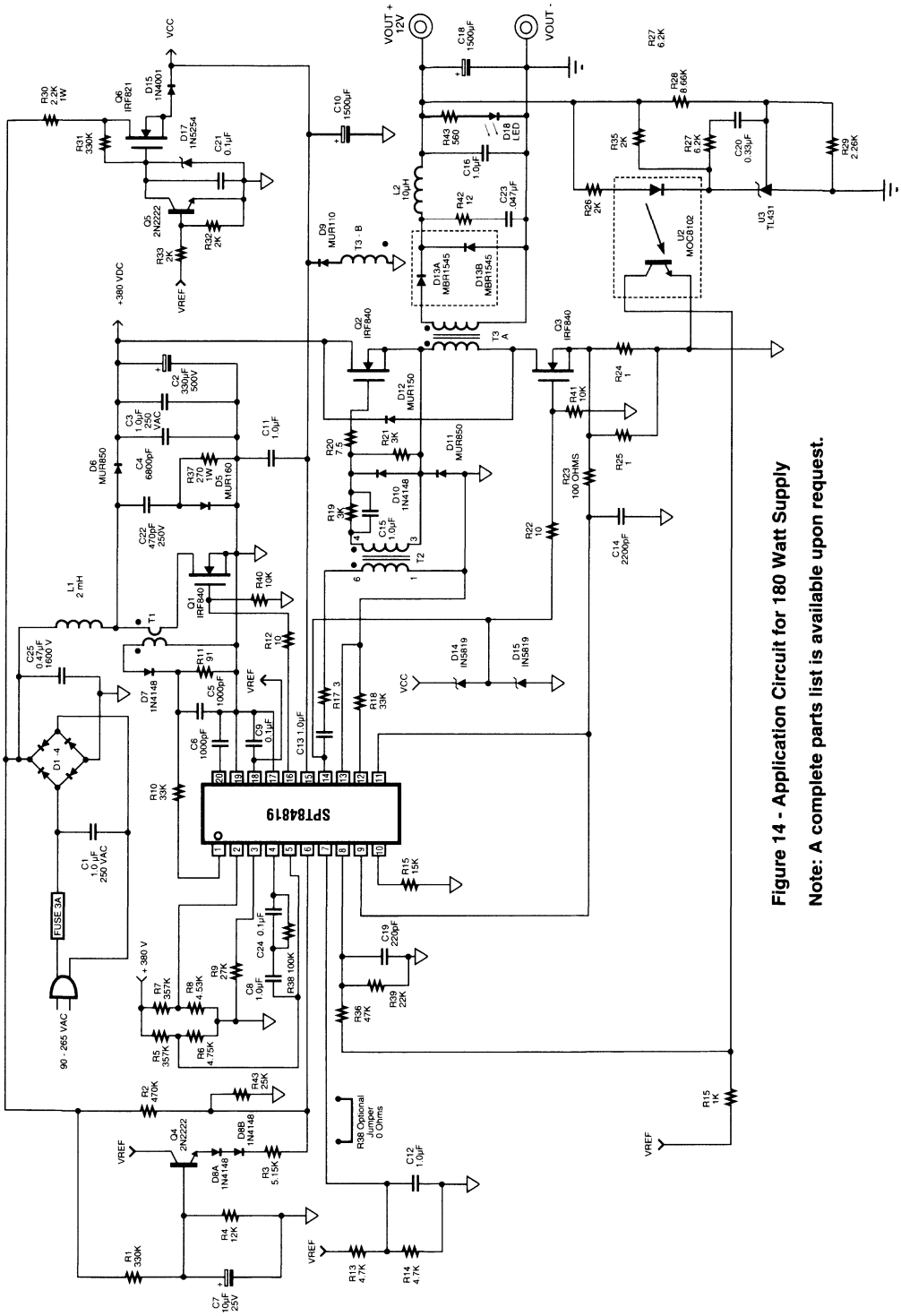


Figure 14 - Application Circuit for 180 Watt Supply

Note: A complete parts list is available upon request.

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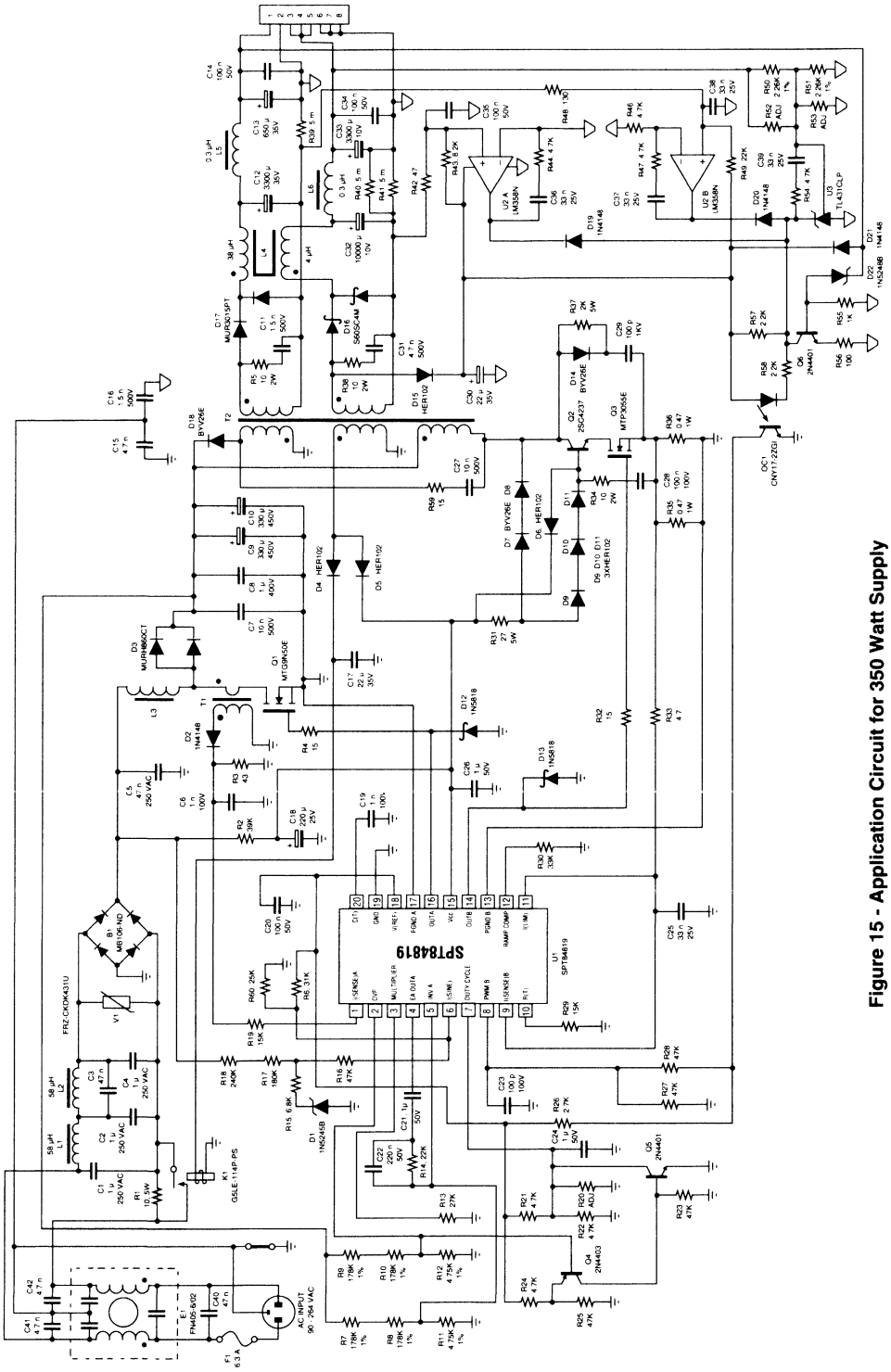

Figure 15 - Application Circuit for 350 Watt Supply

Note: A complete parts list is available upon request.

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Section 10 Evaluation Boards

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SPT
SIGNAL PROCESSING TECHNOLOGIES

EB104
EVALUATION BOARD

FEATURES

- Provides Operating Environment for HADC574Z, HADC674Z, or SPT774 Devices
- Fully Demonstrates Device Function and Resolution
- Eliminates Noisy Breadboard Evaluation Circuitry
- Buffered A/D and D/A Conversion Data Buses
- Includes Sample/Hold-Amp and Output Op Amp ICs
- Unipolar or Bipolar Operation

APPLICATIONS

- Evaluation/Comparison of HADC574/674Z and SPT774 Converters
- System Development
- Data Acquisition Systems
- Bus Structured Instumentation
- Process Control Systems

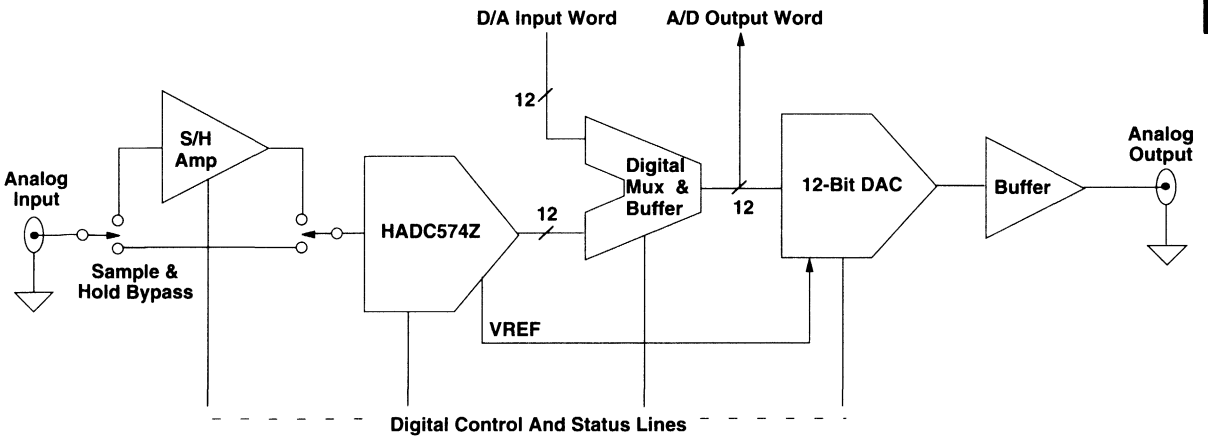
GENERAL DESCRIPTION

The EB104 evaluation board fully demonstrates the capabilities of the HADC574/674Z and SPT774 12-bit analog-to-digital converters. All of the basic power supply connections, control lines, and external components are included. Unlike most laboratory breadboarding, the ground-planed PC board provides the necessary low-noise environment essential for 12-bit resolution. The board makes full use of connectors to allow easy hookup and operation.

Other support provided on the EB104 includes an input sample/hold amplifier, output operational amplifiers and potentiometers for offset and gain adjustments. Customization and function selections are performed by jumper pins.

The EB104 is supplied with an HADC574ZBCJ device. It will support all 574/674/774 type devices.

BLOCK DIAGRAM



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SPT
SIGNAL PROCESSING TECHNOLOGIES

EB105
EVALUATION BOARD

FEATURES

- Complete With Socketed HSCF24040 Device
- Demonstrates HSCF24040 Performance and Capabilities
- Toggle Switches For On-Board Control and Programming
- Connectors Allow Easy Interfacing of External Control, Programming, and Analog Signals
- Crystal Time Base
- Leaded Power Supply Connector

APPLICATIONS

- HSCF24040 Evaluation
- Prototype System Development
- Programmable General Purpose Subassembly

GENERAL DESCRIPTION

The EB105 evaluation board allows full exercise of the HSCF24040 programmable 7th order low pass active filter. Unlike a hand-wired breadboard, this ground-planed, printed circuit board provides a high performance, noise-free environment. It provides full demonstration and evaluation of the superb HSCF24040 dynamic characteristics. Programming and control of the device is conveniently enabled by on-board toggle switches. Alternately, programming and control can be accomplished through the on-board ribbon cable connector. This option allows software control which can aid in system development.

By making full use of the HSCF24040, the EB105 provides an analog input and output for both the RC and switched-capacitor filters. Both of these low-pass filters are fully programmable. Analog interfacing is accomplished with on-board BNC connectors to minimize noise and digital signal coupling. The EB105 also makes use of separate analog and digital supply grounds to further minimize digital coupling.

A clock crystal is supplied on the board which utilizes the HSCF24040 crystal oscillator feature. An external time base can be used optionally. BNC connectors are provided for external clock input and clock output for the CONVERT output and the SYNC control line. Use of BNC connectors on these active digital lines assures a minimum of digital-to-analog coupling.

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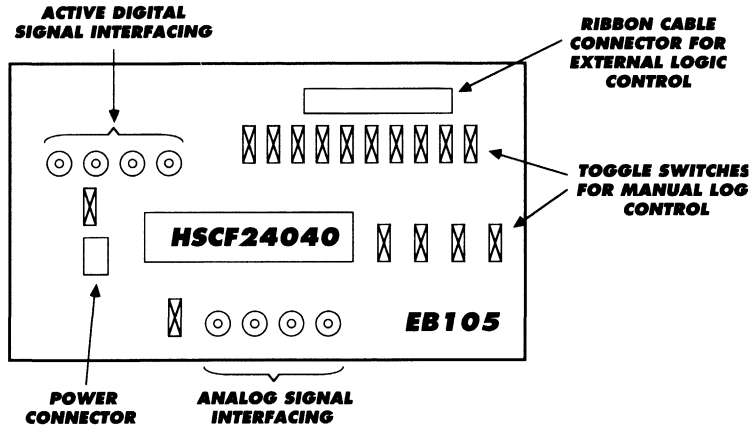

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SIGNAL PROCESSING TECHNOLOGIES

EB1175
EVALUATION BOARD

PRELIMINARY INFORMATION

FEATURES

- 40 MSPS Conversion Rate
- On-Board Reference Driver Circuit
- Analog Input Buffer
- Clock Input/Clock Divider Circuit
- On-Board Reconstruction DAC

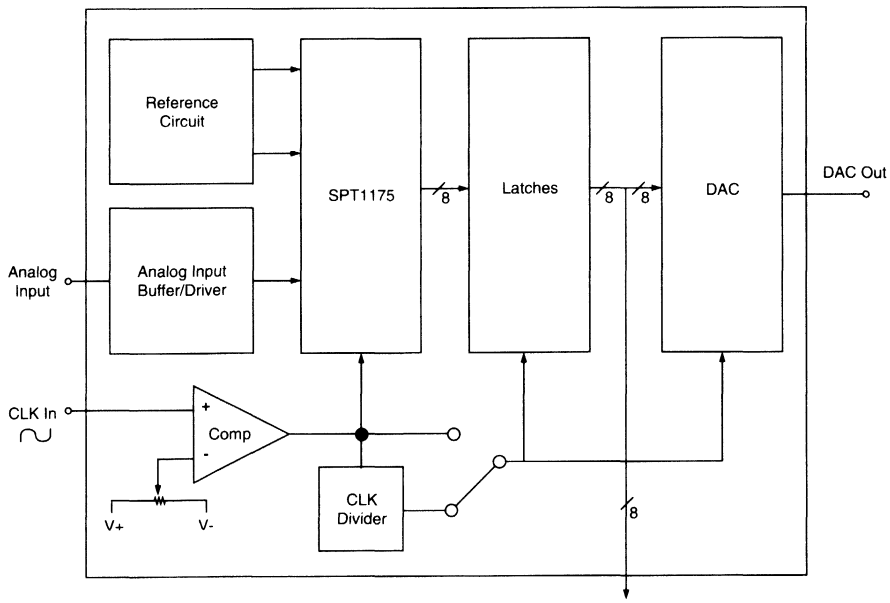
APPLICATIONS

- Evaluation of SPT1175, 8-Bit, 40 MSPS ADC
- Engineering System Prototype Aid
- Incoming Inspection Tool
- AC and DC Accuracy Testing
- Guide for System Layout

GENERAL DESCRIPTION

The EB1175 evaluation board is intended to demonstrate the performance of the SPT1175, 8-bit, 40 MSPS analog-to-digital converter (ADC). The on-board clock divider circuit provides the user more flexibility in capturing data in the output latches and reconstructing through the on-board DAC.

BLOCK DIAGRAM



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SIGNAL PROCESSING TECHNOLOGIES

EB7710/25 EVALUATION BOARD

FEATURES

- 150 and 250 MSPS Conversion Rates
- On-Board Reconstruction DAC
- Analog Input Buffer
- Flexible Clock Input That Accepts a Variety of Signal Generators
- Clock Divider Circuit

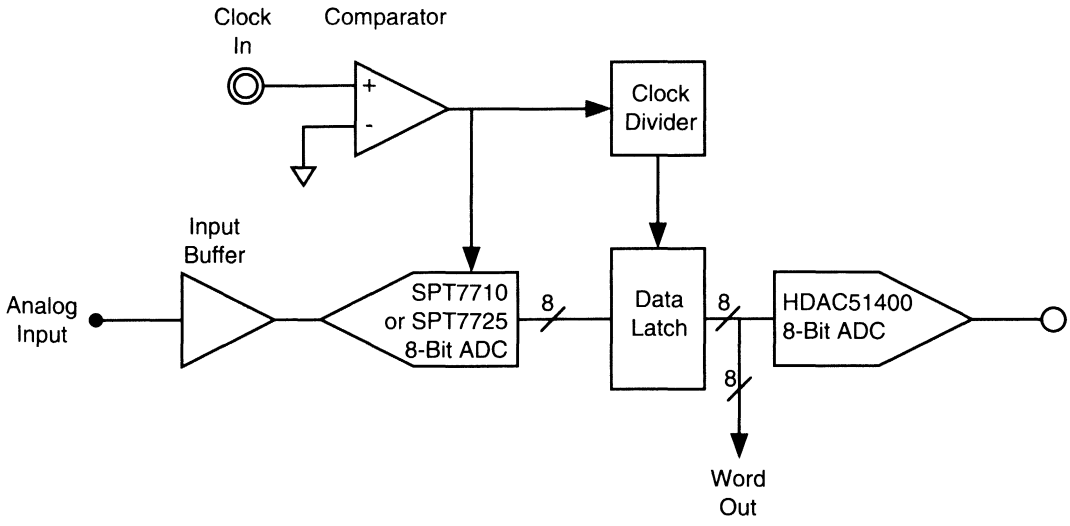
APPLICATIONS

- Evaluation of SPT7710 and SPT7725 ADCs
- Engineering System Prototype Aid
- Incoming Inspection Tool
- Guide for System Layout

GENERAL DESCRIPTION

The EB7710/25 evaluation board is intended to show the performance of the SPT7710 and SPT7725 8-bit, flash analog-to-digital converters (ADCs). The SPT7710 is capable of digitizing an analog input signal into 8-bit words at a minimum of 150 MSPS. The SPT7725 is capable of digitizing an analog input signal into 8-bit words at a minimum of 250 MSPS. For most applications, no external THA is required for accurate conversion due to the device's wide large-signal bandwidth.

BLOCK DIAGRAM



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SIGNAL PROCESSING TECHNOLOGIES

EB7750 EVALUATION BOARD

PRELIMINARY INFORMATION

FEATURES

- Reference Driver Circuits
- Analog Input Buffer/Driver
- Clock Driver Circuit
- Output Data Latches
- Reconstruction DAC

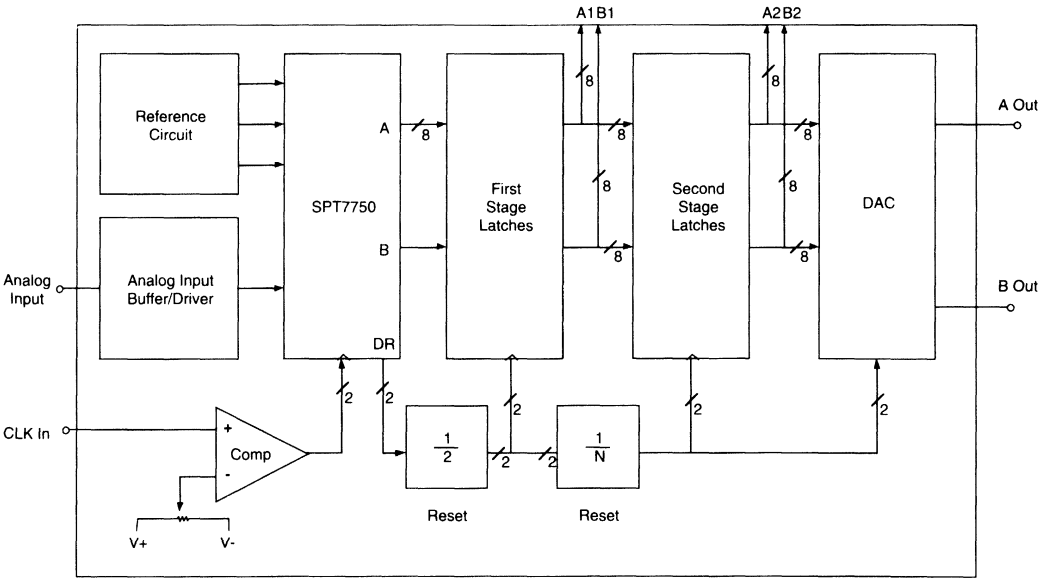
APPLICATIONS

- Engineering System Prototype Aid
- Incoming Inspection Tool
- AC and DC Linearity Testing
- Guide for System Layout

GENERAL DESCRIPTION

The EB7750 evaluation board is intended to demonstrate the performance of the SPT7750, 8-bit, 500 MSPS ADC. The two stages of output data latches and data ready reset circuits simplify the capture of the demuxed output data.

BLOCK DIAGRAM



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SIGNAL PROCESSING TECHNOLOGIES

EB7810/14 EVALUATION BOARD

FEATURES

- 20 and 40 MSPS Conversion Rates
- On-Board Reconstruction DAC
- Differential Clock Driver
- Data Output and Strobe Signal - ECL
- Data Output and Strobe Signal - TTL
- User Selectable Capture Clock
- On-Board Reference Drivers
- On-Board Power Supplies for SPT7810/14

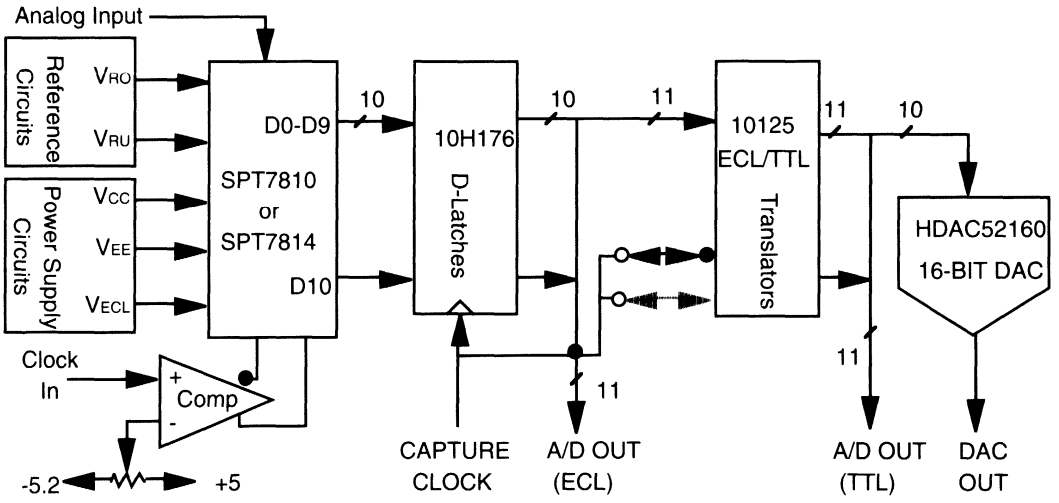
APPLICATIONS

- Evaluation of SPT7810 and SPT7814, 10-Bit ADCs
- Engineering System Prototype Aid
- Incoming Inspection Tool
- AC Accuracy Testing: SNR, THD
- DC Accuracy Testing: ILE, DLE
- Power Supply Sensitivity Testing
- Guide for System Layout

GENERAL DESCRIPTION

The EB7810/14 evaluation board is intended to demonstrate the performance of the SPT7810 and SPT7814, monolithic high speed analog-to-digital converters (ADCs). The SPT7810 is capable of digitizing a ±2 V analog input signal into 10-bit words at a minimum of 20 MSPS update rate, while the SPT7814 is capable of digitizing at a minimum of 40 MSPS update rate.

BLOCK DIAGRAM



The EB7810/14 consists of the following separate sections:

- Reference circuits
- Power supply circuits
- SPT7810 or SPT7814, 10-bit ADC (not included)
- Clock driver circuit
- Output ECL data latches available through 26-pin female ribbon connector
- ECL-to-TTL output translators available through 26-pin female ribbon connector

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SIGNAL PROCESSING TECHNOLOGIES

EB7820/24 EVALUATION BOARD

FEATURES

- 20 and 40 MSPS Conversion Rates
- On-Board Reconstruction DAC
- On-Board Reference Drivers
- On-Board Power Supplies to SPT7820/24
- Data Output - TTL
- User Selectable Capture Clock
- Improved Output Drive (Doubly-Terminated 50 Ω)

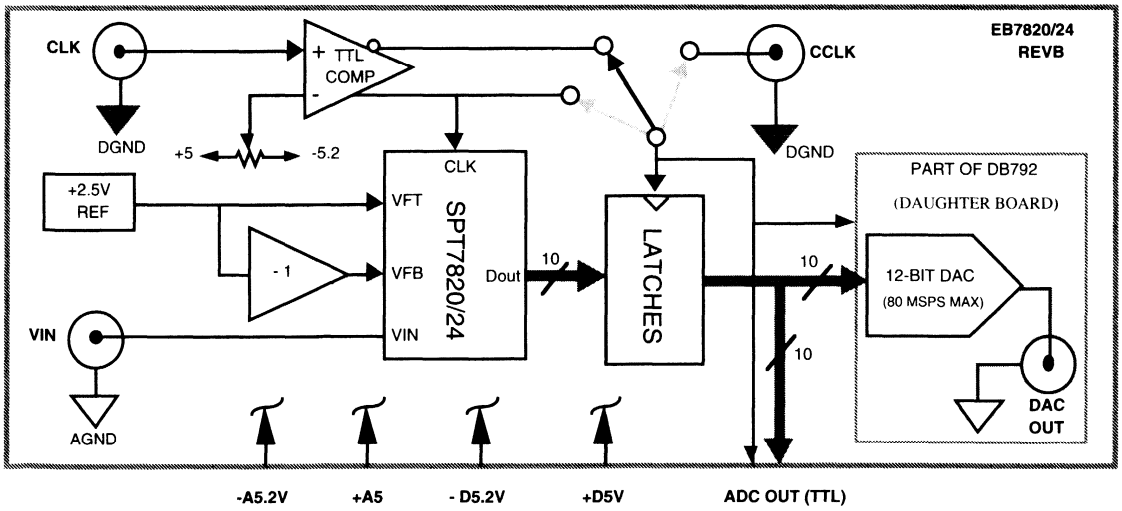
APPLICATIONS

- Evaluation of SPT7820 and SPT7824
- Engineering System Prototype Aid
- Incoming Inspection Tool
- Differential Linearity Error (DLE) Testing
- Integral Linearity Error (ILE) Testing
- AC Accuracy Testing: SNR, THD
- Power Supply Sensitivity Testing
- Guide for System Layout

GENERAL DESCRIPTION

The EB7820/24 Evaluation Board is intended to demonstrate the performance of the SPT7820 and SPT7824, monolithic, high-speed, analog-to-digital converters. Both the SPT7820 and SPT7824 have analog input ranges of ±2 V. The SPT7820 is capable of digitizing an analog input signal into 10-bit words at a minimum update rate of 20 MSPS, while the SPT7824 is capable of digitizing an analog input signal into 10-bit words at a minimum update rate of 40 MSPS.

BLOCK DIAGRAM



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EB7840/50/60 EVALUATION BOARD

PRELIMINARY INFORMATION

FEATURES

- 10, 20 and 40 MSPS Conversion Rates
- On-Board Reconstruction DAC
- Clock Driver Circuit
- Data Output Latch
- On-Board Reference Circuits

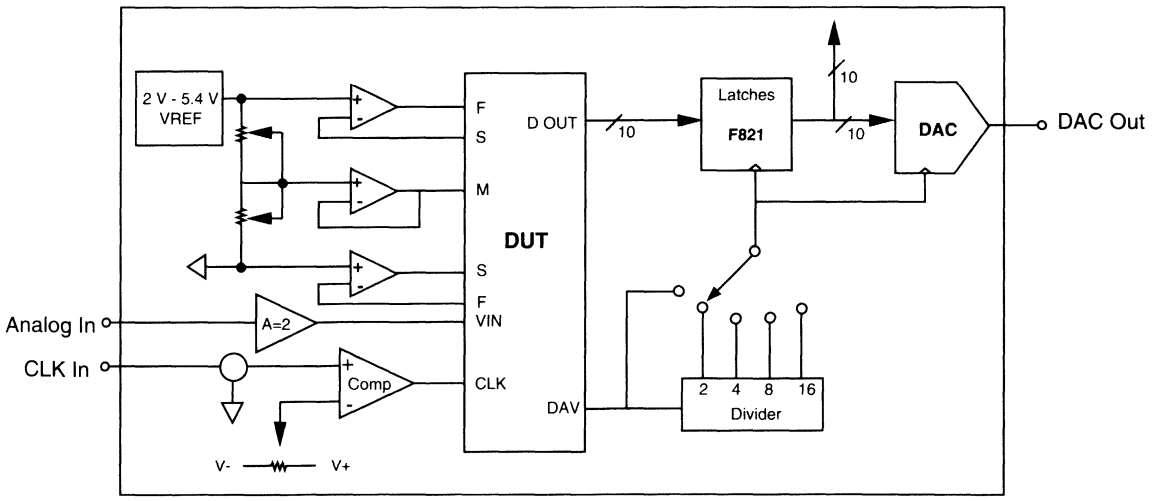
APPLICATIONS

- Evaluation of SPT7840/50/60 10-Bit ADCs
- Engineering System Prototype Aid
- Incoming Inspection Tool
- Guide for System Layout

GENERAL DESCRIPTION

The EB7840/50/60 evaluation board is intended to demonstrate the performance of the SPT7840 (10 MSPS ADC), the SPT7850 (20 MSPS ADC) and the SPT7860 (40 MSPS ADC). The board is interchangeable with adjustments to the clock circuit required to test each device.

BLOCK DIAGRAM



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SIGNAL PROCESSING TECHNOLOGIES

EB791
EVALUATION BOARD

PRELIMINARY INFORMATION

FEATURES

- 30 MSPS Conversion Rate
- On-Board Reference
- ECL Data Output
- Data Ready Output
- On-Board Track-and-Hold Amp
- 60 dB SNR at 15 MHz f_{IN}

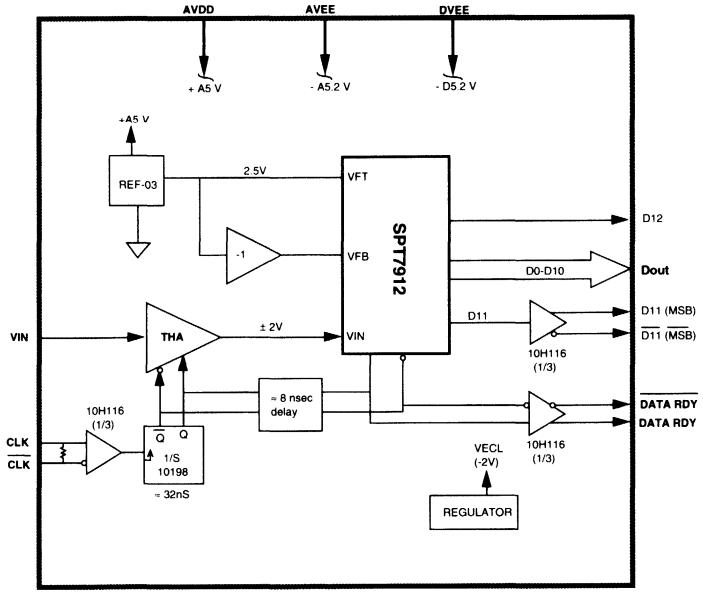
APPLICATIONS

- Evaluation of SPT7912 With External THA
- Guide for System Layout
- Engineering System Prototype Aid for Applications Such As:
  - Digital Storage Oscilloscopes
  - Radar
  - Electronic Warfare
  - Medical Imaging

GENERAL DESCRIPTION

The EB791 is a 3.0" by 3.5" 32-pin circuit board used to evaluate the performance of the SPT7912 using an external THA for applications requiring improved performance at higher input bandwidths. The board is capable of digitizing analog input signals up to 15 MHz into 12-bit words at update rates of 30 MSPS. The board is shipped complete with the SPT7912 and all supporting devices shown in the block diagram. The board dissipates 4.85 W typical.

BLOCK DIAGRAM



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SIGNAL PROCESSING TECHNOLOGIES

EB7910/12 EVALUATION BOARD

FEATURES

- 10 and 30 MSPS Conversion Rates
- On-Board Reconstruction DAC
- Differential Clock Driver
- Data Output and Strobe Signal - ECL
- Data Output and Strobe Signal - TTL
- User Selectable Capture Clock
- On-Board Reference Drivers
- On-Board Power Supplies for SPT7910/12

APPLICATIONS

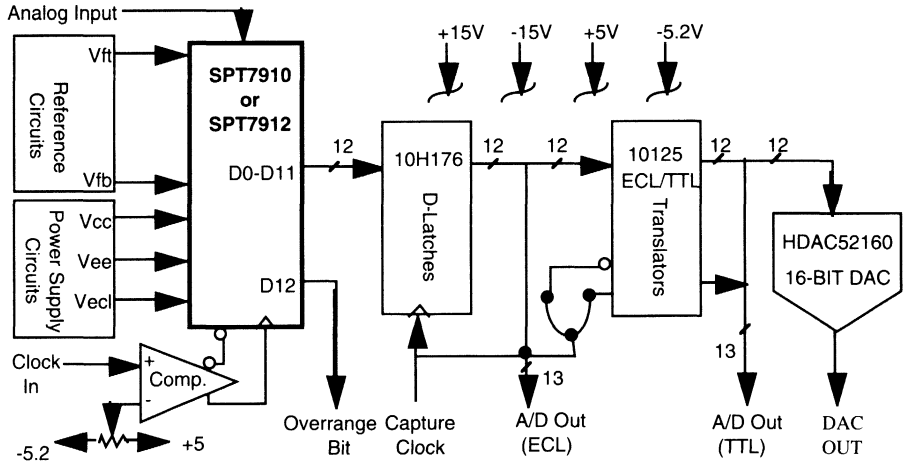
- Evaluation of SPT7910 and SPT7912
- Engineering System Prototype Aid
- Incoming Inspection Tool
- Differential Linearity Error (DLE) Testing
- Integral Linearity Error (ILE) Testing
- AC Accuracy Testing: SNR, THD
- Power Supply Sensitivity Testing
- Guide for System Layout

GENERAL DESCRIPTION

The EB7910/12 evaluation board is intended to demonstrate the performance of the SPT7910 and SPT7912, monolithic high speed analog-to-digital converters (ADCs). Both the SPT7910 and SPT7912 have an analog input range of ±2 V.

The SPT7910 is capable of digitizing an analog input signal into 12-bit words at a minimum of 10 MSPS update rate, while the SPT7912 is capable of digitizing an analog input signal into 12-bit words at a minimum of 30 MSPS update rate.

BLOCK DIAGRAM



The EB7910/12 consists of seven separate sections:

- Reference circuits
- Power supply circuits
- SPT7910 or SPT7912, 12-bit ADC (not included)
- Clock driver circuit
- Output ECL data latches available through 26-pin female ribbon connector
- ECL-to-TTL output translators available through 26-pin female ribbon connector
- DAC reconstruction

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SIGNAL PROCESSING TECHNOLOGIES

EB7920/22 EVALUATION BOARD

FEATURES

- 10 and 30 MSPS Conversion Rates
- On-Board Reconstruction DAC
- On-Board Reference Drivers
- On-Board Power Supplies to SPT7920/22
- Data Output - TTL
- User Selectable Capture Clock
- Improved Output Drive (Doubly-Terminated 50 Ω)

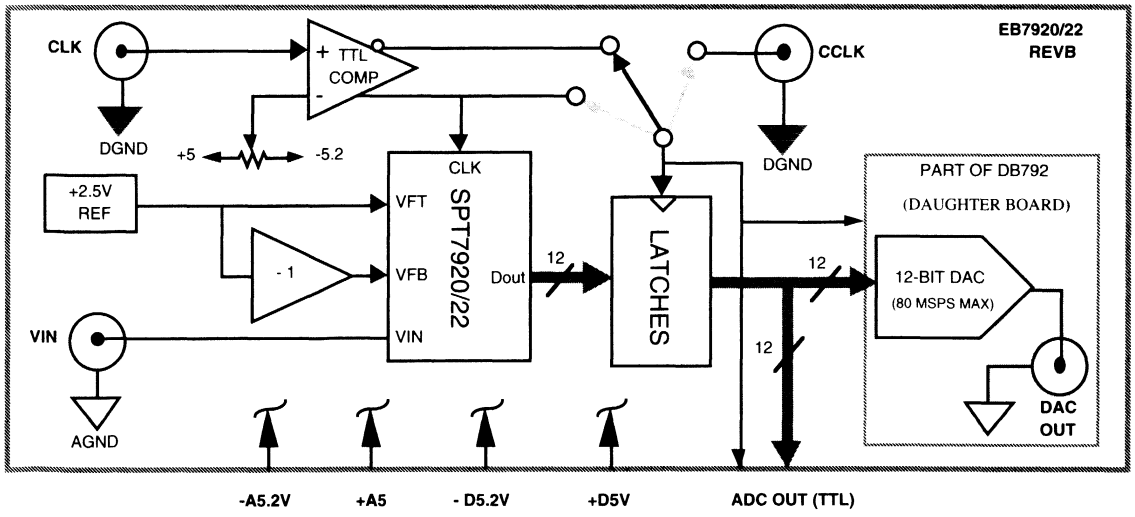
APPLICATIONS

- Evaluation of SPT7920 and SPT7922
- Engineering System Prototype Aid
- Incoming Inspection Tool
- Differential Linearity Error (DLE) Testing
- Integral Linearity Error (ILE) Testing
- AC Accuracy Testing: SNR, THD
- Power Supply Sensitivity Testing
- Guide for System Layout

GENERAL DESCRIPTION

The EB7920/22 Evaluation Board is intended to demonstrate the performance of the SPT7920 and SPT7922, monolithic, high-speed, analog-to-digital converters. Both the SPT7920 and SPT7922 have analog input ranges of ±2 V. The SPT7920 is capable of digitizing an analog input signal into 10-bit words at a minimum update rate of 10 MSPS, while the SPT7922 is capable of digitizing an analog input signal into 10-bit words at a minimum update rate of 30 MSPS.

BLOCK DIAGRAM



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SPT
SIGNAL PROCESSING TECHNOLOGIES

APPLICATION NOTES & BRIEFS

CONTACT SPT FOR COMPLETE COPIES OF THE FOLLOWING APPLICATION NOTES.

AN104
VIDEO DACS AND RASTER GRAPHICS

AN104 explains high-speed DACS and how they are used in CRT designs and raster graphics systems. This application note describes video DAC performance parameters including speed, rise time, glitch energy, resolution, logic compatibility, and analog output drive. A block diagram and associated graphs are included to clearly illustrate raster scan graphics systems.

AN106
EB104 EVALUATION BOARD

The EB104 is used to demonstrate performance of the HADC574Z/674Z, and SPT774A 12-bit ADC products. The low noise environment provided by the board makes 12-bit resolution easier to achieve compared to most lab breadboarding. Features include buffered A/D and D/A conversion data buses, S/H amp and output op-amp ICs, and unipolar or bipolar operation. It is shipped fully assembled and tested.

AN108
THERMAL CONSIDERATIONS FOR HIGH-PERFORMANCE DEVICES

AN108 is a general overview of the integrated circuit package and its interface to the outside world. Information on system thermodynamics, calculating the operating die temperature, package thermal resistance, and heat sinking is included. Thermal resistances of concern to system designers are also discussed.

AN109
EB105 EVALUATION BOARD

The EB105 evaluation board provides for the full demonstration and evaluation of the HSCF24040 programmable 7th order low-pass active filter. Programming and control of the device are enabled by on-board toggle switches. The board provides a ground planed, high performance, noise free environment for testing of the device. It is shipped fully assembled and tested with one HSCF24040.

AN7810/14
EB7810/14 EVALUATION BOARD

The EB7810/14 evaluation board is used to demonstrate the performance of the SPT7810 and the SPT7814. Features include reference inputs, clock driver circuit, on-board reconstruction DAC, data output and strobe signals for ECL and TTL, user-selectable capture clock, and conversion rates up to 40 MSPS. It includes detailed discussions of power supplies, grounding, voltage references, clock driver, output data latches, timing, DAC reconstruction, selection of signal generators, and product characterization. Board calibration, accuracy testing and dynamic testing are explained in detail. The board can be used for system prototypes, incoming inspection, testing of IL and DL, AC accuracy testing, and power supply sensitivity testing. The board is calibrated and tested before shipment. The ADC device is not included with the board.

AN7820/24
EB7820/24 EVALUATION BOARD

The complete application note for the AN7820/24 is included later in this section.

AN7910/12
EB7910/12 EVALUATION BOARD

The EB7910/12 evaluation board is used to demonstrate the performance of the SPT7910 and the SPT7912. Features include on-board reference drivers, on-board reconstruction DAC, data output and strobe signals for ECL and TTL, user selectable capture clock, and conversion rates up to 30 MSPS. It includes detailed discussions of power supplies, grounding, voltage references, clock driver, output data latches, timing, DAC reconstruction, selection of signal generators, and product characterization. Board calibration, accuracy testing and dynamic testing are explained in detail. The board can be used for system prototypes, incoming inspection, testing of IL and DL, AC accuracy testing, power supply sensitivity testing and as a guide for system layout. The board is calibrated and tested before shipment. The ADC device is not included with the board.

AN7920/22
EB7920/22 EVALUATION BOARD

The complete application note for the AN7920/22 is included later in this section.

AN7840/50/60
EB7840/50/60 EVALUATION BOARD

The EB7840/50/60 evaluation board is used to demonstrate the performance of the SPT7840, SPT7850, and SPT7860, 10-bit ADCs. Features include 10, 20 and 40 MSPS conversion rates, on-board reference driver circuits, and a reconstruction DAC. Detailed discussions on grounding, references, timing, and product characterization are included. The board is shipped calibrated and tested. The ADC device is not included with the board.

AN1175
EB1175 EVALUATION BOARD

The EB1175 evaluation board is used to demonstrate the performance of the SPT1175, 8-bit, 40 MSPS A/D converter. Features include 40 MSPS conversion rate, on-board reference driver circuits, and a reconstruction DAC. Detailed discussions on grounding, references, timing, and product characterization are included. The board is shipped calibrated and tested. The ADC device is not included with the board.

AN7710/25
EB7710/25 EVALUATION BOARD

The EB7710/25 evaluation board is used to demonstrate the performance of the SPT7710 and SPT7725, 8-bit 150 and 250 MSPS A/D converters. Features include 150 and 250 MSPS conversion rates, on-board reference driver circuits, and a reconstruction DAC. Detailed discussions on timing and product characterization are included. The board is shipped calibrated and tested. The ADC device is not included with the board.

AN7750
EB7750 EVALUATION BOARD

The EB7750 evaluation board is used to demonstrate the performance of the SPT7750, 8-bit 500 MSPS A/D converter. Features include 500 MSPS conversion rate, on-board reference driver circuits, timing circuits and two latches to capture each of the demuxed outputs. Discussions on timing and product characterization are included. The SPT7750 device is not included with the board.

AN791
EB791 EVALUATION BOARD

The EB791 evaluation board is used to demonstrate the performance of the SPT7912, 12-bit 30 MSPS, ECL A/D converter with an external track-and-hold amplifier. The board is 3.5" by 3.0", 32-pin, and dissipates 4.85 W typ. Input signals up to 15 MHz can be digitized with an SNR of 61 dB. The board includes an SPT7912 device and is shipped calibrated and tested.

AN111
ANALOG/DIGITAL INTERFACE REQUIREMENTS FOR THE HSCF24040

This application note describes the internal workings of the HSCF24040 to assist the user in system design. It includes specific information on analog and digital interface requirements and how to choose proper SC and RC filter bandwidths. It is an excellent tool for understanding switched-cap basics and system design.

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AB100
USING ECL DACS WITH TTL LOGIC

This application brief describes why most high-speed DACs are designed to perform in ECL systems due to the speed and low noise characteristics of this logic group. It gives specific information on methods for using SPT's ECL DACs in TTL systems. Solutions for overcoming incompatibility between -5.2 V and +5 V systems are included.

AB102
CHARGE SCALING DATA CONVERTERS

Current scaling versus charge scaling data conversion techniques are discussed in this application note. SPT's BiCMOS process used to manufacture the HADC574Z, HADC674Z, and SPT774 uses this technique to lower power consumption and provide an inherent S/H function. A simple explanation of how this is performed is included.

AB103
HADC574Z/674Z AND SPT774 ANALOG INPUT STRUCTURE

This application brief describes the BiCMOS process and design architecture of the input circuits of the HADC574Z/674Z and the SPT774 and how the architecture reduces the need for specific signal source characteristics and signal buffering. Included is a brief discussion of conversion events and DC dynamic input characteristics of the device and how the input structure improves the overall performance of the ADC.

AB104
TESTING THE HADC574Z/674Z AND THE SPT774 ON THE LTS2020

This application brief provides technical information on the LTS2020 test system commonly used as an incoming inspection tool. Hardware and software modifications to achieve accurate test results for the HADC574Z/674Z and SPT774 are explained.

AB105
GLITCH ENERGY IN HIGH-SPEED D/A CONVERTERS

This brief provides a brief explanation of how glitch energy affects some applications, how to overcome these problems, and why SPT's devices have superior glitch performance. Included is specific information on SPT's DAC designs and information on defining glitch energy.

LEADERSHIP IN DATA CONVERSION AND SIGNAL PROCESSING

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SIGNAL PROCESSING TECHNOLOGIES

AN7820/24

EVALUATION BOARD APPLICATION NOTE

FEATURES

- 20 and 40 MSPS Conversion Rate
- On-Board Clock Drivers
- Data Output and Strobe Signal
- User Selectable Capture Clock
- On-Board Reference Drivers
- Dimension : ≈ 4.0" X 7.5"

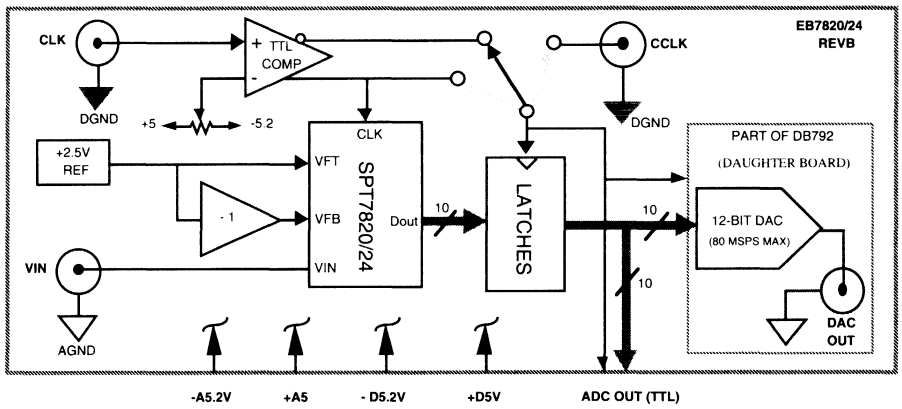
APPLICATIONS

- Evaluation of SPT7820 and SPT7824
- Engineering System Prototype Aid
- Incoming Inspection Tool
- Differential Linearity Error (DLE) Testing
- Integral Linearity Error (ILE) Testing
- AC Accuracy Testing: SNR, THD
- Guide for System Layout

GENERAL DESCRIPTION

The EB7820/24 Evaluation Board is intended to demonstrate the performance of the SPT7820 and SPT7824, monolithic high speed analog to digital converters (ADC). This document is also to be used as an application note and as supplemental information to the existing data sheets (SPT7820 or SPT7824). Both the SPT7820 and SPT7824 have an analog input range of ±2 V. The SPT7820 is capable of digitizing an analog input signal into 10-bit words at a minimum of 20 MSPS update rate, while the SPT7824 is capable of digitizing an analog input signal into 10-bit words at a minimum of 40 MSPS update rate. Both devices are pin compatible. All input/output logic is TTL compatible.

Figure 1: EB7820/24 Block Diagram. (The full detail schematic is shown in figure 17.)



The EB7820/24 (≈ 4" X 7.56") consists of five separate sections:

- Reference circuits
- Clock circuits
- SPT7820 or SPT7824, 10-bit ADC (Not Included With Board)
- Output latches available through 26-pin female ribbon connector
- DAC reconstruction board, DB792, a separate daughter board (≈ 2.5" X 3.0") directly interfaces with the EB7820/24

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Figure 10: Driving Circuit Block Diagram

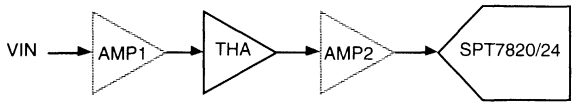

Figure 10 shows the typical analog driving circuit. AMP1 or AMP2 are optional. For an application where noise is the major concern, use AMP1 (disregard AMP2) low noise amplifier to gain up to ± 2 volts before getting to the THA. In another application where high frequency VIN is the major concern, use AMP2 instead of AMP1 to amplify the THA signal to ±2 volts before reaching to SPT7820 or SPT7824. In the latter case, the low level VIN provides a faster acquisition time for the THA.

UNCOMMITTED PROTO SOCKET SPACE

Referring to the detail schematic Figure 17, there are two slots available for applications where additional circuits may be needed in order to interface with the EB7820/24. These two slots (labeled A & D in the PCB assembly) are electrically noncommitted:

- Slot A is physically located near VIN (BNC) and is intended for the analog interfacing circuit. It has one 16-DIP and one 8-SIP.

- Slot D is physically located between P2 and P3 (connectors) and is intended for the digital interfacing circuit. It has three 16-DIPs, three 8-SIPs and one 37-pin D connector.

  Both slots have the appropriate power supplies and grounds in their vicinity as labeled.

DB792 DAUGHTER BOARD (RECONSTRUCTION DAC)

DB792 (figure 18) is the daughter board that interfaces directly to the EB7820/24 via P2 and P3. It is suited for an application where the reconstruction DAC is needed to evaluate the ADC performance in the time domain. EB792 is designed around the Analog Device's AD9713, 12 bit TTL digital-to-analog converter, 80 MSPS update rate. It is set-up in bipolar operation. The detailed schematic is shown in figure 18. Refer to the Analog Device AD9713B data sheet for detail.

SPT7820/24 INPUT AND LATCH-UP PROTECTIONS

The SPT7820/24 is free from any possible latch-up when following the recommended interfacing circuit as shown in figure 11. The following lists are for both latch-up and input protection interface requirements:

1) The input clock (pin 15) must be driven from a TTL logic (VIH ≤ 4.5 V). Fast TTL logic family or equivalent is strongly recommended due to its fast rise time (6 nsec or faster). In the event where the clock is driven from a high current source (greater than 400 mA), use a 100 Ω resistor in series to current limit to roughly 45 mA.

2) D1 is a Schottky or hot carrier diode (Motorola, 1N5817 or equivalent) installed between VEE and AGND (reverse bias).

3) Both VCC (pin 18 & 25) and DVCC (pin 14 & 28) are driven from the same analog +5 V supply.

4) The ferrite beads (FB1 and FB2) are to be mounted as closely to the device as possible. The bead to ADC connections should not be shared with any other device.

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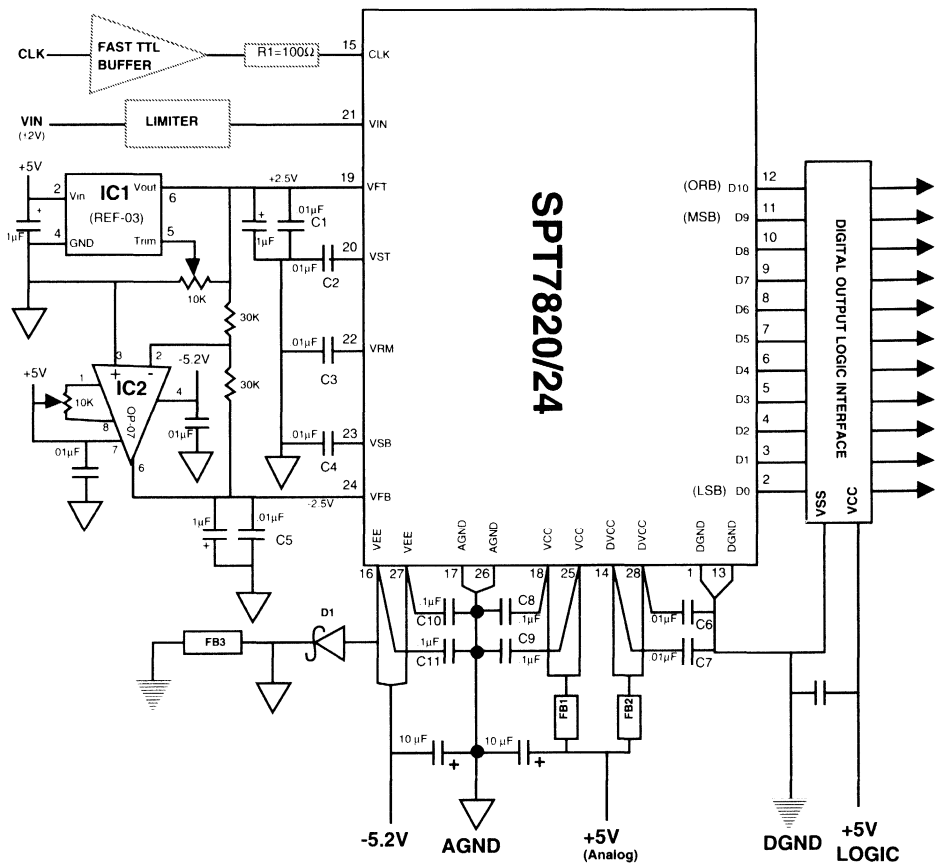
Figure 11: Recommended Interfacing Circuit

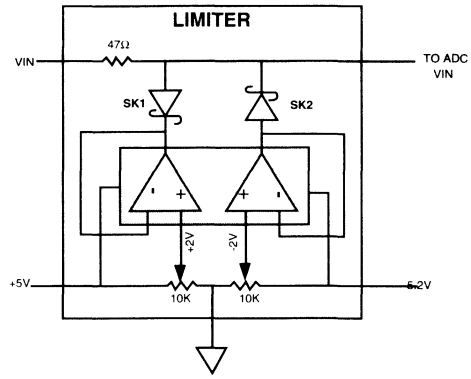


5) All reference and power supply pins must be bypassed as closely to the device pin as possible (chip caps C1-11 are preferred): 0.1 µF for VCC and VEE, and 0.01µF for DVCC and Vref.

6) The top reference (VFT) driver must be current limited to 20 mA maximum if a different reference driver circuit is used in place of the recommended circuit shown in figure 11.

7) The limiter is required if the maximum peak-to-peak voltage of the analog input exceeds ±2.5 V. Incorporate the limiter within the analog input driver or use the circuit shown in figure 12. Another option is to add a 100 Ω resistor in series to current limited the input. This last option adds another LSB error to both ± full scale compared to only 1/2 LSB when using the circuit shown in figure 12.

Figure 12 : An Example of an Input Limiter



SK1,2 = Fast recovery schottky diode:
RCA, P/N SK9091 or equivalent

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SPT7820/24 CHARACTERIZATION

The performance at speed is the main goal in evaluating any ADC, but it is beneficial to start from a relatively low speed and verify key parameters. It is also beneficial to at least predict performance at speed. If the transition noise and/or the differential linearity of the device perform poorly at low frequency, then the SNR at speed cannot be expected to be better. In addition, the low frequency set-up can be useful as a verification tool for the test set-up.

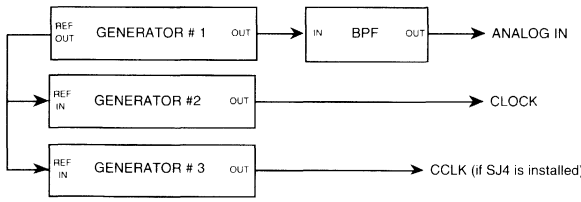
At low frequency there are numerous ways of characterizing the differential linearity error (DLE), integral linearity error (ILE), transition noise, missing codes (MC), synchronous noise, non-monotonicity, power supply sensitivity and power supply currents. SPT will guide the user through two classical yet powerful testing approaches to achieve fast and relatively accurate results.

High frequency or dynamic testing, the missing codes test, ILE, DLE, VOS and the gain error tests are based on statistical results. They can be performed using the *Histogram* technique. SNR and THD are tested by using the Fast Fourier Transform (FFT).

EB7820/24 was designed to provide optimum capability in fulfilling the above characterization needs.

EQUIPMENT HOOK-UP

Figure 13: Synchronous Equipment Hook-up



Coherent testing is recommended in characterizing the SPT7820/24. All three signals (VIN, CLK and CCLK) are synchronized. This testing gives well defined results when using the following suggested techniques for evaluating the performance of the device. These techniques will also significantly reduce the testing time, especially the dynamic testing. The diagram in Figure 13 suggests one way to achieve this goal. Generator #1 is the Analog input. Generator 2 is the sampling clock, sinewave and ±3 V P-P max. Generator #3 (only needed if you elect to use the solder jumper option SJ4) is the capture clock, TTL. A phase adjustment option for generator #3 is necessary to place the edge of the capture clock at the proper setup time. R11 and R12 are 51 Ω and serve as termination resistors for generator #2 and generator #3, respectively.

SELECTION OF THE SIGNAL GENERATORS

For very high speed and high accuracy ADC testing, selection of both analog and clock inputs is critical. Two parameters are important in selecting the generators #1 and #2:

1) The purity of the output sinewave must be at least 76 dB or better of SNR . An appropriate band pass filter (BPF) installed after the generator will help improve the SNR.
2) The sampling clock jitter or aperture jitter. This jitter can originate both inside and outside the A/D converter.

Consider the selection of an acceptable clock generator. The uncertainty of the clock placement due to the time jitter (aperture jitter) will degrade the effective performance of the device. This jitter is translated into the ADC amplitude error and is proportional to the analog input slew rate. For a sinusoidal input, the uncertainty of the clock edge placement from cycle to cycle due to the equipment jitter will have an effect on the A/D converter performance, especially the SNR:

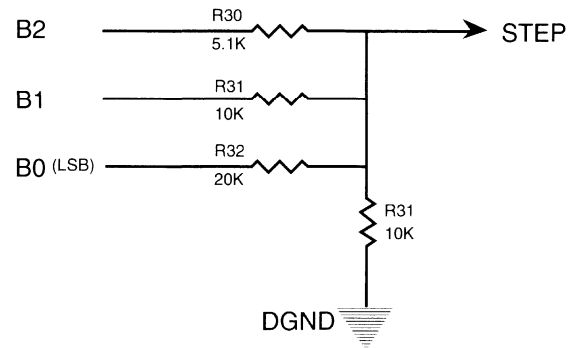
$$SNR\ (Max) = \{20\ LOG\ [1/(2\pi\ Fin\ Tj)] + 3.02\}\ dB,$$

Where : Fin = analog input frequency
and Tj = the aperture jitter in RMS

SPT uses the following equipment when characterizing / testing the SNR and THD: HP8644A synthesized signal generator for both generators 1 and 2 and HP3325 function generator for generator 3.

LOW FREQUENCY PERFORMANCE CHECK

Figure 14 : Three-bit Reconstruction DAC



This section is intended to suggest one approach to visual evaluation of the differential linearity error (DLE), missing codes (MC), non-monotonicity, synchronous noise and transition noise. The BNC DAC OUT (from the mother board, EB792, figure 18) can be the monitoring point to view the

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quality of the quantization signal, but this may pose a great deal of difficulty. SPT suggests another approach commonly used in the industry. This approach is to use a three bit reconstruction DAC generated from the last three LSB's TTL outputs. This circuit is shown in Figure 17: when the jumpers SJ9-SJ11 are installed, R30-R33 forms a three bit DAC as shown in Figure 14.

The output of this three bit reconstruction DAC could be viewed through the test point STEP with the scope. For this test, use a function generator for the generator #1 and #2 (HP3325A or equivalent) and set-up for a ramp output. Replace the BPF by an RC low pass filter (1K & 0.01 μF) to eliminate all high frequency components. The slew rate of this ramp signal should be set to 1 LSB per n conversions (sampling period) for a desired (1/n) test resolution. A minimum of n = 10 is recommended for this application. The P-P voltage and the period of the ramp input are then dependent on the selection of the number of steps (LSBs) within one ramp's period. Note that R10 (51Ω) may need to be removed. The CLK and CCLK are to be set to the same relatively low frequency, approximately 1 MHz or even slower. Adjustments are needed to meet the tpwH and ts specifications (see Figure 5-6 and Table 5).

The following formulas summarize the criteria for selecting the analog ramp input signal:

The ramp peak-to-peak voltage:
V(p-p) = m(FSR/1024)

The ramp period: T = (m) (n) / Fs Where:

m =	desired number of steps (LSBs) per ramp's period
Fs =	sampling frequency
FSR =	full scale range (typically SPT7820/24'sFSR is 4 V)
n =	desired test resolution or the number of conversions / LSB

Figure 15 shows the relationship between the analog input ramp signal and the resulting three-bit reconstruction DAC. It shows 16 LSBs of P-P input voltage (i.e., two 8-level steps) per period. For an ideal ADC and an ideal ramp input, its digital output code will change state by 1 LSB every (n)th conversion (dash line in the transfer curve). Any error in the ADC will make the corresponding output codes change their state before or after the (n)th conversion. This error will translate into smaller or larger respective step width. The DLE will be judged visually by comparing the actual step size with respect to the ideal step with ±(1/n)LSB of accuracy. In this case, the ideal step is the average of the step size. Other errors (MC, transition noise and non-monotonicity) can be resolved in a similar way. Figure 15 also gives the identification of each error from the actual transfer curve.

Example:

1) SPT7820 is operated at 500 kHz (sampling frequency)
2) (1/10) of the test resolution is desired
3) The scope is externally triggered to the ramp input. Three retraces of 8-level steps (or 24 total steps) per ramp's period are selected.

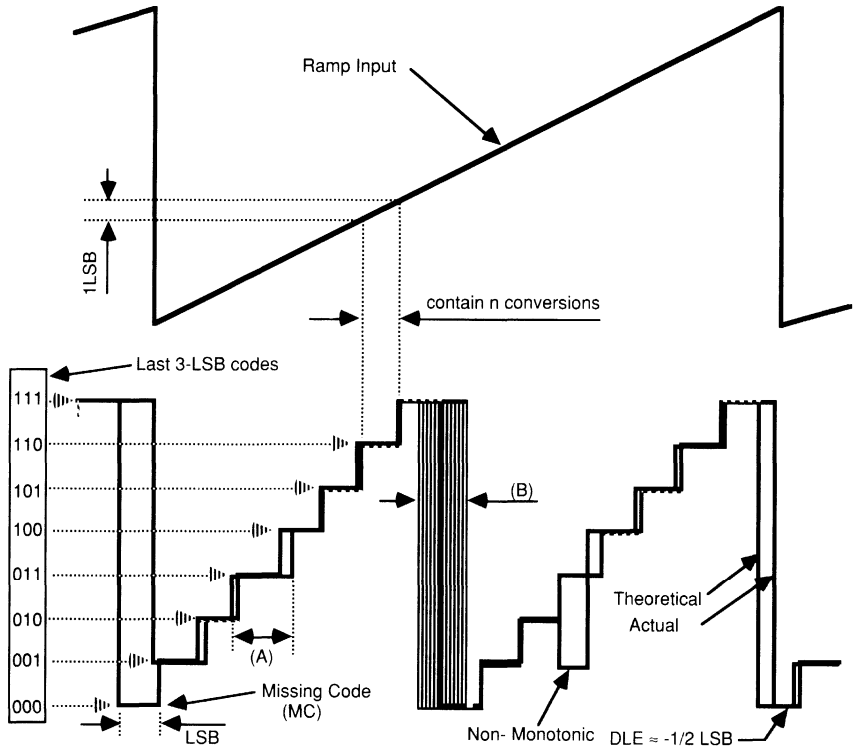
What peak-to-peak voltage (V p-p) and period (T) of the ramp input signal are required to drive the SPT7820?

Answer:
1) Fs = 500 kHz,
2) n = 10 ,
3) m = 24, then V(p-p) = m (FSR / 1024) = 24(4 /1024) = 94 mV
   and T = (m) (n) / Fs = (24) (10) / 5000,000 = 480 μsec

Noting the above input signal will only cover 24 parts in 1024 of the FSR. To identify all errors through the full scale range, sweep slowly the ramp input from -FS to +FS and observe the output steps for the MC, transition noise, DLE and non-monotonicity as indicated in the transfer curve (Figure 15). Most generators do not have the DC offset covering the range from +2.5 V to -2.5 V An additional circuit may need to be constructed using the classical summing amplifier to DC offset the above ramp input signal.

The synchronous noise in an ADC is the distortion of the performance of the device (normally, the DLE can be clearly observed) when the sampling frequency varies. This is usually caused by the digital signals being coupled back, internally, into the analog input signal. This problem is very common for ADCs using the successive approximation register (SAR) architecture. The ADC that possesses this kind of symptom will present some weak performances at a specific sampling frequency (within the specified sampling rate), but will show better results when the sampling frequency is varied up or down from that weak spot. To verify the synchronous noise using this set-up, slowly change the sampling frequency and observe the transfer curve, especially the changes in DLE.

Figure 15: Three-Bit Reconstruction DAC Waveform Using Analog Input Ramp



(A) is the actual bit weight for the output code multiple of 011
(B) is the major transition noise. This noise level shown is greater than ± 1/2 LSB

Advantages:

1) Many tests (as stated above) can be extracted from this one, simple test set-up.
2) The missing code and the transition noise can be accurately identified better than with any other standard test methods.
3) Quick set-up and relatively accurate.

Disadvantages:

1) The accuracy depends on human judgement and can be very difficult if not familiar.
2) The exact code is not shown in the transfer curve, but rather a multiple of the last three LSB's bits. To overcome this problem every bit must be probed using an oscilloscope, or install LEDs at each output , P3 connector, to signal the state of each output bit.

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DYNAMIC TESTING

Figure 16: Dynamic Testing Test Set-up

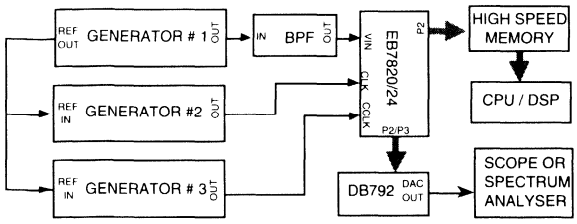

Figure 16 is the recommended block diagram suitable for dynamic testing of the SPT7820 or SPT7824 using the EB7820/24 evaluation board. In an earlier time, the DAC OUT signal had been used to analyze the ADC's dynamic performances (SNR and THD) through a spectrum analyzer. This method of testing presented some uncertainties. The DAC must be near perfect, free from glitches, and its dynamic accuracy (DLE and ILE) must be far better than the ADC under test. Any errors in the DAC would be added to the total SNR and/or THD.

Today, it is preferable to perform these tests by means of digital signal processing (DSP). Presently, there are numerous standard software packages on the market to service this application. The EB7820/24 provides the data outputs through P2 (see Table 5 for detail). The reconstruction DAC could be obtained from DB792 daughter board. Both set-ups are very important in characterizing the dynamic performance of the SPT7820 or SPT7824.

In many cases, the speed of the capture memory is much slower than the available output valid data of the ADC under test. If this is the case, it is necessary to decimate the capture clock at a rate of Fs / N, where N is a power of 2. The beat frequency can be achieved by slightly changing the analog input frequency by an amount of Δfin. For a 4096-point FFT, the beat frequency of Δfin = Fc / 4096 would be added (or subtracted) to the analog input frequency. 4096 data points will be filled in one test period, where the input is at Fin $\pm$ (Fc/4096) and the output is updated at 1/Fc interval. The selection of Fin is suggested to be the multiple (integer) of Fc to achieve a complete system synchronization. Both capture memory and the DAC will run at a relatively low update rate (Fs / N).

The daughter board DB972 is capable of updating up to 80 MSPS.

EB7820/24 CALIBRATION

This section will serve as a guide for the DC calibration of the EB7820/24 if needed. Note that this board was fully calibrated before the shipment. For every new SPT7820 or SPT7824, VST and VSB voltages require new calibration.

Check for the following jumpers installation: SJ2B, SJ2C and SJ3.

1.0 Equipment Needed
1.1 4 DC power supplies: analog +5 V, analog -5.2 V, digital +5 V and digital -5.2 V.
1.2 1 Hewlett Packard, HP3325A, function generators or equivalent
1.3 1 DVM with 5&1/2 digit precision
1.4 1 Oscilloscope

2.0 Equipment Set-Up / Hook-Up
2.1 No SPT7820 or SPT7824 in U1 socket at this point
2.2 Connect all 4 power supplies as shown in table 1, figure 2 and figure 3
2.3 Connect the function generator to CLK BNC
2.4 Set the CLK to 3 MHz, sine wave , $\pm$2 V
2.5 Connect VIN to AGND

3.0 References Calibration
3.1 Monitor TP1 with respect to AGND test point with DVM
3.2 Adjust R1 for +2.500 V at TP1
3.3 Monitor TP2 with respect to AGND test point with DVM
3.4 Adjust R2 for -2.500 V at TP2
3.5 Turn all power to off
3.6 Install SPT7820 or SPT7824 into U1 socket (repeat from this procedure for all new devices)
3.7 Turn all powers back to on
3.8 Monitor U1, pin 22 (VST) with respect to AGND test point with DVM
3.9 Adjust R1 for +2.000 V at VST
3.10 Monitor U1, pin 27 (VSB) with respect to AGND test point with DVM
3.11 Adjust R2 for -2.000 V at VSB
3.12 Repeat procedure from paragraph 3.8 until VST and VSB reach the desired voltages ($\pm$2.000 V respectively)

4.0 Clock Circuit Calibration
4.1 Monitor PJ1 with scope on channel 1 (Externally sync to the generator)
4.2 Observe the TTL clock and adjust R3 for approximately 50 % of duty cycle

5.0 Latches (U7 & U8) Test
5.1 Remove R10
5.2 Connect VIN to TP1
5.3 Monitor P2, odd number pins (7-25) with scope and observe TTL logic high on all pins
5.4 Connect VIN to TP2
5.5 Monitor P2, odd number pins (7-25) with scope and observe TTL logic low on all pins

End of calibration Procedure

EB7820/24 PARTS LIST, Rev B

#	Ref. Des.	Description	Vendor Part Number	Qty
1	C1-7,10	Capacitor, Tant., 10µF, 25V, .10"	Sprague / 199D106X0025B A 1, or eq.	8
2	C20,22-28,30-32	Capacitor, 0.01µF, Chip	Sprague / 11C1206X7R103J050AB, or eq.	11
3	C21,29	Capacitor, 0.1µF, Chip	Sprague / 11C1206X7R104J050AB, or eq.	2
4	C50-58	Capacitor, 0.01µF,10%, Ceramic	MURATA / RPE110X7R103K050V or eq.	9
5	D1	Lead Mounted Hot carrier Rectifier	MOT / IN5817, or eq.	1
6	FB1-3	Ferrite bead, Lead Mounted	Fair Rite / 2743001111	3
7	P2,3	Ribbon Plug Connector	T & B Ansley / 622-2627, or eq.	2
8	P1	Power Connector, 9 Pins	Molex / 09-18-5094, or eq.	1
9	P1/Recept	Power Connector, 9 Pins, Recept	Molex / 03-09-1093, or eq	1
10	PJ1-2	Probe Connector (25 sets/bag)	Tektronix / 131-4353-00	2
11	R3	Potentiometer, 2K , 12 Turns	Bourns / 44F3531, or eq.	1
12	R1,2	Potentiometer, 10K , 12 Turns	Bourns / 44F3533, or eq.	2
13	R10-12	Resistor, 51 Ω, 5%, 1/8 W	Allen-Bradley / BB-510-5, or eq.	3
14	R20,21	Resistor, 820 Ω, 5%, 1/8 W	Allen-Bradley / BB-821-5, or eq.	2
15	R26,27,30	Resistor, 20K, 5%, 1/8 W	Allen-Bradley / BB-203-5, or eq.	3
16	R28	Resistor, 1M, 5%, 1/8 W	Allen-Bradley / BB-105-5, or eq.	1
17	R32	Resistor, 5.1K, 5%, 1/8 W	Allen-Bradley / BB-512-5, or eq	1
18	R33	Resistor, 10K, 5%, 1/8 W	Allen-Bradley / BB-103-5 , or eq.	1
19	RN1,2	8 pin SIP Resistor, 10K, 708A type	Newark stock 81F9599, or eq.	2
20	TP1-3,AG,DG,STEP	Test Point Terminal. 76 mil hole dia	Cambion / 160-2044—02-01-00, or eq.	6
21	U1	Device Under test, 10 Bit ADC	SPT7820 or SPT7824	1
22	U2	+2.5V Precision Voltage Reference	PMI/REF-03GP, or eq.	1
23	U3	OP-AMP, Low Noise	PMI/ OP-07EP	1
24	U5	Single, Fast TTL comparator, 8 DIP	MAXIM / MAX9686CPA	1
25	U7,8	HEX D Flip-Flop, TTL, Fast Series	Fairchild / 74F174, or eq.	2
26	N/A	BNC Connector, Receptacle	Amphenol / 31-5329, or eq.	3
27	N/A	28-Pin DIP socket, .600" (U1)	AMP / M528-611D, or eq.	1
28	N/A	SIP Socket Strip, 20, Break-Away	Adv. Intercon. / SS-020-51-TG 1, or eq.	1
29	N/A	Nylon Standoff,1", Round	Plastic Component Corp / C34005, or eq.	4
30	N/A	Nylon Screw, 4-40,3/16", Round Head	Plastic Component Corp / S120040, or eq.	4
31	N/A	Crimp Male Terminal for P3	Molex, 02-09-2103	1
32	N/A	Crimp Female Terminal for P3	Molex, 02-09-1104	8
33	EB7820/24,PCB	Printed Circuit Board	SPT / EB7820/24 Drawing, Rev: B	1

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DB792 PARTS LIST, Rev A

#	Ref. Des.	Description	Vendor Part Number	Qty
1	C1-2	Capacitor, Tant., 10 µF, 25 V, .10"	Sprague / 199D106X0025B A 1, or eq.	2
2	C10-16	Capacitor, 0.01 µF, Chip	Sprague / 11C1206X7R103J050AB, or eq.	7
3	C21-25	Capacitor, 0.1 µF,10%, Ceramic	MURATA / RPE110X7R104K050V or eq.	5
4	D1	2 Terminal IC,1.2 V Reference	Maxim/ ICL8069CCSQ2, or eq.	1
5	P2,3	26 Pin Dual Row Vert PCB Mount Conn	Molex 15-44-3213, or eq.	2
6	R1	Potentiometer, 10K , 12 Turns	Bourns / 44F3533 ,or eq.	1
7	R2	Resistor, 7.5K, 5%, 1/8 W	Allen-Bradley / BB-752-5, or eq.	1
8	R3	Resistor, 22 Ω, 5%, 1/8 W	Allen-Bradley / BB-220-5, or eq.	1
9	R4	Resistor, 10K, 5%, 1/8 W	Allen-Bradley / BB-103-5, or eq.	1
10	R5	Resistor, 15K, 5%, 1/8 W	Allen-Bradley / BB-153-5, or eq.	1
11	R6	Resistor, 20K, 5%, 1/8 W	Allen-Bradley / BB-203-5, or eq.	1
12	R7	Resistor, 1K, 5%, 1/8 W	Allen-Bradley / BB-102-5, or eq.	1
13	R8	Resistor, 1K, 5%, 1/8 W	Allen-Bradley / BB-102-5, or eq.	1
14	R11,12	Resistor, 150 Ω, 5%, 1/8 W	Allen-Bradley / BB-151-5, or eq.	2
15	R20,21	Resistor, 820 Ω, 5%, 1/8 W	Allen-Bradley / BB-821-5, or eq.	2
16	R22	Resistor, 200 Ω, 5%, 1/8 W	Allen-Bradley / BB-221-5, or eq.	1
17	TP1,AG,DG	Test Point Terminal. 76 mil hole dia	Cambion / 160-2044—02-01-00, or eq.	3
18	U9	DAC/TTL, 100 MHz, 12 Bits	AD9713	1
19	U10	OP-AMP, Low Noise	PMI/ OP-07EP	1
20	U11	OP-AMP, Low Distortion	AD9617JN	1
21	N/A	BNC Connector, Receptacle	Amphenol / 31-5329, or eq.	1
22	N/A	Crimp Male Terminal for P3	Molex, 02-09-2103	1
23	DB792,PCB	Printed Circuit Board	SPT/DB792,PCB Drawing, Rev: A1	1
24	FB1-2	Ferrite Bead, Lead Mounted	Fair Rite / 2743001111	2

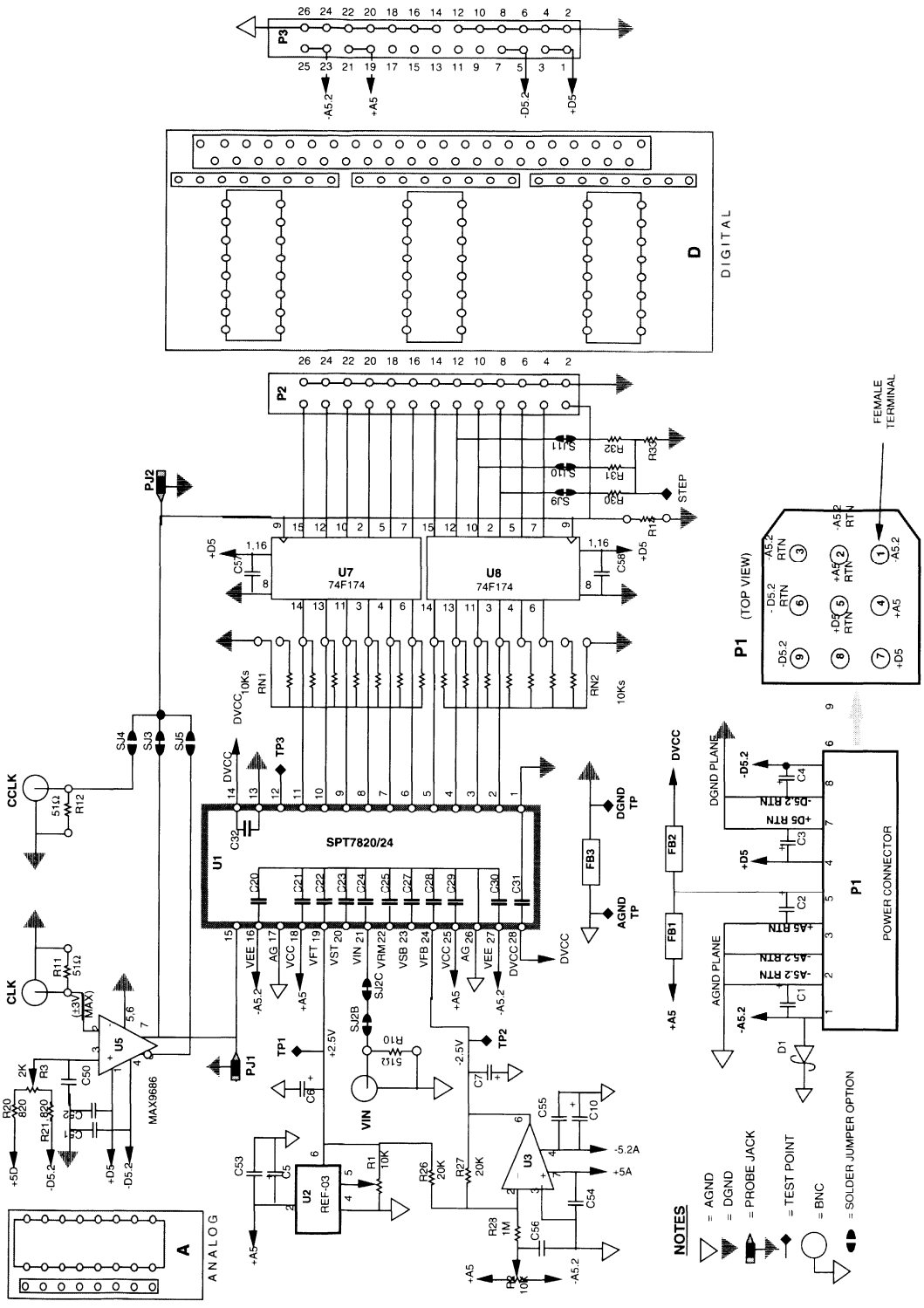

Figure 17 - EB7820/24 Detail Schematic, Rev B

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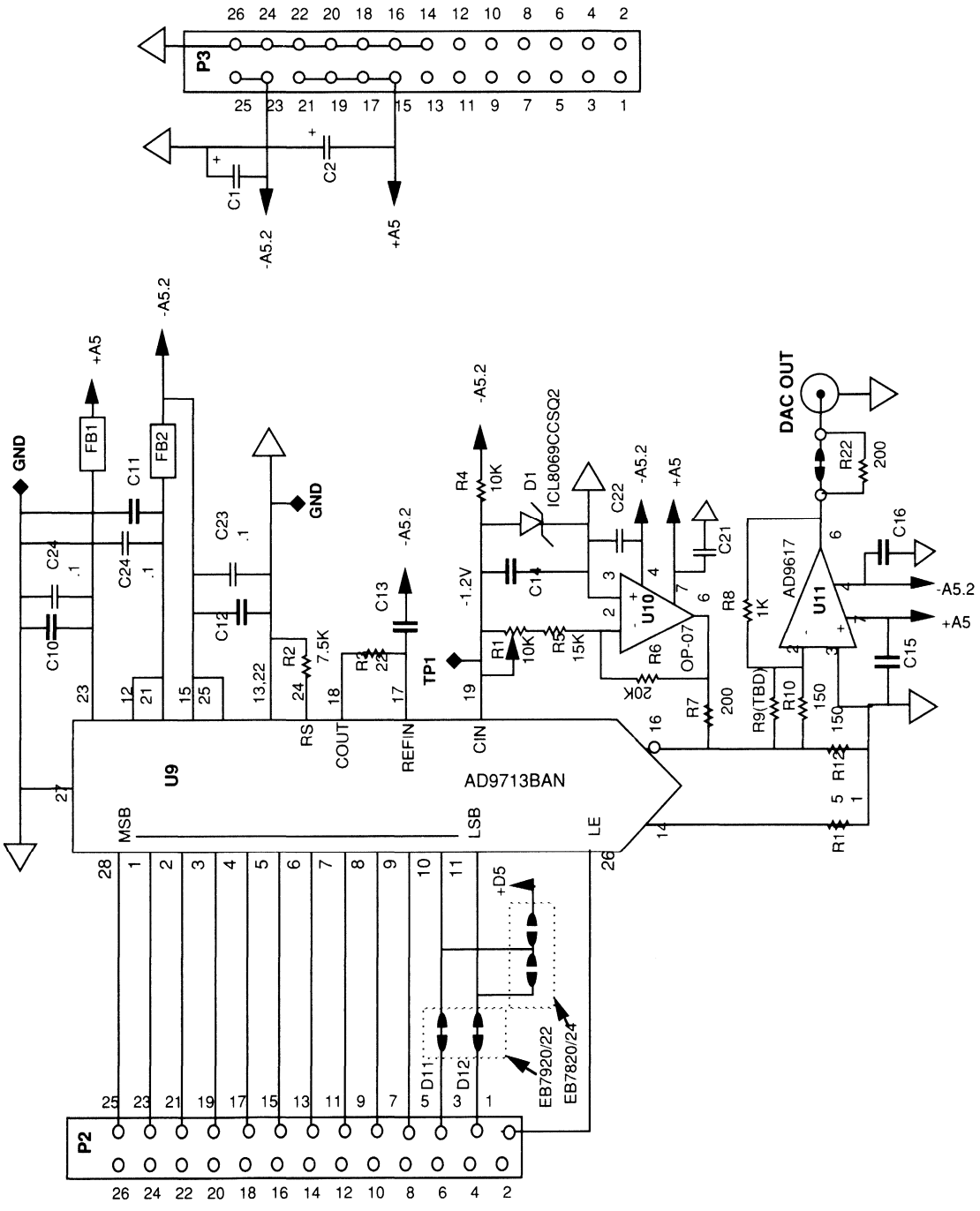

Figure 18 - DB792 Detail Schematic, Rev A1

LEADERSHIP IN DATA CONVERSION AND SIGNAL PROCESSING

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SIGNAL PROCESSING TECHNOLOGIES

AN7920/22

EVALUATION BOARD APPLICATION NOTE

FEATURES

- Up to 30 MSPS Conversion Rate
- On-Board Clock Drivers
- Data Output and Strobe Signal
- User Selectable Capture Clock
- On-Board Reference Drivers
- Dimension : ≈ 4.0" X 7.5"

APPLICATIONS

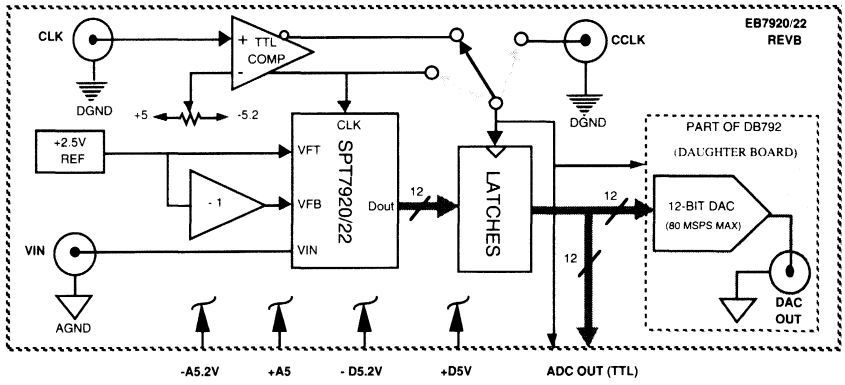
- Evaluation of SPT7920 and SPT7922
- Engineering System Prototype Aid
- Incoming Inspection Tool
- Differential Linearity Error (DLE) Testing
- Integral Linearity Error (ILE) Testing
- AC Accuracy Testing: SNR, THD
- Guide for System Layout

GENERAL DESCRIPTION

The EB7920/22 evaluation board demonstrates the performance of the SPT7920 and SPT7922, monolithic high speed analog-to-digital converters (ADC). This document can also be used as an application note or as supplemental information to the existing data sheet (SPT7920 or SPT7922).

Both the SPT7920 and SPT7922 have analog input ranges of ±2 V. The SPT7920 is capable of digitizing an analog input signal into 12-bit words at a minimum update rate of 10 MSPS, while the SPT7922 is capable of digitizing an analog input signal into 12-bit words at an update rate of a minimum of 30 MSPS. Both devices are pin-compatible. The input/output logic is TTL-compatible.

Figure 1 - Block Diagram (The full detail schematic is shown in figure 17.)



The EB7920/22 (≈ 4" X 7.56") consists of five separate sections:

- Reference circuits
- Clock circuits
- SPT7920 or SPT7922, 12-bit ADC
- Output latches available through 26-pin female ribbon connector
- DAC reconstruction board, DB792, is a separate daughter board (≈2.5" X 3.0") which directly interfaces with the EB7920/22

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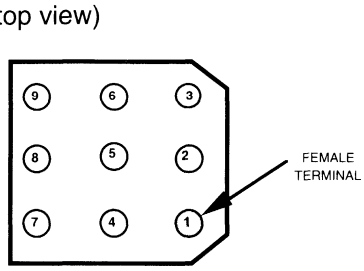
POWER SUPPLIES

The EB7920/22 requires four power supply sources: analog -5.2 V (-A5.2 V), analog +5 V (+A5 V), digital -5.2 V (-D5.2 V), and digital +5 V (+D5 V). P1 is the power connector. (See figure 2.) The recommended operating voltage range is shown in table 1.

Table 1 - Recommended Power Suppy Operating Range

Power Supply	Min	Typ	Max	Typ Current
-A5.2 V	-4.95 V	-5.2 V	-5.45 V	60 mA
+A5 V	+4.75 V	+5.00 V	+5.25 V	240 mA
-D5.2 V	-4.95 V	-5.2 V	-5.45 V	15 mA
+D5 V	+4.75 V	+5.00 V	+5.25 V	60 mA

Figure 2 - P1, Power Supply Connector's Pin Assignment

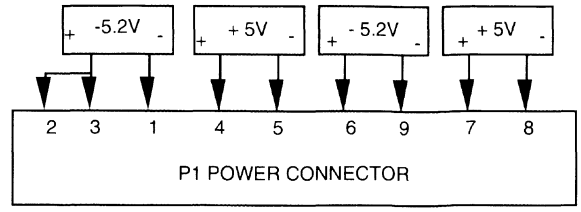


PIN #	PIN ASSIGNMENT
1	Analog -5.2 V
2	Analog -5.2 V Return #1 (AGND)
3	Analog -5.2 V Return #2 (AGND)
4	Analog +5 V
5	Analog +5 V Return (AGND)
6	Digital -5.2 V Return (DGND)
7	Digital +5 V
8	Digital +5 V Return (DGND)
9	Digital -5.2 V

The total power dissipation for the EB7920/22 is typically 1.89 watts.

POWER SUPPLY HOOKUPS

Figure 3 - P1 Connector/Hookup



POWER SUPPLIES AND GROUNDING

The SPT7920/22 requires two analog supply voltages: -A5.2 V and +A5 V. The +A5 V supply is common to analog VCC (pins 20 and 29) and digital DVCC (pins 16 and 32). A ferrite bead in series with each supply (RF1 and RF2) reduces the transient noise injected into VCC. The bead (RF1 or RF2) to SPT7920/22 connections should not be shared with any other device. Bypass each power supply pin as closely as possible to the device (0.1 µF to AGND for each VEE and VCC pin and 0.01 µF to DGND for DVCC pin).

AGND and DGND are isolated on the SPT7920 or SPT7922. Both -A5.2 V and +A5 V are the analog supply sources. As with all very high speed ADCs, grounding is critical. Therefore, the ground plane technique is the most desirable for the SPT7920/22. To accomplish this, split and tie together AGND and DGND ground planes at the device (SPT7920/22) through an RF bead. The EB920/22 is a four-layer printed circuit board: top signal, ground (AGND and DGND) plane, power plane, and the bottom signal. The two ground planes are connected together at the device through a ferrite bead (RF3). All three ferrite beads (RF1-3) are located close to the ADC.

The analog input (pin 24) is physically sandwiched between the reference taps. Plan the printed circuit board layout to minimize any pickup from VIN (high frequency) into the references (VST, VRT1-3 and VSB).

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REFERENCE CIRCUIT

The SPT7920/22 requires the use of two voltage references: VFT and VFB. VFT is the force for the top of the voltage reference ladder (+2.5 V typ) and VFB (-2.5 V typ) is the force for the bottom of the voltage reference ladder. Both voltages are applied across an internal reference ladder resistance of 900 Ω. In addition, there are five reference ladder taps: VST, VRT3, VRT2, VRT1 and VSB. VST is the top of the reference ladder tap (+2 V), VRT3 is the top half of the ladder (+1.0 V typ), VRT2 is the middle point (0.0 V typ), VRT1 is the bottom half (-1.0 V) and VSB is the bottom of the reference ladder tap (-2 V). The voltages seen at VST and VSB are the expected full-scale input voltages of the device when VFT and VFB are driven to the recommended voltages (+2.5 V and -2.5 V typical, respectively). Use VST and VSB to monitor the actual full scale input voltages (±2 V) by adjusting VFT and VFB. These adjustments have some interaction; and repeat them a few times as needed until VST and VSB settle at the desired voltages. Do not drive the three taps (VRT1, VRT2 and VRT3) as is commonly done with the standard flash ADC converter. When not being used, decouple with a 0.01 μFd chip capacitor (surface mounted capacitor) to AGND from each tap to minimize high frequency noise injection.

Referring to figure 17, U2 is the + 2.5 V reference with ± 150 mV of adjustable range (R1 potentiometer). U3 (OP-07) is set up as an inverting amplifier. Its tolerance is 5% with ± 300 mV of adjustable range (R2 potentiometer). SPT recommends that you operate these references (VFT & VFB) to within ±2% (or ±2.5 V ±50 mV) to maintain accuracy within the specified limit. Before each EB7920/22 board is shipped, the references are adjusted for VFT and VFB of ±2.5 V ±5 mV respectively. For each new SPT7920 or SPT7922, readjust the VST and VSB . All measurements must be referenced to AGND test point (provided).

REFERENCE MONITORING

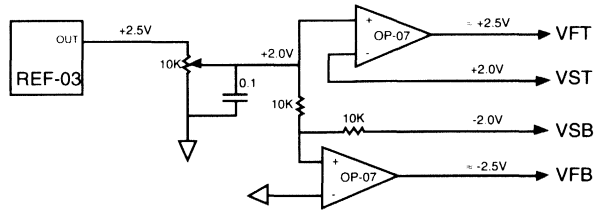
Table 2 - Recommended Operating Voltage Range

	VST	VSB
Point	U1, PIN 21	U1, PIN 27
Min	+1.950 V	-2.050 V
Typ	+2.000 V	-2.000 V
Max	+2.050 V	-1.950 V
Adjust	R1	R2

Note: The SPT7920 and SPT7922 (especially all reference taps: VFT, VFB, VST, VSB, VRT1, VRT2 and VRT3) are very sensitive to electrostatic discharge (ESD).

Figure 17 shows one type of reference driver. Figure 4 (block diagram) illustrates another way to drive the reference circuits using force and sense. This circuit provides a better control on the plus full scale (+FS) and minus full scale (-FS) errors by sensing VST and VSB to ± 2.0 V, respectively. On the other hand, the reference pins VST and VSB are not low impedance nodes thus requiring additional precaution when routing (PCB layout).

Figure 4 - Alternative Reference Driver



SPT7920 OR SPT7922, 12-BIT ADC

The SPT7920 integrated circuit is a 12-bit analog-to-digital converter capable of digitizing an input signal with a minimum update rate of 10 megasamples per second (MSPS). Conversely, the SPT7922 is pin compatible with the SPT7920 except that it is three time faster: 30 MSPS for the sampling frequency. On both devices, the expected full scale analog input range is from VST to VSB. The analog input is latched at the leading edge of the CLK. There are 13 digital TTL outputs. D0-D11 are the parallel TTL output bits, with D0 the LSB, D11 the MSB and D12 the overrange bit. The data outputs are latched at the rising edge of the CLK, with a propagation delay of typically 14 nsec. There is one clock latency between CLK and valid output data (see figure 5 for more detail.) The output code is a straight binary.

Table 3 - SPT7920/22 Output Coding (Ø indicates the flickering bit between logic 0 and 1)

Analog Input	D12 (Overrange bit)	Data output code
<-2.0 V	0	0000 0000 0000
-2.0 V +1 LSB	0	0000 0000 000Ø
0 V	0	0ØØØ ØØØØ ØØØØ
+2.0 V -1 LSB	0	1111 1111 111Ø
>+2.0 V +1/2 LSB	1	1111 1111 1111

Pin 24 is the analog input pin. Selecting the analog input driver for the SPT7920 or SPT7922 should be less of an issue than with most Flash ADCs because the input impedance and input capacitance are typically 300 kΩ and 5 pF, respectively. For example, at 5 MHz and 4 Vp-p sinewave input, the input driver source requires only 0.324 mA of peak output current (4 πFC).

The analog input is directly fed from a BNC (VIN). R10 (51 Ω) is the analog input source termination mounted on a socket as a user-selectable termination. The analog input pin has no circuit protection. Its maximum rating is from VFT to VFB (±2.5 V). In an application in which the analog input range is greater than ±2.5 V, protect the input pin from permanent damage with a voltage limiter. (Refer to input and latchup protection section.)

INPUT CLOCK DRIVER

CLK is the single-ended input clock to the EB7920/22 (evaluation board), CLK IN is the input clock to the SPT7920 or SPT7922, and CCLK is the capture clock used for the output latches (U7 & U8).

The clock input of the SPT7920/22 requires TTL-logic level with a rise time of 6 nsec or faster to improve the noise. Fast TTL-family (74FXX) fits well in this application. Finding a square wave generator, TTL-logic up to 30 MHz, fast slew rate and low jitter is harder than a sine wave, low jitter generator. U5 (MAX9686, TTL voltage comparator) provides most of the above requirements to drive the SPT7920 or SPT7922 (except the low jitter generator). The CLK signal could be a sine wave signal with the amplitude not to exceed ± 3 V (input common mode limitation of U5). R11 (51 Ω) is the CLK source termination. Use R3 to adjust the duty cycle of the CLK IN. CLK IN is in phase with CLK and with a typical propagation delay of 6 nsec . Keep the positive clock (CLK IN) pulse width between 15 nsec to 300 nsec for SPT7922 and 30 to 300 nsec for SPT7920. This is due to the internal THA. When operating the SPT7920 or SPT7922 faster than 3 MSPS, keep the clock duty cycle at approximately 50% ±10%. The probe jack PJ1 is the monitoring test point for the CLK IN. Use this test point when adjusting the clock duty cycle.

Logic low of the CLK IN (pin 17) causes the internal THA to go into track. Keep the SPT7920 or SPT7922 in the track mode when the device is idle for an extended period of time or at the startup time. This setup will prevent the internal THA from going into saturation due to the internal THA's droop. EB7920/22 provides a logic low to the clock of the SPT7920/22 when the pulse generator (CLK) is removed from the evaluation board.

TTL OUTPUT DATA LATCHES

The rise time (Trise) and fall time (Tfall) of the SPT7920/22 (D0-D12) are not symmetrical. The propagation delay with respect to Trise (at the 2.4 V crossing) is typically 14 nsec, and 6 nsec is typical with respect to Tfall at the 2.4 V crossing. Figure 5 illustrates the actual output characteristic of the SPT7920/22. This nonsymmetrical Trise and Tfall creates approximately 8 nsec of invalid data.

In an application in which a reconstruction DAC is needed, the above invalid data zone will cause the reconstruction signal to have an unwanted heavy glitch if the DAC is directly interfaced with SPT7920 or SPT7922. To avoid this, buffer the SPT7920/22 by the edge triggered latches. The FAST family TTL-logic will fit well in this application due to its fast setup and hold time.

U7 and U8 (74F174) are the output latches. The FAST family TTL-logic is very sensitive to electrostatic discharge (ESD). RN1 and RN2 are the 8-pin SIP resistor network, 10 kΩ. They will protect U7 and U8 by providing the ESD path to DGND. The BNC connector (CCLK) is the capture clock, which has 51 Ω termination R12 onboard. The outputs of the data latches (D0-D11) are routed through the standard 26-pin female ribbon connector (P2). SJ3-5 are the solder jumper options for the capture clock. Only one of these jumpers needs to be connected.

- If SJ3 is installed (factory installed when this board was shipped), SPT7920/22 and the latches (U7 & U8) are clocked at the same time. With this configuration, the data seen at the connector P2 adds another clock of latency (two clocks of latency total as shown in figure 6).

- If SJ4 is installed, the capture clock must be supplied externally through CCLK. The setup time (ts) and hold time (th) shown in table 5 must be met when selecting this option.

- If SJ5 is selected, the buffers will be latched at the falling edge of the CLK IN (SPT7920/22). With this option, the setup time (ts) and hold time requirements for the 74F174 latches must be met (table 5). The placement of this capture clock edge is dependent on the clock pulse width and the sampling frequency. This option is not recommended above 25 MSPS.

Table 4- 2, SPT7920/229 output data (Latched), 26-pin Female Ribbon Connector

P2	Function	Logic	P2	Function	Logic
1	CCLK	TTL	2	DGND	DGND
3	D0 (LSB)	TTL	4	DGND	DGND
5	D1	TTL	6	DGND	DGND
7	D2	TTL	8	DGND	DGND
9	D3	TTL	10	DGND	DGND
11	D4	TTL	12	DGND	DGND
13	D5	TTL	14	DGND	DGND
15	D6	TTL	16	DGND	DGND
17	D7	TTL	18	DGND	DGND
19	D8	TTL	20	DGND	DGND
21	D9	TTL	22	DGND	DGND
23	D10	TTL	24	DGND	DGND
25	D11(MSB)	TTL	26	DGND	DGND

The digital outputs (latched) are routed through P2, 26-pin ribbon connector. (See table 4.) The overrange bit (D12) can be viewed through test point TP13. D12 does not bring out through P2.

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Figure 5 - Digital Output Characteristic of the SPT7920 or SPT7922

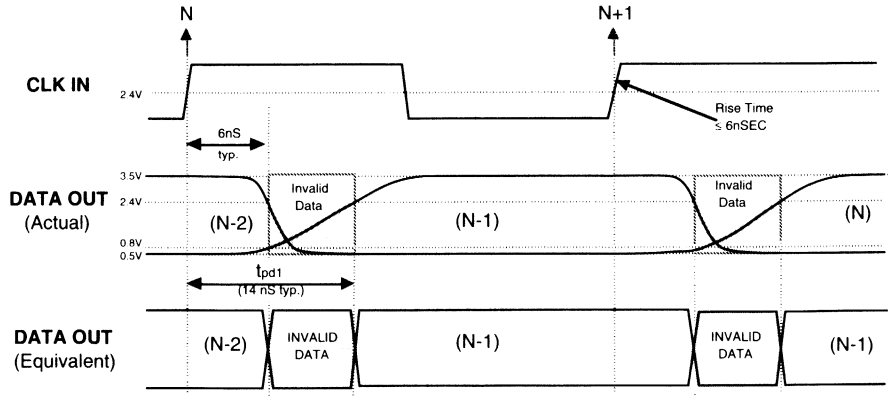


Figure 6 - EB7920/22 Timing Diagram In Which CCLK is the Same as CLK IN

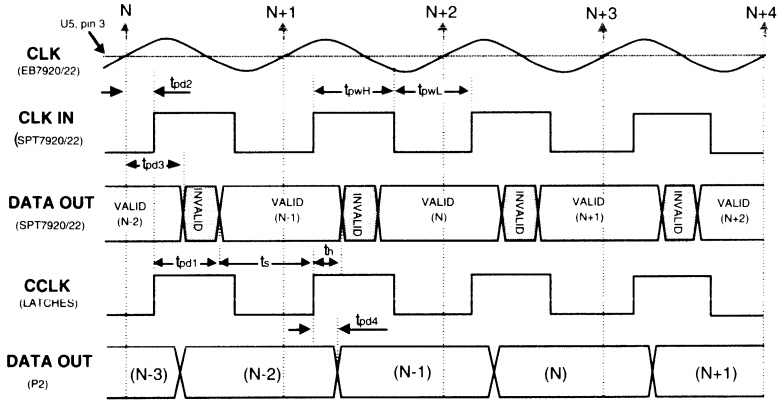


Figure 7 - EB7920/22 Timing Diagram In Which CCLK is 180° Out of Phase From CLK IN

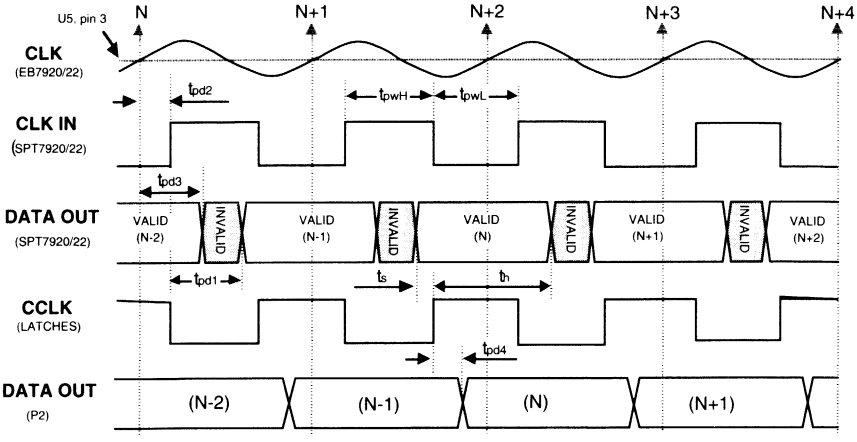


Table 5 - Timing Specification

Function	Description	Min	Typ	Max	Unit
tpd1	SPT7920/22, CLK to Data Valid Prop. Delay	-	14	18	nsec
tdp2	MAX9686 Prop. Delay	-	6	9	nsec
tdp3	SPT7920/22, t_{FALL} Prop. Delay	4.5	7	10	nsec
tdp4	74F174, Prop. Delay	4.5	7	10	nsec
ts	74F174 Setup Time	4	-	-	nsec
th	74174, Hold Time	4	-	-	nsec
tpwH	CLK Positive Pulse Width (SPT7920)	30	-	300	nsec
tpwL	CLK Negative Pulse Width (SPT7920)	30	-	-	nsec
tpwH	CLK Positive Pulse Width (SPT7922)	15	-	300	nsec
tpwL	CLK Negative Pulse Width (SPT7922)	15	-	-	nsec

SPT7920/22 ACQUISITION TIME SPECIFICATION

The acquisition time (Tacq) is defined as the hold-to-track full scale settling time for the internal track and hold (THA). Logic low of the clock input corresponds to track mode and logic high is the hold mode for the internal THA. Figure 8 shows two types of acquisition time:

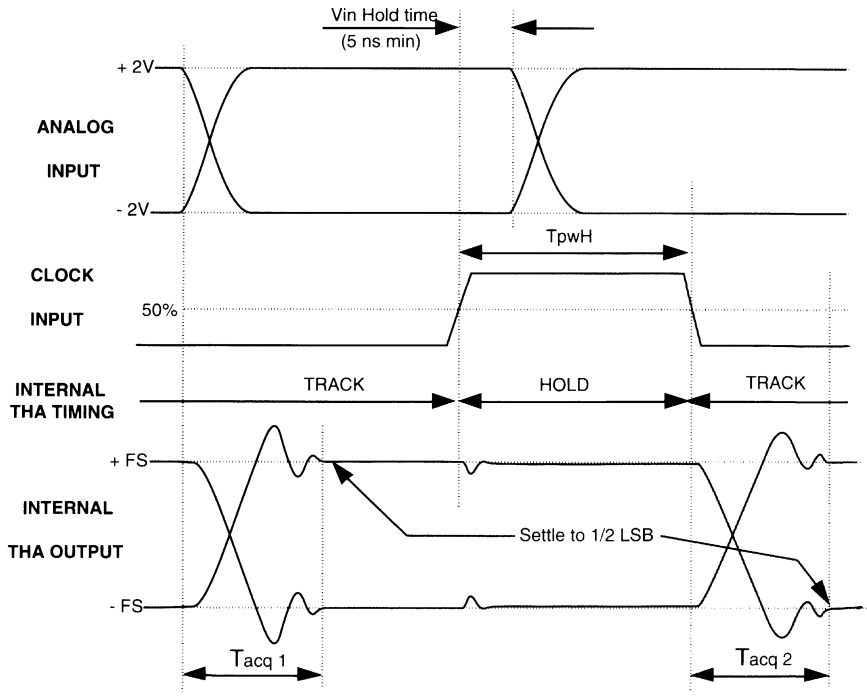
1. Tacq 1 is the settling time of the THA when it is in track and it is driven by the analog input switching.

2. Tacq 2 is the amount of time it takes for the internal THA of the ADC to reacquire the analog input when switching from hold to track (CLK IN from high to low) to within 1/2 LSB.

Both Tacq 1 and Tacq 2 need the same amount of time. (See the acquisition time specification for the respective data sheet.)

The low-to-high clock transition should be placed after both the analog input and the internal THA are settled. The analog input must remain for at least 5 ns (Vin hold time) after the low-to-high clock transition. Keep the clock positive pulse width (TpwH) to within the recommended limit (refer to the specification in the respective data sheet).

Figure 8 - Acquisition Time



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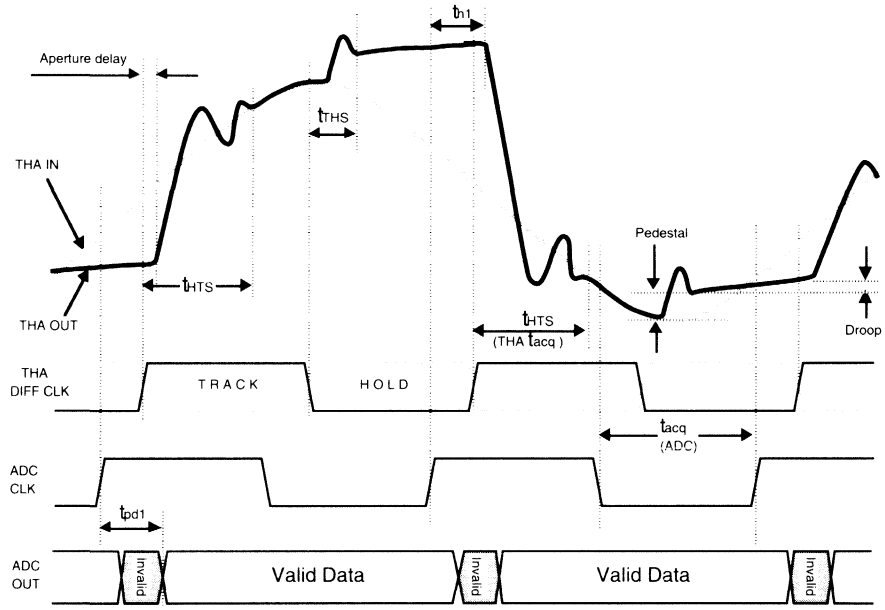
TIMING CONSIDERATIONS WHEN USING AN EXTERNAL TRACK-AND-HOLD

In regards to the SPT7920 or SPT7922 dynamic performance specifications, the signal-to-noise ratio (SNR) and the total harmonic distortion (THD) degrade as the analog input frequency increases. These parameters imply that the differential linearity error (DLE) and the integral linearity error (ILE) degrade as well at high frequency. These degradations are mainly due to the aperture jitter and/or analog input bandwidth limitation and/or slew rate limition of the SPT7920 or SPT7922. Below 1 MHz, the SNR and THD of the SPT7920 and SPT7922 are generally constant. In order to bring these accuracies up (at high frequency), you may need to buffer the analog input using a track-and-hold amplifier (THA). THAs are not perfect (especially at high frequency); otherwise the dynamic performance of the SPT7920 or SPT7922 would be constant and equal to its performance at 1 MHz.

Figure 9 - Critical Timing Between External THA and ADC



Selecting an acceptable THA for a specific application is sometimes difficult. The timing diagram shown in figure 9 and table 6 address the critical timing necessary when driving the ADC from a THA.

Table 6 - Critical Timing Specifications

Parameter	Description	Min	Typ	Max	Unit
tHTS	THA, Hold-to-track settling time	X	X	X	nsec
tTHS	THA, Track-tohold settling time	X	X	X	
tacq	ADC, acquisition time, 4 V step	20			nsec
th1	Hold time after the ADC rising clock	5			nsec

X= This limit depends on the THA chosen

The settling time to 1/2 LSB (488 μV) is one of the principal requirements in a 12-bit THA. This includes both track-to-hold (tTHS) and hold-to-track (tHTS) settling times. tHTS varies with the step size (voltages) that the THA needs to swing. Place the rising edge of the ADC clock after tTHS has settled. SPT7920/22 requires that the analog input be held for an additional 5 nsec minimum (th1) after the rising edge of the clock. Figure 9 shows the ADC is running at Nyquist; the sampling frequency is practically twice the input frequency. In this example, the ADC could have as much as a 4 volt step (±FS) from one conversion to the next. The acquisition time (tacq) of the ADC must be met. This is the time necessary to allow the internal THA of the SPT7920/22 to track (CLK= low) and settle to 1/2 LSB while the input is sharply changed to its new continuous level. The minimum acquisition time is 20 nsec for a 4 volt step and 12 nsec for a 0.5 or less volt step.

The maximum sampling rate of the SPT7920 or SPT7922 when driving from an external THA can be decided from the proper combination of tTHS, tHTS and tacq.

The pedestal and the droop of the THA shown in figure 9 are not critical to the dynamic performance as long as they are constant with respect to the analog input range. They are seen as offset errors.

LOW LEVEL ANALOG INPUT SIGNAL

SPT7920 or SPT7922 requires that the analog input (V_{IN}) range be operated within ±2 V ±2%. Amplification and level shifting are needed for a lower voltage level V_{IN}.

Figure 10 - Driving Circuit Block Diagram

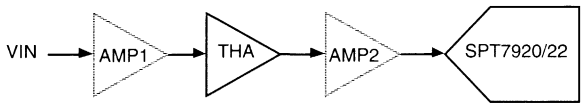


Figure 10 shows the typical analog driving circuit. AMP1 or AMP2 are optional. For an application in which noise is the major concern, use AMP1 (disregard AMP2) low noise amplifier to gain up to ± 2 volts before getting to the THA. In another application in which high frequency VIN is the major concern, use AMP2 instead of AMP1 to amplify the THA signal to ±2 volts before reaching to SPT7920 or SPT7922. In the latter case, the low level V_{IN} provides a faster acquisition time for the THA.

UNCOMMITTED PROTO SOCKET SPACE

Referring to the detail schematic in figure 17, there are two slots available for applications where additional circuits may be needed to interface with the EB7920/22. These two slots (labeled A & D in the PCB assembly) are electrically noncommitted.

- Slot A is physically located near VIN (BNC) and is intended for the analog interfacing circuit. It has one 16-DIP and one 8-SIP.

- Slot D is physically located between P2 and P3 (connectors) and is intended for the digital interfacing circuit. It has three 16-DIPs, three 8-SIPs and one 37-pin D connector.

Both slots have the appropriate power supplies and grounds in their vicinity as labeled.

DB792 DAUGHTER BOARD (RECONSTRUCTION DAC)

DB792 (figure 18) is the daughter board that interfaces directly to the EB7920/22 via P2 and P3. It is suited for an application in which the reconstruction DAC is needed to evaluate the ADC performance in the time domain. DB792 is designed around the Analog Device AD9713B, 12-bit TTL, digital-to-analog converter, 80 MSPS update rate. It is set up in bipolar operation. The detailed schematic is shown in figure 18. Refer to the Analog Device's AD9713B data sheet for detail.

SPT7920/22 INPUT AND LATCHUP PROTECTIONS

The SPT7920/22 is free from any possible latchup when the recommended interfacing circuit shown in figure 11 is followed.

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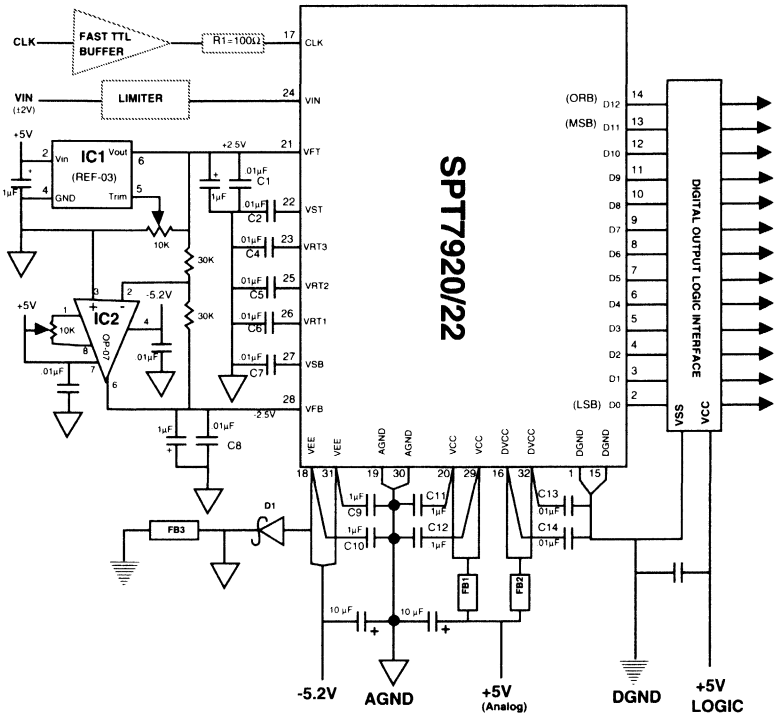
Figure 11 - SPT7920/22 Recommended Interfacing Circuit



The following information is for both latchup and input protection interface requirements:

1) Drive the input clock (pin 17) from a TTL logic ($V_{IH} \leq 4.5$ V). A fast TTL-logic family or equivalent is strongly recommended due to its fast rise time (6 nsec or faster). In the event that the clock is driven from a high current source (greater than 400 mA), use a 100 Ω resistor in series to current limit to roughly 45 mA.

2) D1 is a Schottky or hot carrier diode (Motorolla, 1N5817 or equivalent) installed between VEE and AGND (reverse bias).

3) Both VCC (pin 20 & 29) and DVCC (pin 16 & 32) are driven from the same analog +5 V supply.

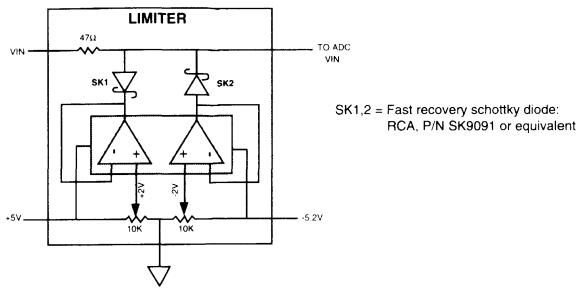
4) Mount the ferrite beads (FB1 and FB2) as closely to the device as possible. The bead to the ADC connections should not be shared with any other device.

5) All reference and power supply pins must be bypassed as closely to the device pin as possible (chip caps C1-14 are preferred): 0.1 μF for VCC and VEE and 0.01 μF for DVCC.

6) The top reference (VFT) driver must be current limited to 20 mA maximum if a different reference driver circuit is used in place of the recommended circuit shown in figure 11.

7) The limiter is required if the maximum peak-to-peak voltage of the analog input exceeds ±2.5 V. Incorporate this limiter within the analog input driver or use the circuit shown in figure 12 below. Another option is to add a 100 Ω resistor in series to current limit the input. This last option adds another LSB error to both ± full scale compared to only 1/2 LSB when using the circuit shown in figure 12.

Figure 12 - An Example of an Input Limiter



SPT7920/22 CHARACTERIZATION

Performance at speed is the main goal in evaluating any ADC, but it is beneficial to start from a relatively low speed and verify key parameters. It is also beneficial to predict performance at speed. If the transition noise and/or the differential linearity of the device perform poorly at low frequency, the SNR at speed cannot be expected to be better. In addition, the low frequency setup can be useful as a verification tool for the test setup.

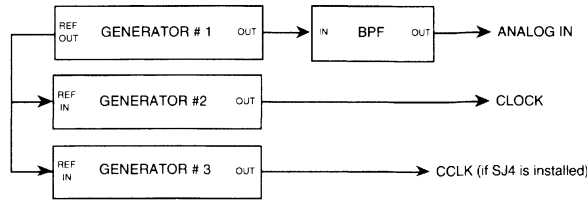
At low frequency there are numerous ways of characterizing the differential linearity error (DLE), integral linearity error (ILE), transition noise, missing codes (MC), synchronous noise, nonmonotonicity, power supply sensitivity and power supply currents. SPT will guide the user through two classical yet powerful testing approaches to achieve fast and relatively accurate results.

High frequency or dynamic testing, the missing codes test, ILE, DLE, VOS and the gain error tests are based on statistical results. They can be performed using the *histogram* technique. SNR and THD are tested by using the Fast Fourier Transform (FFT).

The EB7920/22 was designed to provide optimum capability in fulfilling the above characterization needs.

EQUIPMENT HOOKUP

Figure 13 - Synchronous Equipment Hookup



Coherent testing is recommended in characterizing the SPT7920/22. All three signals (VIN, CLK and CCLK) are synchronized. This testing gives well defined results when using the following suggested techniques for evaluating the performance of the device. These techniques will also significantly reduce the testing time, especially the dynamic testing. The diagram in figure 13 suggests one way to achieve this goal. Generator 1 is the analog input. Generator 2 is the sampling clock, sinewave and ±3 Vp-p maximum. Generator 3 (only needed if the solder jumper option SJ4 is used) is the capture clock, TTL. A phase adjustment option for generator 3 is necessary to place the edge of the capture clock at the proper setup time. R11 and R12 are 51 Ω and serve as termination resistors for the generator 2 and generator 3, respectively.

SELECTION OF SIGNAL GENERATORS

For very high speed and high accuracy ADC testing, selection of both analog and clock inputs is critical. Two parameters are important when selecting generators 1 and 2.

1. The purity of the output sinewave must be at least 76 dB or better of SNR. An appropriate bandpass filter (BPF) installed after the generator will help improve the SNR.
2. The sampling clock jitter or aperture jitter can originate both inside and outside the A/D converter.

Consider the selection of an acceptable clock generator. The uncertainty of the clock placement due to the time jitter (aperture jitter) will degrade the effective performance of the device. This jitter is translated into the ADC amplitude error and is proportional to the analog input slew rate. For a sinusoidal input, the uncertainty of the clock edge placement from cycle to cycle due to equipment jitter will have an effect on the A/D converter performance, especially the SNR.

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SNR (Max) = {20 LOG [1/ (2 π Fin Tj)] + 3.02 } dB,
Where: Fin = analog input frequency
and Tj = the aperture jitter in RMS

SPT uses the following equipment when characterizing/ testing the SNR and THD: HP8644A synthesized signal generator for both generators 1 and 2 and HP3325 function generator for generator 3.

LOW FREQUENCY PERFORMANCE CHECK

This section describes one approach to visual evaluation of the differential linearity error (DLE), missing codes (MC), nonmonotonicity, synchronous noise and transition noise. The BNC DAC OUT (from the mother board, EB792X, figure 17) can be the monitoring point to view the quality of the quantization signal, but this may pose a great deal of difficulty. SPT suggests another approach commonly used in the industry. This approach is to use a three-bit reconstruction DAC generated from the last three LSB's TTL outputs. This circuit is shown in figure 17. When the jumpers SJ9-SJ11 are installed, R30-R33 forms a three-bit DAC as shown in figure 14.

Figure 14 - Three-Bit Reconstruction DAC

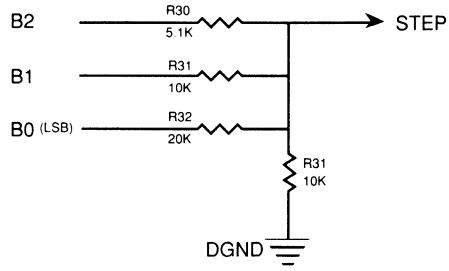
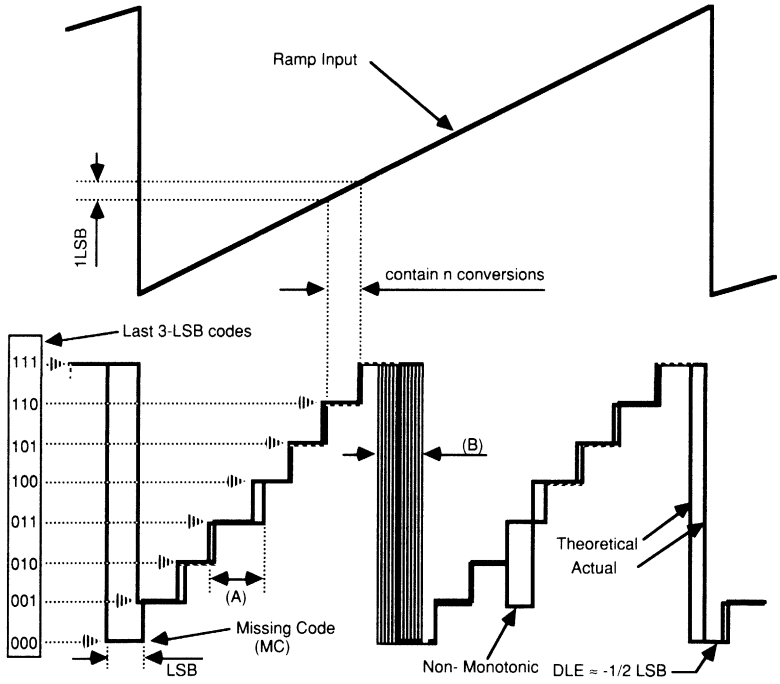


Figure 15 - Three-Bit Reconstruction DAC Waveform Using Analog Input Ramp



(A) is the actual bit weight for the output code multiple of 011
(B) is the major transition noise. This noise level shown is greater than ±1/2 LSB.

The output of this three-bit reconstruction DAC can be viewed through the test point STEP with the scope. For this test, use a function generator for generator 1 and 2 (HP3325A or equivalent) and set up for a ramp output. Replace the BPF with a RC low pass filter (1k & 0.01 μF) to eliminate all high frequency components. The slew rate of this ramp signal should be set to 1 LSB per n conversions (sampling period) for a desired (1/n) test resolution. A n=10 minimum is recommended for this application. The p-p voltage and the period of the ramp input are then dependent on the selection of the number of steps (LSBs) within one ramp's period. Note that R10 (51 Ω) may need to be removed. Set the CLK and CCLK to the same relatively low frequency, approximately 1 MHz or slower. Adjustments are needed to meet the tpwH and ts specifications. (See figure 5-6 and table 5.)

The following formulas summarize the criteria for selecting the analog ramp input signal:

The ramp peak-to-peak voltage: V(p-p) = m (FSR/1024)
The ramp period : T = (m) (n) /Fs
Where:
m=desired number of steps (LSBs) per ramp's period
Fs=sampling frequency
FSR=full scale range (SPT7920's FSR is 4 V, typically)
n = desired test resolution or the number of conversions / LSB

Example:

1. SPT7920 is operated at 500 kHz (sampling frequency).
2. (1/10) of the test resolution is desired.
3. The scope is externally triggered to the ramp input. Three retraces of 8-level steps (or 24 total steps) per ramp's period are selected.
   What peak-to-peak voltage (Vp-p) and period (T) of the ramp input signal are required to drive the SPT7920?

Answer:

1. Fs=500 kHz,
2. n=10,
3. m=24, then V(p-p)= m(FSR/4096)=24(4/4096)=23 mV
   and T=(m) (n)/Fs=(24) (10)/5000,000=480 μsec

Figure 15 shows the relationship between the analog input ramp signal and the resulting three-bit reconstruction DAC. It shows 16 LSBs of p-p input voltage (i.e., two 8-level steps) per period. For an ideal ADC and an ideal ramp input, its digital output code will change state by 1 LSB every (n)th conversion (dash line in the transfer curve). Any error in the ADC will make the corresponding output codes change their state before or after the (n)th conversion. This error will translate into smaller or larger respective step width. The DLE will be judged visually by comparing the actual step size with respect to the ideal step with ±(1/n) LSB of accuracy. In this case, the ideal step is the average of the step size. Other errors (MC, transition noise and nonmonotonicity) can be resolved in a similar way. Figure 15 also gives the identification of each error from the actual transfer curve.

Note that the above input signal will only cover 24 parts in 1024 of the FSR. To identify all errors through the full scale range, sweep the ramp input from -FS to +FS slowly and observe the output steps for the MC, transition noise, DLE and non-monotonicity as indicated in the transfer curve (figure 15). Most generators do not have the DC offset covering the range from +2.5 V to -2.5 V. You may need to construct an additional circuit using the classical summing amplifier to DC-offset the above ramp input signal.

The synchronous noise in an ADC is the distortion of the performance of the device (normally, the DLE can be clearly observed) when the sampling frequency varies. This is usually caused by the digital signals being coupled back internally into the analog input signal. This problem is very common for ADCs using the successive approximation register (SAR) architecture. The ADC that possesses this kind of symptom will present some weak performances at a specific sampling frequency (within the specified sampling rate), but will show better results when the sampling frequency is varied up or down from that weak spot. To verify the synchronous noise using this set-up, slowly change the sampling frequency and observe the transfer curve, especially the changes in DLE.

Advantages

1. Many tests (as stated above) can be extracted from this one simple test set-up.
2. The missing code and transition noise can be more accurately identified than with any other standard test methods.
3. Set-up is quick and relatively accurate.

Disadvantages

1. The accuracy depends on human judgement and can be very difficult if the person is not familiar with it.
2. The exact code is not shown in the transfer curve, but rather a multiple of the last three bits of the ILCB. To overcome this problem, probe every bit using an oscilloscope or install LEDs at each output, P3 connector, to signal the state of each output bit.

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DYNAMIC TESTING

Figure 16 - Dynamic Testing Test Set-Up

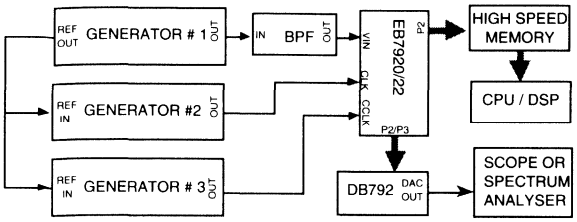


Figure 16 is the recommended block diagram suitable for dynamic testing of the SPT7920 or SPT7922 using the EB7920/22 evaluation board. In an earlier time, the DAC OUT signal had been used to analyze the ADC's dynamic performances (SNR and THD) through a spectrum analyzer. This method of testing presented some uncertainties. The DAC had to be near perfect, free from glitches, and its dynamic accuracy (DLE and ILE) had to be far better than the ADC under test. Any errors in the DAC were added to the total SNR and/or THD.

Today, it is preferable to perform these tests by means of digital signal processing (DSP). Presently, there are numerous standard software packages on the market to service this application. The EB7920/22 provides the data outputs through P2 (see table 5 for detail). The reconstruction DAC could be obtained from DB792 daughter board. Both set-ups are very important in characterizing the dynamic performance of the SPT7920 or SPT7922.

In many cases, the speed of the capture memory is much slower than the available output valid data of the ADC under test. In this case, it is necessary to decimate the capture clock at a rate of Fs/N, in which N is a power of 2. The beat frequency can be achieved by slightly changing the analog input frequency by an amount of Δfin. For a 4096-point FFT, the beat frequency of Δfin = Fc/4096 is added (or subtracted) to the analog input frequency. 4096 data points will be filled in one test period where the input is at Fin $\pm$ (Fc/4096) and the output is updated at 1/Fc interval. Select Fin to be the multiple (integer) of Fc to achieve a complete system synchronization. Both capture memory and the DAC will run at a relatively low update rate (Fs/N). The daughter board DB792 is capable of updating up to 80 MSPS.

EB7920/22 CALIBRATION

This section will serve as a guide for the DC calibration of the EB7920/22 if needed. Note that this board was fully calibrated before the shipment. For every new SPT7920 or SPT7922, VST and VSB voltages require new calibration. Check for the following jumpers installation: SJ2B, SJ2C and SJ3.

1.0 Equipment Needed

1.1 4 DC power supplies: analog +5 V, analog -5.2 V, digital +5 V and digital -5.2 V.
1.2 1 Hewlett Packard, HP3325A, function generator or equivalent
1.3 1 DVM with 5&1/2 digit precision.
1.4 1 oscilloscope.

2.0 Equipment Set-Up/Hook-Up

2.1 No SPT7920 or SPT7922 in U1 socket at this point.
2.2 Connect all 4 power supplies as shown in table 1, figure 2 and figure 3.
2.3 Connect the function generator to CLK BNC .
2.4 Set the CLK to 3 MHz, sinewave , $\pm$2 V.
2.5 Connect VIN to AGND.

3.0 References Calibration

3.1 Monitor TP1 with respect to AGND test point with DVM.
3.2 Adjust R1 for +2.500 V at TP1.
3.3 Monitor TP2 with respect to AGND test point with DVM.
3.4 Adjust R2 for -2.500 V at TP2.
3.5 Turn all power to off.
3.6 Install SPT7920 or SPT7922 into U1 socket (repeat from this procedure for all new devices).
3.7 Turn all powers back to on.
3.8 Monitor U1, pin 22 (VST) with respect to AGND test point with DVM.
3.9 Adjust R1 for + 2.000 V at VST.
3.10 Monitor U1, pin 27 (VSB) with respect to AGND test point with DVM.
3.11 Adjust R2 for -2.000 V at VSB.
3.12 Repeat procedure from paragraph 3.8 until VST and VSB reach the desired voltages ($\pm$2.000 V respectively).

4.0 Clock Circuit Calibration

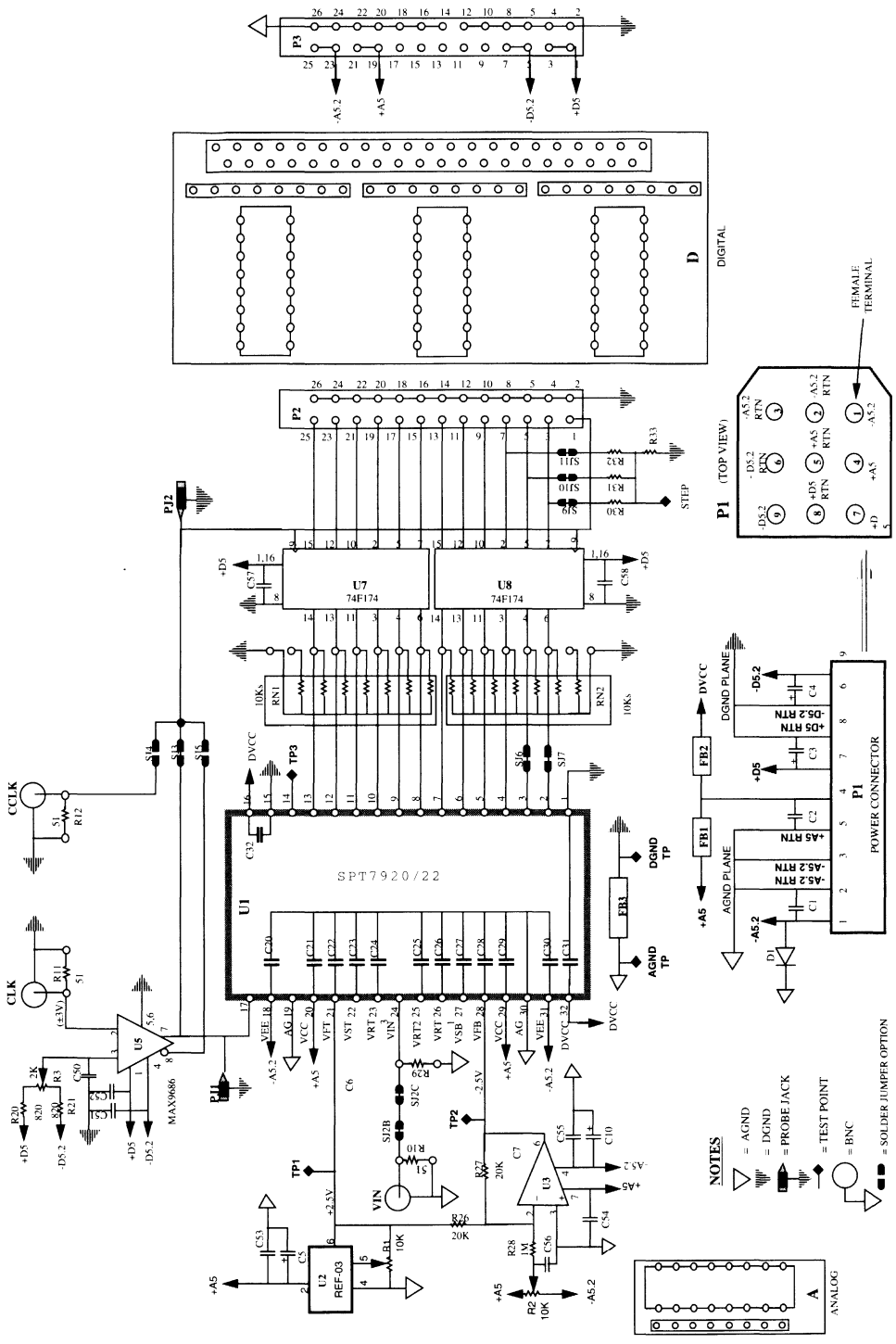
4.1 Monitor PJ1 with scope on channel 1 (Externally sync to the generator).
4.2 Observe the TTL clock and adjust R3 for approximately 50% of duty cycle.

5.0 Latches (U7 & U8) Test

5.1 Remove R10.
5.2 Connect VIN to TP1.
5.3 Monitor P2, odd number pins (3-25) with scope and observe TTL logic high on all pins.
5.4 Connect VIN to TP2.
5.5 Monitor P2, odd number pins (3-25) with scope and observe TTL logic low on all pins.

End of Calibration Procedure

Figure 17 - EB7920/22 Detailed Schematic (Rev B1)



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DB792 PARTS LIST, REV A

#Ref. Des.	Description	Vendor Part Number	Qty
1 C1-2	Capacitor, Tant., 10 µF, 25 V, .10"	Sprague/199D106X0025B A1, or eq	2
2 C10-16	Capacitor, 0.01 µF, Chip	Sprague/11C1206X7R103J050AB, or eq	7
3 C21-25	Capacitor, 0.1 µF, 10%, Ceramic	MURATA/RPE110X7R104K050V or eq	5
4 D1	2 Terminal IC, 1.2 V Reference	Maxim/ICL8069CCSQ2, or eq	1
5 P2,3	26-Pin Dual Row Vert PCB Mount Conn	Molex 15-44-3213, or eq	2
6 R1	Potentiometer, 10k , 12 Turns	Bourns/44F3533, or eq	1
7 R2	Resistor, 7.5k, 5%, 1/8 W	Allen-Bradley/BB-752-5, or eq	1
8 R3	Resistor, 22 Ω, 5%, 1/8 W	Allen-Bradley/BB-220-5, or eq	1
9 R4	Resistor, 10k, 5%, 1/8 W	Allen-Bradley/BB-103-5, or eq	1
10 R5	Resistor, 15k, 5%, 1/8 W	Allen-Bradley/BB-153-5, or eq	1
11 R6	Resistor, 20k, 5%, 1/8 W	Allen-Bradley/BB-203-5, or eq	1
12 R7	Resistor, 1k, 5%, 1/8 W	Allen-Bradley/BB-102-5, or eq	1
13 R8	Resistor, 1k, 5%, 1/8 W	Allen-Bradley/BB-102-5, or eq	1
14 R11,12	Resistor, 150 Ω, 5%, 1/8 W	Allen-Bradley/BB-151-5, or eq	2
15 R20,21	Resistor, 820 Ω, 5%, 1/8 W	Allen-Bradley/BB-821-5, or eq	2
16 R22	Resistor, 200 Ω, 5%, 1/8 W	Allen-Bradley/BB-221-5, or eq	1
17 TP1,AG,DG	Test Point Terminal. 76 Mil Hole Dia	Cambion/160-2044—02-01-00, or eq	3
18 U9	DAC/TTL, 100 MHz, 12 Bits	AD9713	1
19 U10	OP-AMP, Low Noise	PMI/OP-07EP	1
20 U11	OP-AMP, Low Distortion	AD9617JN	1
21 N/A	BNC Connector, Receptacle	Amphenol/31-5329, or eq	1
22 N/A	Crimp Male Terminal for P3	Molex, 02-09-2103	1
23 DB792,PCB	Printed Circuit Board	SPT/DB792, PCB Drawing, Rev: A1	1
24 FB1-2	Ferrite Bead, Lead Mounted	Fair Rite/2743001111	2

LEADERSHIP IN DATA CONVERSION AND SIGNAL PROCESSING

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EB7920/22 PARTS LIST, REV B

#	Ref. Des.	Description	Vendor Part Number	Qty
1	C1-7,10	Capacitor, Tant., 10 µF, 25 V, .10"	Sprague/199D106X0025B A1, or eq	8
2	C20,30	Capacitor, 0.1 µF, Chip	Sprague/11C1206X7R104J050AB, or eq	2
3	C21-29,31,32	Capacitor, 0.01 µF, Chip	Sprague/11C1206X7R103J050AB, or eq	11
4	C50-58	Capacitor, 0.01 µF, 10%, Ceramic	MURATA/RPE110X7R103K050V or eq	9
5	D1	Lead Mounted, Hot Carrier Diode	MOT/IN5817, or eq	1
6	FB1-3	Ferrite Bead, Lead Mounted	Fair Rite, 2743001111	3
7	P2,3	Ribbon Plug Connector	T & B Ansley/622-2627, or eq	2
8	P1	Power Connector, 9 Pins	Molex/09-18-5094, or eq	1
9	P1/Recept	Power Connector, 9 Pins, Recept.	Molex/03-09-1093, or eq	1
10	PJ1-2	Probe Connector (25 Sets/Bag)	Tektronix/131-4353-00	2
11	R3	Potentiometer, 2k, 12 Turns	Bourns/44F3531, or eq	1
12	R1,2	Potentiometer, 10k , 12 Turns	Bourns/44F3533, or eq	2
13	R10-12	Resistor, 51 Ω, 5%, 1/8 W	Allen-Bradley/BB-510-5, or eq	3
14	R20,21	Resistor, 820 Ω, 5%, 1/8 W	Allen-Bradley/BB-821-5, or eq	2
15	R26,27,30	Resistor, 20k, 5%, 1/8 W	Allen-Bradley/BB-203-5, or eq	3
16	R28	Resistor, 1M, 5%, 1/8 W	Allen-Bradley/BB-105-5, or eq	1
17	R32	Resistor, 5.1k, 5%, 1/8 W	Allen-Bradley/BB-512-5, or eq	1
18	R33	Resistor, 10k, 5%, 1/8 W	Allen-Bradley/BB-103-5, or eq	1
19	RN1,2	8-pin SIP Resistor, 10k, 708A Type	Newark 81F9599, or eq	2
20	TP1-3,AG,DG,STEP	Test Point Terminal, 76 Mil Hole Dia	Cambion/160-2044—02-01-00, or eq	6
21	U1	Device Under Test, 10-Bit ADC	SPT7920 or SPT7922	1
22	U2	+2.5 V Precision Voltage Reference	PMI/REF-03GP, or eq	1
23	U3	OP-AMP, Low Noise	PMI/ OP-07EP	1
24	U5	Single, Fast TTL Comparator, 8-DIP	MAXIM/MAX9686CPA	1
25	U7,8	HEX D Flip-Flop, TTL, Fast series	Fairchild/74F174, or eq	2
26	N/A	BNC Connector, Receptacle	Amphenol/31-5329, or eq	3
27	N/A	32-Pin DIP Socket, .600" (U1)	Aries/32-6518-10T, eq	1
28	N/A	SIP Socket Strip, 20, Break-Away	Adv. Intercon/SS-020-51-TG 1, or eq	1
29	N/A	Nylon Standoff, 1", Round	Plastic Component Corp/C34005, or eq	4
30	N/A	Nylon Screw, 4-40, 3/16", Round Head	Plastic Component Corp/S120040, or eq	4
31	N/A	Crimp Male Terminal for P3	Molex, 02-09-2103	1
32	N/A	Crimp Female Terminal for P3	Molex, 02-09-1104	8
33	EB7920/22,PCB	Printed Circuit Board	SPT/EB7920/22 Drawing, Rev: B	1

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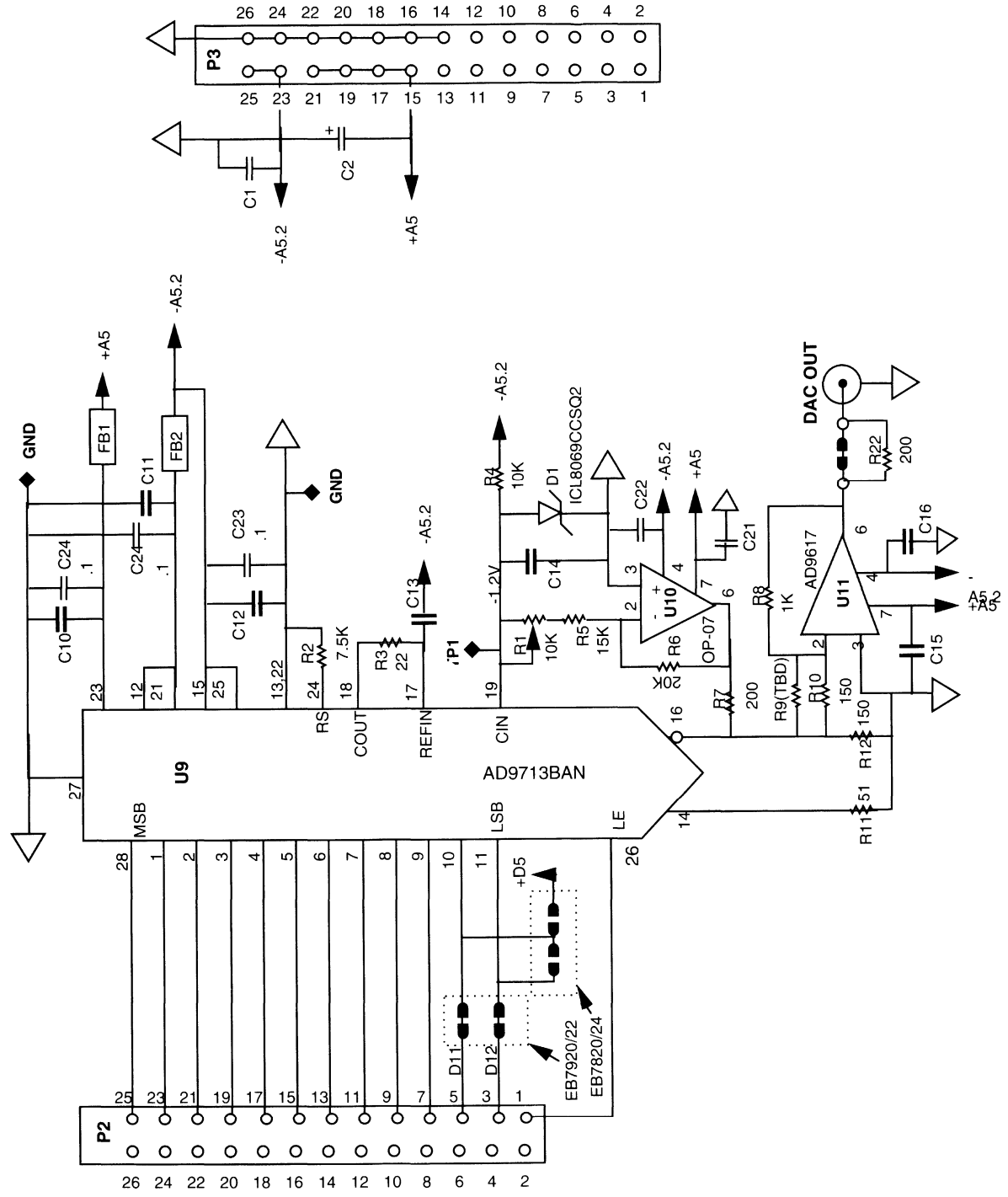
Figure 13 - DB792 Detailed Schematic (Rev A1)



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SIGNAL PROCESSING TECHNOLOGIES

QUALITY ASSURANCE

QUALITY AND RELIABILITY

To remain competitive in today's integrated circuit market, a company must work continuously to improve quality. Improved quality and increased reliability are achieved by reducing variation of output using statistical process control.

Quality and reliability of electronic components are critical issues at Signal Processing Technologies. Realizing the relationship between its customers' success and its own, SPT has put into place a quality assurance program that makes its products among the highest quality and most reliable components available. In doing so, the SPT program complies with the following military specifications: MIL-STD-883, MIL-M-38510, MIL-I-45208, MIL-Q-9858, MIL-STD-105, MIL-STD-1686, and MIL-STD-45662.

Certification in accordance with MIL-STD-883 and MIL-M-38510 is required in order to manufacture and sell Class B and Hi-Rel products. SPT is certified in this area and updates the process annually by means of self audits and required document control. SPT's MIL-STD-883 manufacturing process includes:

- A dedicated facility where manufacturing and testing operations are performed with state-of-the-art instrumentation and automatic test equipment.
- Fully documented and controlled manufacturing processes that utilize procedures to ensure total compliance with applicable military and customer specifications.
- Screening operations designed to isolate potential infant mortality failures before they are shipped to customers.
- A documented product traveler system that details and guarantees flow of product throughout the SPT manufacturing process.
- A training program to assure that SPT employees with responsibilities in the manufacturing flow of products understand and adhere to the requirements of controlled specifications and procedures.
- Operator training and certification programs to provide highly trained personnel qualified to manufacture and test SPT parts.
- A product analysis system that provides the necessary input to update applicable processes and associated documentation.
- An SPT manufacturing facility that minimizes electrostatic discharge (ESD) damage. The SPT ESD program complies with guidelines established by MIL-STD-1686.
- Equipment calibration performed and controlled by the guidelines established under MIL-STD-45662.
- A quality assurance inspection system that maintains quality products acceptable to both the customer and SPT.
- Product reliability ensured through comprehensive Quality Assurance monitoring throughout the manufacturing process and screening of the final product.
- Initial full-product qualification for Class B and Hi-Rel products before the product is released into the production process.

All SPT products are fully characterized and initially qualified to MIL-M-38510 requirements before introduction to the production process. After successful product qualification, periodic product reliability testing and screening of Quality Conformance Inspection groups A, B, C, and D takes place to assure the short-term quality and long-term reliability of the products.

APPLICABLE GOVERNMENT SPECIFICATIONS AND STANDARDS

MIL-STD-883
TEST METHODS AND PROCEDURES FOR MICROELECTRONICS

MIL-STD-883 establishes uniform methods, controls and procedures for designing, testing, identifying and certifying microelectronic devices, including basic environment tests. All certified SPT products are compliant with all applicable methods and associated procedures for Class B products.

MIL-M-38510
GENERAL SPECIFICATION FOR MICROCIRCUITS

MIL-M-38510 supports government microcircuit application and logistic programs. All certified SPT products are compliant with applicable sections of MIL-M-38510 are required by MIL-STD-883 for Class B related products.

MIL-I-45208
INSPECTION SYSTEM REQUIREMENTS

MIL-I-45208 establishes requirements for inspection systems pertaining to the inspections and tests necessary to substantiate product conformance to drawings, specifications and contract requirements. SPT's inspection system meets the requirements of MIL-I-45208.

MIL-Q-9858
QUALITY PROGRAM REQUIREMENTS

MIL-Q-9858 establishes a contractor quality program to assure compliance with the requirements of applicable contracts. SPT's quality program meets the requirements of MIL-Q-9858.

MIL-STD-105
SAMPLING PROCEDURES AND TABLES FOR INSPECTION BY ATTRIBUTE

MIL-STD-105 establishes sampling plans and procedures for inspection by attributes. SPT's sampling procedures and tables comply with the requirements of MIL-STD-105.

MIL-STD-1686
ELECTROSTATIC DISCHARGE CONTROL PROGRAM FOR PROTECTION OF ELECTRICAL AND ELECTRONIC PARTS, ASSEMBLIES AND EQUIPMENT

MIL-STD-1686 establishes the requirements for an ESD control program to minimize the effects of ESD on parts, assemblies and equipment. An effective ESD program increases reliability while decreasing maintenance actions and lifetime costs. SPT's ESD program fully complies with the requirements of MIL-STD-1686.

MIL-STD-45662
CALIBRATION SYSTEMS REQUIREMENTS

MIL-STD-45662 provides requirements for the establishment and maintenance of a calibration system to control the accuracy of measurement and test equipment and measurement standards used to assure that supplies and services delivered to the government comply with prescribed technical requirements. SPT's calibration system was established to the requirements of MIL-STD-45662.

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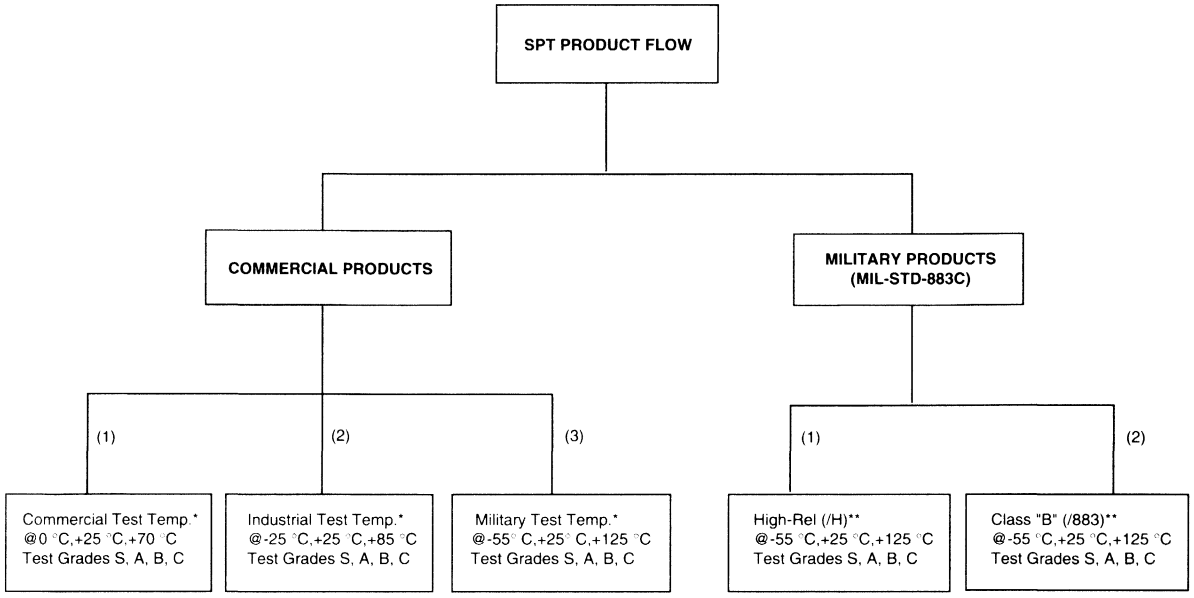
SPT PRODUCT FLOW DESCRIPTION



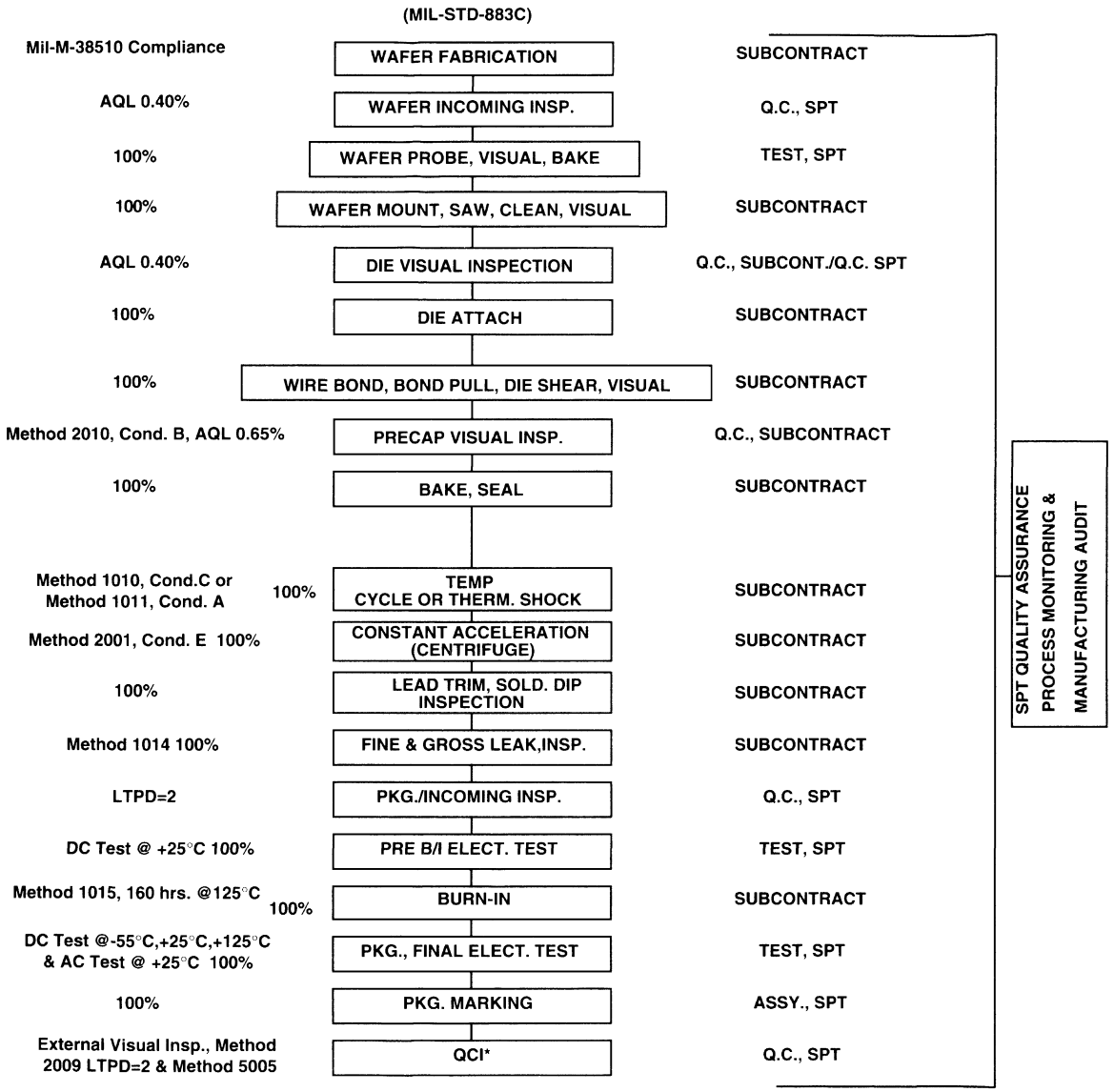
* The only difference between Commercial, Industrial, and Military is the Test temperature, although all three are considered Commercial products.

** Differences between:	/H	and /883
1) Mil-M-38510 Certified wafer FAB required.	No	Yes
2) Lot traceability required	Yes	Yes
3) PDA Calculation required	Yes	Yes
4) Off-shore assembly permitted	Yes	Yes
5) Method 5004, Class "B" screening procedures	Yes	Yes
6) Method 5005, Class "B" initial product Qual. group A, B, C, & D required	Yes	Yes

** Differences between:	/H	and /883
7) QCI Visual & Group A on every production lot required	Yes	Yes
8) QCI group B on every production lot required	No	Yes
9) QCI group C every 3 months of production required	No	Yes
10) QCI group D every 6 months of production required	No	Yes
11) Certificate of Compliance w/every lot shipment required	Yes	Yes

12

SPT MILITARY PRODUCT FLOW (1)



(1) INCLUDES HIGH-REL (/H) AND CLASS "B" (/883) PRODUCTS. THIS STANDARD FLOW IS SUBJECT TO CHANGE DUE TO PRODUCT SPECIFIC FLOW.

* GROUP "A" ELECTRICAL TEST IS PERFORMED @-55°C, +25°C, +125°C FOR BOTH /H AND /883 PRODUCTS.

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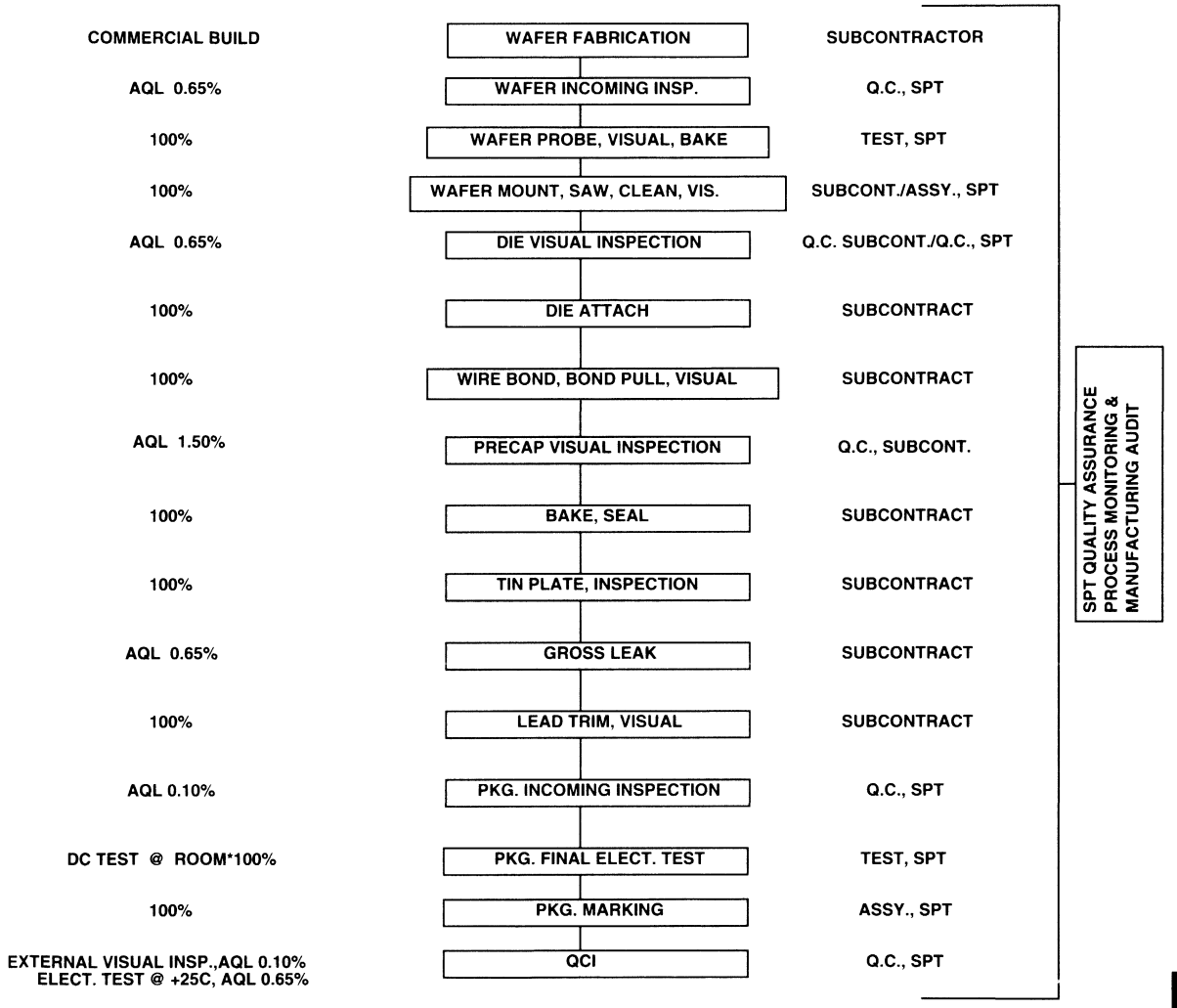
SPT COMMERCIAL PRODUCT FLOW (1)

SECTION 31
COMMERCIAL PRODUCT FLOW



(1) INCLUDES COMMERCIAL, INDUSTRIAL & MILITARY TEST TEMPERATURE. THIS STANDARD FLOW IS SUBJECT TO CHANGE DUE TO PRODUCT SPECIFIC FLOW.

* HOT AND/OR COLD TEST TEMPERATURES AND AC TEST ARE PERFORMED ONLY WHEN REQUIRED.

LEADERSHIP IN DATA CONVERSION AND SIGNAL PROCESSING

4755 Forge Road, Co. Springs, CO 80907
PH: (719) 528-2300; Fax: (719) 528-2370

GENERAL PRODUCT INFORMATION 1
ORDERING INFORMATION 2
ANALOG-TO-DIGITAL CONVERTERS 3
DIGITAL-TO-ANALOG CONVERTERS 4
COMPARATORS 5
FILTERS 6
VOLTAGE REGULATORS 7
RF AMPLIFIERS 8
POWER CONVERSION PRODUCTS 9
EVALUATION BOARDS 10
APPLICATION NOTES 11
QUALITY ASSURANCE 12
PACKAGE OUTLINES 13
SALES OFFICES 14

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Section 13 Package Outlines

20-Lead Sidebrazed 13-5
28-Lead Sidebrazed 13-5
32-Lead Sidebrazed 13-6
42-Lead Sidebrazed 13-6

16-Lead Cerdip 13-7
24-Lead Cerdip 13-7
28-Lead Cerdip 13-8

16-Lead Plastic Dip 13-8
20-Lead Plastic Dip 13-9
28-Lead Plastic Dip 13-9
32-Lead Plastic Dip 13-10

20-Lead Leadless Chip Carrier 13-10
28-Lead Leadless Chip Carrier 13-11

28-Lead Small Outline IC (SOIC) 13-11

20-Lead Plastic Leaded Chip Carrier 13-12

46-Lead Pin-Grid Array 13-12
68-Lead Pin-Grid Array 13-13

8-Lead Plastic Surface Mount (MFP-8) 13-13

3-Lead Plastic (TO-92N) 13-13
3-Lead Plastic (TO-92NT) 13-14

UPACK-3 13-14
UPACK-5 13-14

SOT23L 13-14

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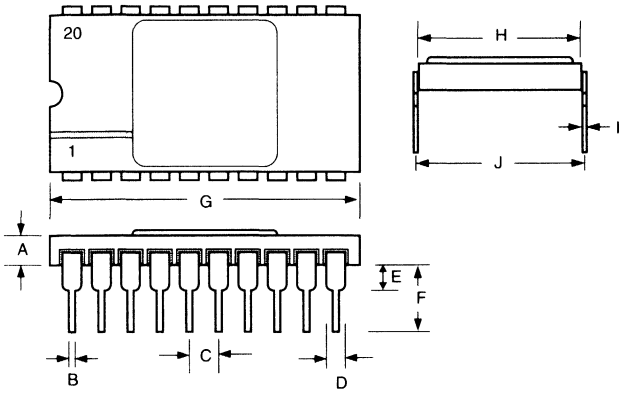
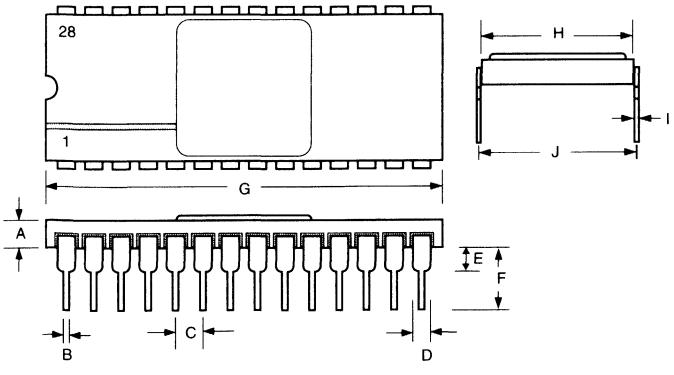
PACKAGING INFORMATION

20-LEAD SIDEBRAZED



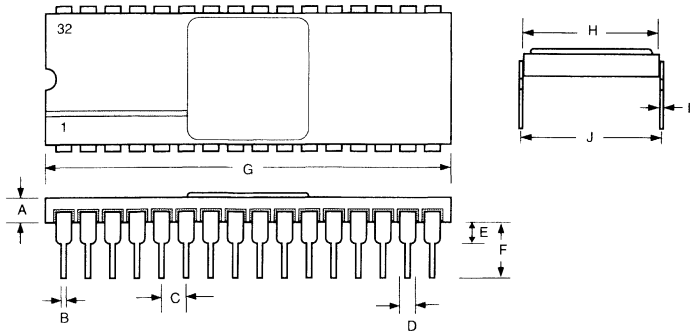
SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.075	0.095	1.91	2.41
B	0.014	0.023	0.36	0.58
C	0.090	0.110	2.29	2.79
D	0.030	0.070	0.76	1.78
E	0.015	0.060	0.38	1.52
F	0.150		3.81	
G		1.060		26.92
H	0.220	0.310	5.59	7.87
I	0.008	0.015	0.20	0.38
J	0.290	0.320	7.37	8.13

28-LEAD SIDEBRAZED



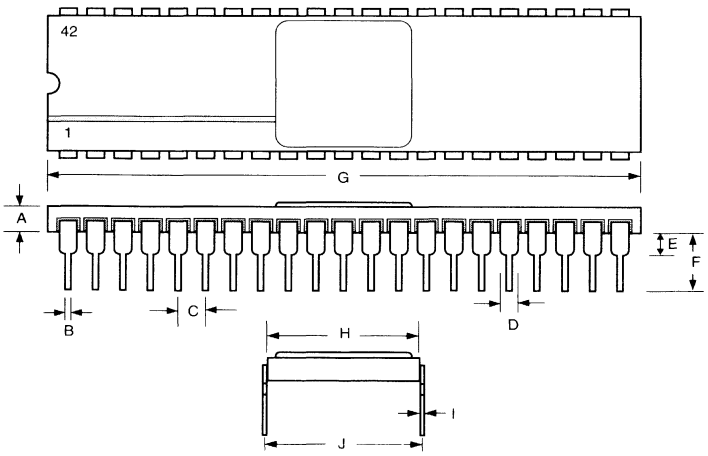
SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.077	0.093	1.96	2.36
B	0.016	0.020	0.41	0.51
C	0.095	0.105	2.41	2.67
D		.050 typ	0.00	1.27
E	0.040	0.060	1.02	1.52
F	0.215	0.235	5.46	5.97
G	1.388	1.412	35.26	35.86
H	0.585	0.605	14.86	15.37
I	0.009	0.012	0.23	0.30
J	0.600	0.620	15.24	15.75

32-LEAD SIDEBRAZED



SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.081	0.099	2.06	2.51
B	0.016	0.020	0.41	0.51
C	0.095	0.105	2.41	2.67
D		.050 typ		1.27
E	0.040		1.02	5.72
F	0.175	0.225	4.45	41.15
G	1.580	1.620	40.13	15.37
H	0.585	0.605	14.86	0.30
I	0.009	0.012	0.23	15.75
J	0.600	0.620	15.24	15.75

42-LEAD SIDEBRAZED



SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.081	0.099	2.06	2.51
B	0.016	0.020	0.41	0.51
C	0.095	0.105	2.41	2.67
D		.050 typ		1.27
E		.050 typ		1.27
F		0.275		6.99
G	2.080	2.120	52.83	53.85
H	0.585	0.605	14.86	15.37
I	0.008	0.015	0.20	0.38
J	0.600	0.620	15.24	15.75

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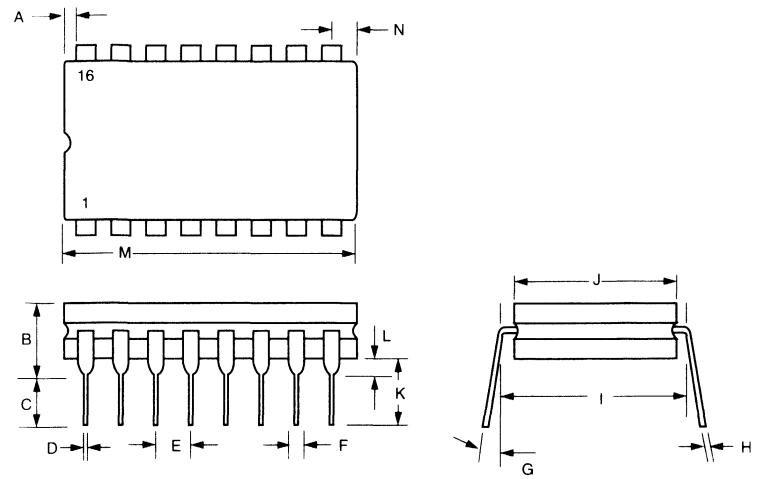
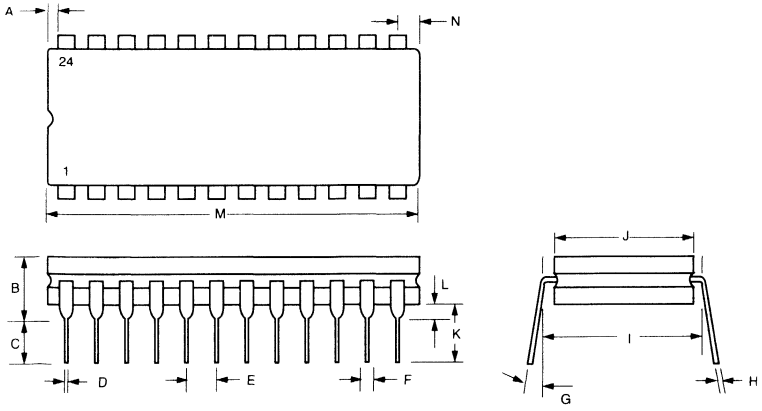
SPT

16-LEAD CERDIP



SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.005		0.13	
B		0.200		5.08
C	0.125	0.150	3.18	3.81
D	0.015	0.023	0.38	0.58
E	0.090	0.110	2.29	2.79
F	0.030	0.065	0.76	1.65
G	0°	15°	0°	15°
H	0.008	0.015	0.20	0.38
I	0.290	0.320	7.37	8.13
J	0.250	0.310	6.35	7.87
K	0.140	0.200	3.56	5.08
L	0.015	0.050	0.38	1.27
M	0.745	0.785	18.92	19.94
N	0.015	0.050	0.38	1.27

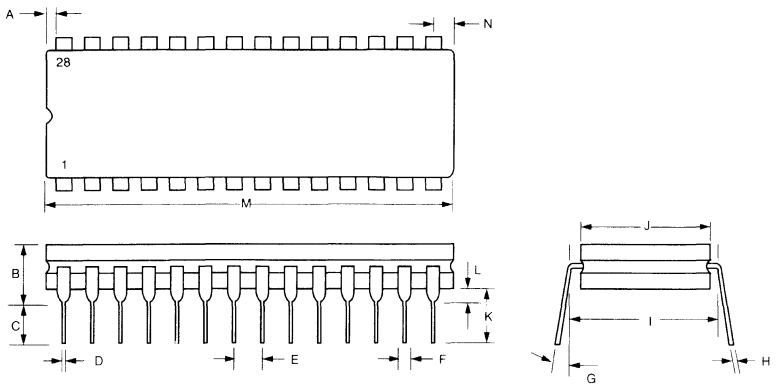
24-LEAD CERDIP



SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.005		0.13	
B		0.200		5.08
C	0.125	0.150	3.18	3.81
D	0.015	0.023	0.38	0.58
E	0.090	0.110	2.29	2.79
F	0.030	0.065	0.76	1.65
G	0°	15°	0°	15°
H	0.008	0.015	0.20	0.38
I	0.290	0.320	7.37	8.13
J	0.250	0.310	6.35	7.87
K	0.140	0.200	3.56	5.08
L	0.015	0.050	0.38	1.27
M	0.745	0.785	18.92	19.94
N	0.015	0.050	0.38	1.27

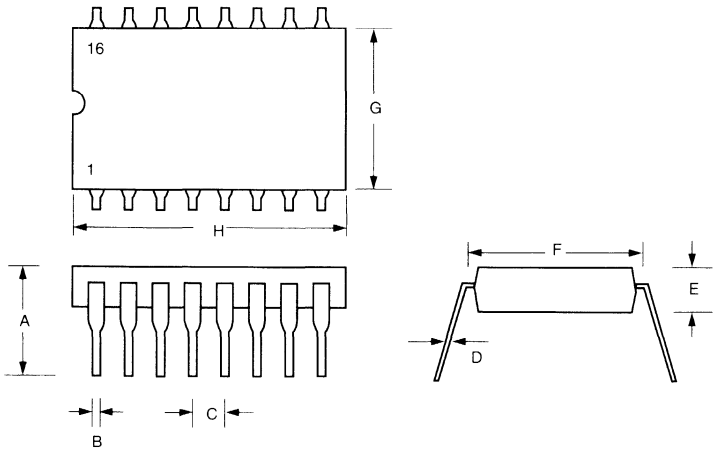
13

28-LEAD CERDIP



SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.005		0.13	
B	0.205	0.235	5.21	5.97
C	0.120	0.200	3.05	5.08
D	0.016	0.020	0.41	0.51
E	0.090	0.110	2.29	2.79
F	0.045	0.065	1.14	1.65
G	0°	15°	0	15°
H	0.009	0.011	0.23	0.28
I	0.590	0.610	14.99	15.49
J	0.500	0.550	12.70	13.97
K	0.160	0.260	4.06	6.60
L	0.040	0.060	1.02	1.52
M	1.430	1.490	36.32	37.85
N	0.060	0.100	1.52	2.54

16-LEAD PLASTIC DIP



SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A		0.300		7.62
B	0.014	0.026	0.36	0.66
C		.100 typ		2.54
D		.010 typ		0.25
E	1.150	1.950	29.21	49.53
F	0.290	0.330	7.37	8.38
G	0.246	0.254	6.25	6.45
H	0.740	0.760	18.80	19.30

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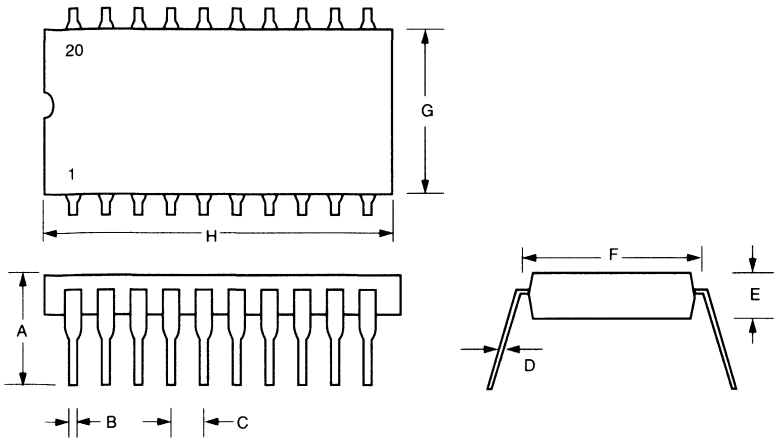
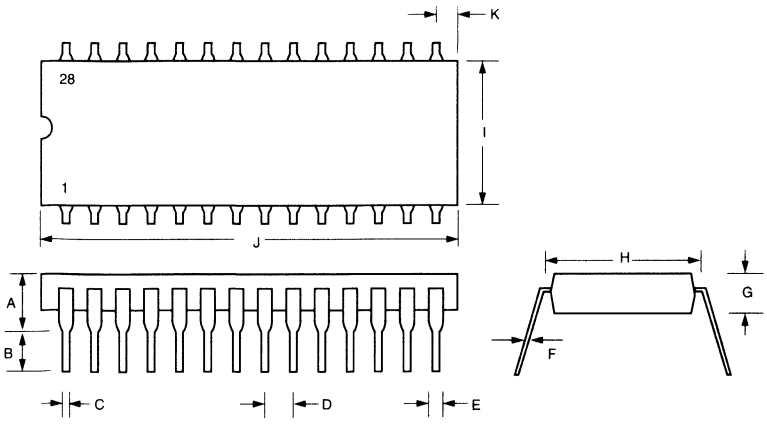
20-LEAD PLASTIC DIP



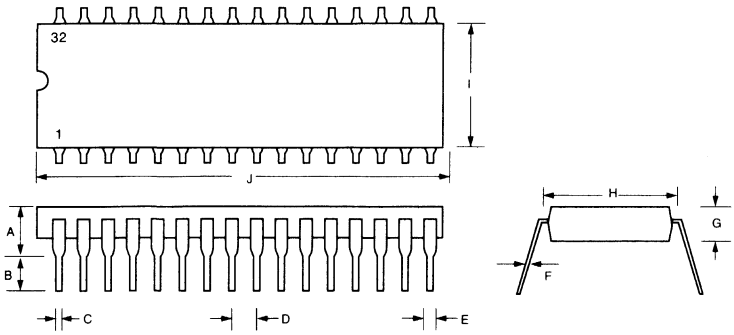
SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A		0.300		7.62
B	0.014	0.026	0.36	0.66
C		.100 typ		2.54
D		.010 typ		0.25
E		1.20 typ		30.48
F	0.290	0.330	7.37	8.38
G	0.246	0.254	6.25	6.45
H	1.010	1.030	25.65	26.16

28-LEAD PLASTIC DIP



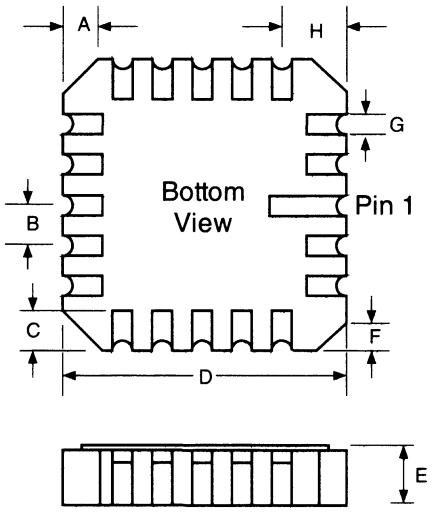
SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A		0.200		5.08
B	0.120	0.135	3.05	3.43
C		0.020		0.51
D		0.100		2.54
E		0.067		1.70
F		0.013		0.33
G	0.170	0.180	4.32	4.57
H		0.622		15.80
I		0.555		14.10
J		1.460		37.08
K		0.085		2.16

32-LEAD PLASTIC DIP



SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A		0.200		5.08
B	0.128	0.131	3.25	3.33
C	0.017	0.018	0.43	0.46
D		.100 typ		2.54
E	0.059	0.060	1.50	1.52
F	0.008	0.010	0.20	0.25
G	0.149	0.150	3.78	3.81
H		.600 typ		15.24
I	0.527	0.543	13.39	13.79
J	1.640	1.660	41.66	42.16

20-LEAD LCC



SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A		.040 typ		1.02
B		.050 typ		1.27
C	0.045	0.055	1.14	1.40
D	0.345	0.360	8.76	9.14
E	0.054	0.066	1.37	1.68
F		.020 typ		0.51
G	0.022	0.028	0.56	0.71
H		0.075		1.91

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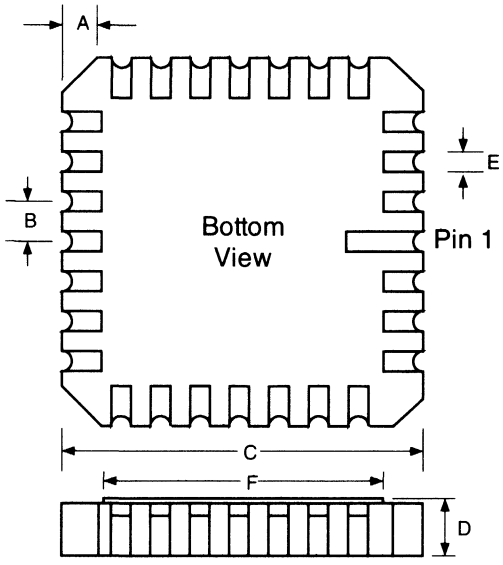
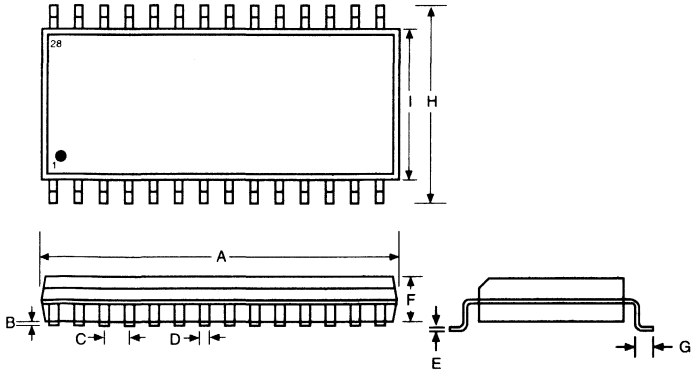
28-LEAD LCC



SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A		.040 x 45°		
B		0.050		1.27
C	0.442	0.458	11.23	11.63
D	0.060	0.070	1.52	1.78
E	0.022	0.028	0.56	0.71
F	0.396	0.412	10.06	10.46

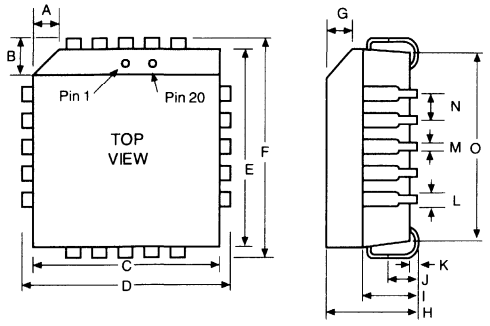
28-LEAD SOIC



SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.696	0.712	17.68	18.08
B	0.004	0.012	0.10	0.30
C		.050 typ	0.00	1.27
D	0.014	0.019	0.36	0.48
E	0.009	0.012	0.23	0.30
F	0.080	0.100	2.03	2.54
G	0.016	0.050	0.41	1.27
H	0.394	0.419	10.01	10.64
I	0.291	0.299	7.39	7.59

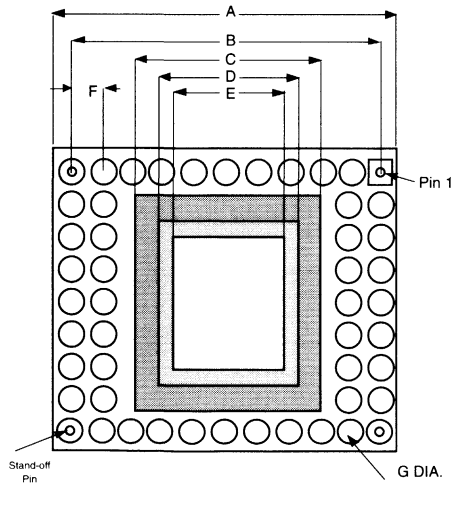
13

20-LEAD PLCC



SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A		.045 typ		1.14
B				
C	0.350	0.356	8.89	9.04
D	0.385	0.395	9.78	10.03
E	0.350	0.356	8.89	9.04
F	0.385	0.395	9.78	10.03
G	0.042	0.056	1.07	1.42
H	0.165	0.180	4.19	4.57
I	0.085	0.110	2.16	2.79
J	0.025	0.040	0.64	1.02
K	0.015	0.025	0.38	0.64
L	0.026	0.032	0.66	0.81
M	0.013	0.021	0.33	0.53
N		0.050		1.27
O	0.290	0.330	7.37	8.38

46-LEAD PIN GRID ARRAY



SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.890	0.910	22.61	23.11
B				
C	0.452	0.468	11.48	11.89
D	0.342	0.358	8.69	9.09
E	0.272	0.288	6.91	7.32
F		0.100		2.54
G	.045 dia	.055 dia	1.14	1.40
H	0.084	0.096	2.13	2.44
I	0.169	0.193	4.29	4.90
J	.020 dia	.030 dia	0.51	0.76
K	0.392	0.408	9.96	10.36
L	0.442	0.458	11.23	11.63
M	0.352	0.368	8.94	9.35

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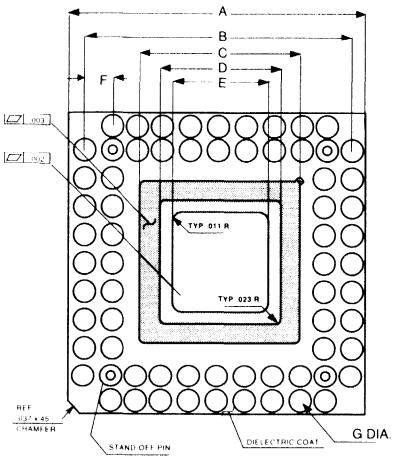
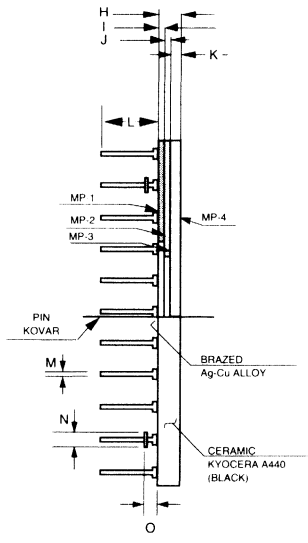
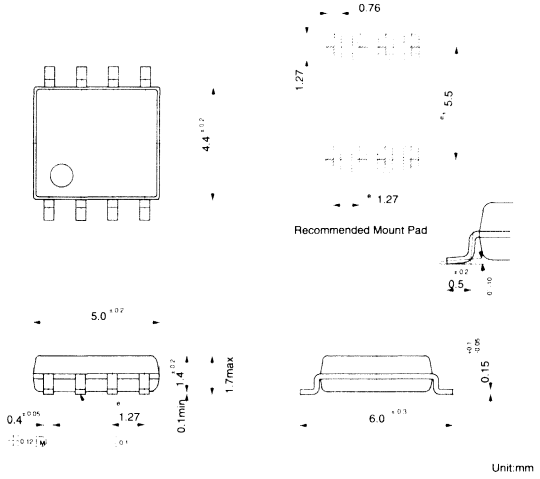
68-LEAD PIN GRID ARRAY



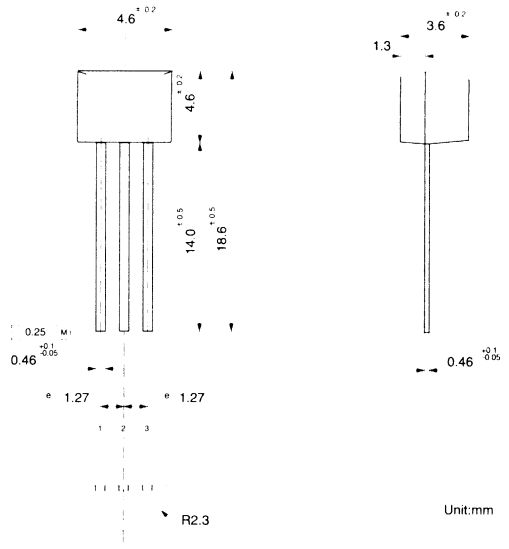


SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.089	1.111	27.66	28.22
B	1.090	1.110	27.69	28.19
C	0.594	0.606	15.09	15.39
D	0.445	0.455	11.30	11.56
E	0.345	0.355	8.76	9.02
F		.100 typ		2.54
G		.070 dia		1.78
H	0.067	0.083	1.70	2.11
I	0.023	0.027	0.58	0.69
J	0.018	0.022	0.46	0.56
K	0.027	0.033	0.69	0.84
L	0.150	0.170	3.81	4.32
M	.016 dia	0.02 dia	0.41	0.51
N		.050 dia		1.27
O		0.050		1.27

8-LEAD PLASTIC MOUNT (MFP-8)



3-LEAD PLASTIC (TO92-N)



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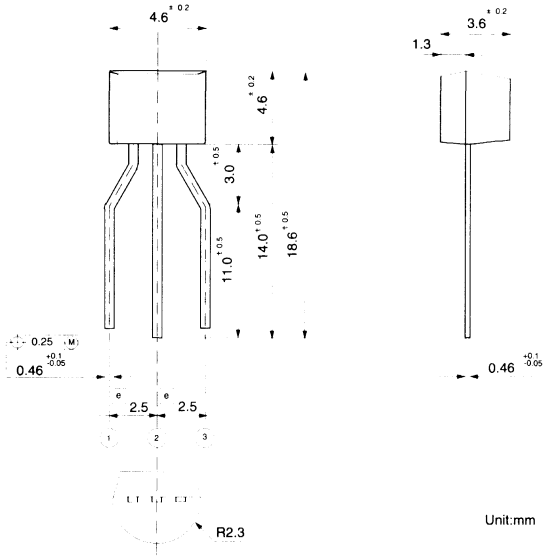
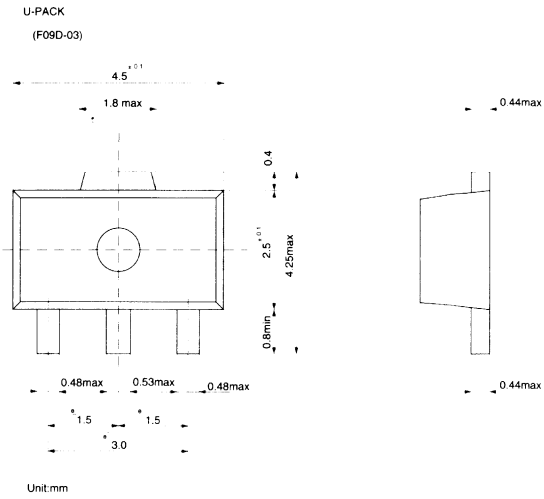
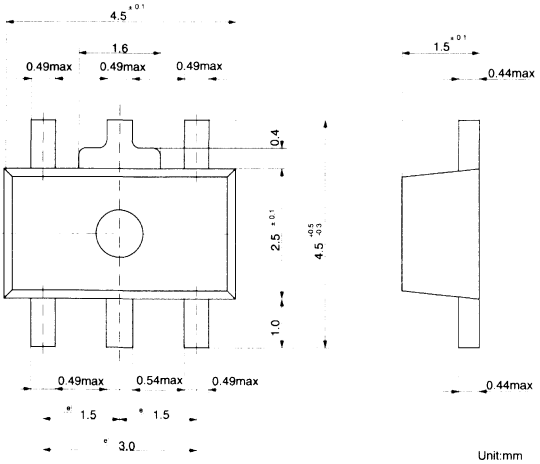
3-LEAD PLASTIC (TO92-NT)



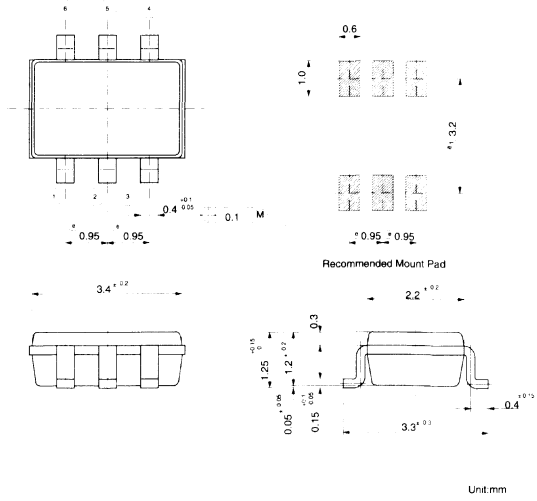
UPACK-3



UPACK-5



SOT23L



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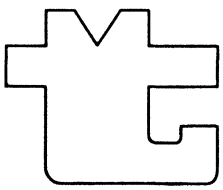

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